Design Optimization of Single-Ended and Differential Impedance PCB Transmission Lines

Gary Brist : Intel Corp.

Session Outline

- Signaling Technologies
  - I/O Trends
  - Differential Bus Designs
- PCB Fabrication Tolerances
  - Line Widths
  - Trace Thicknesses
  - Dielectric Thicknesses
  - Registration

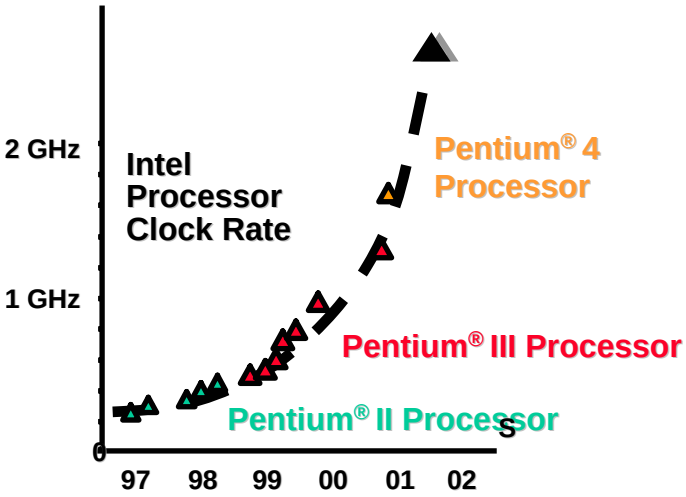
Session Outline

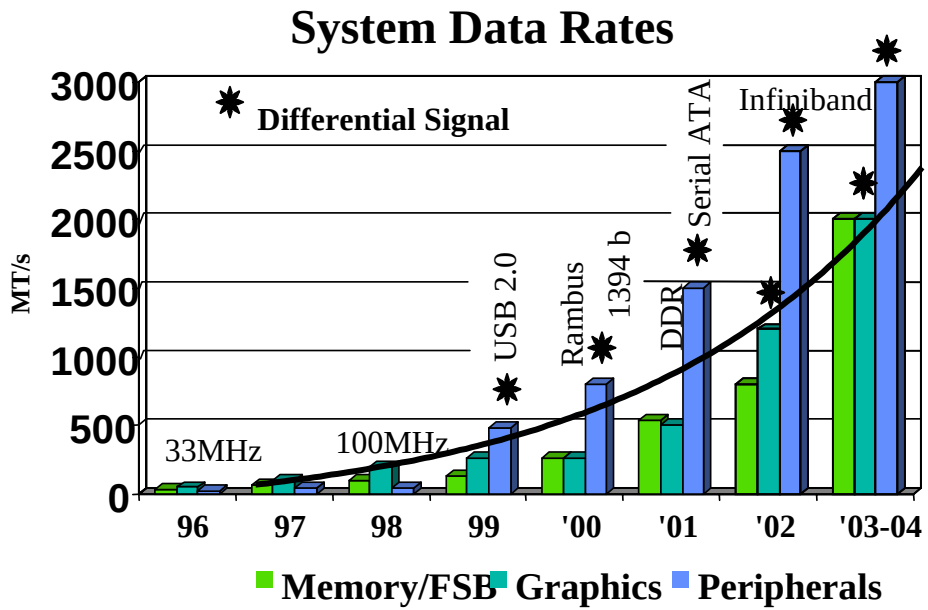
- Impedance Modeling
  - Review Common Impedance Structures
  - PCB Fabrication Impacts on Zo Tolerance
  - Measured Capability
- PCB Materials
  - Copper and Metallization
  - Dielectric Materials
    - Loss
    - Dielectric Constant
    - Spatial Properties

Signaling Architectures

Signaling Architectures
Trends

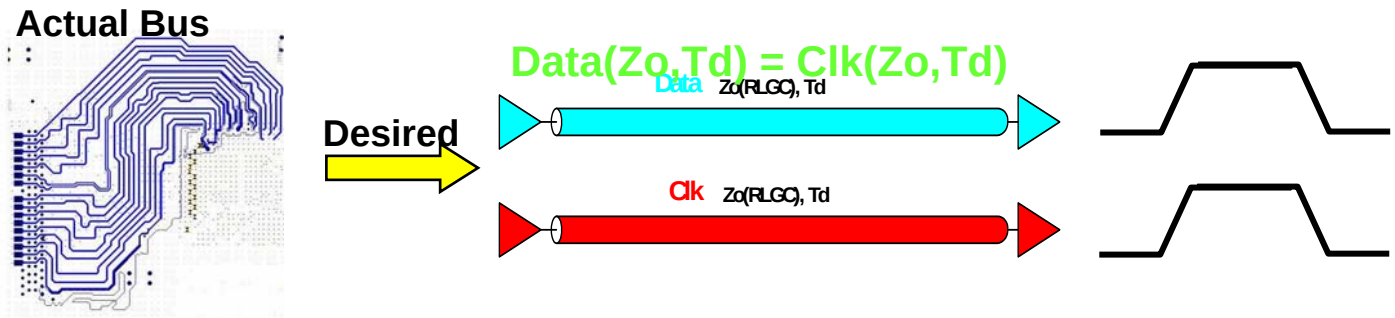
- Microprocessor performance growing exponentially
- Board level interconnects must keep pace with silicon performance





Signaling Architectures
Current I/O Bus Design Challenges

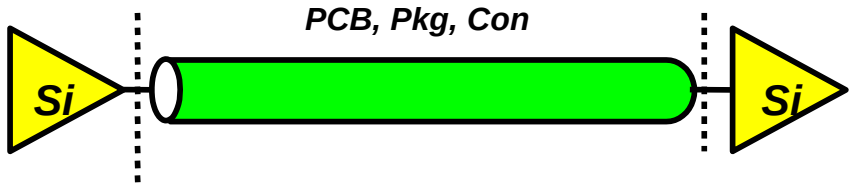
- Clk-data relationships (Source Synchronous designs)
  - All signals and clock must arrive within a specific period of time
- Clock impedance and data impedance need to be equivalent
- Transmission attenuation increases as frequencies increase
- Processor voltages decreasing



Localized differences affect performance

Signaling Architectures
Increasing I/O performance

- Silicon solutions
  - New IO bus architectures
  - Signal compensation techniques
- Design solutions
  - Point to Point improves Zo reflections
  - Uniform Zo Chip to Chip
- Physical Interconnect Solutions
  - Decrease Zo tolerance
  - Decrease bus lengths
    - **Issue:** Physical lengths difficult to scale
  - Decrease Dk and Material loss
    - **Issue:** Limits to scaling material properties
    - **Issue:** Difficult to introduce new materials each Si generation



Signaling Architectures
Technology-Architecture Options

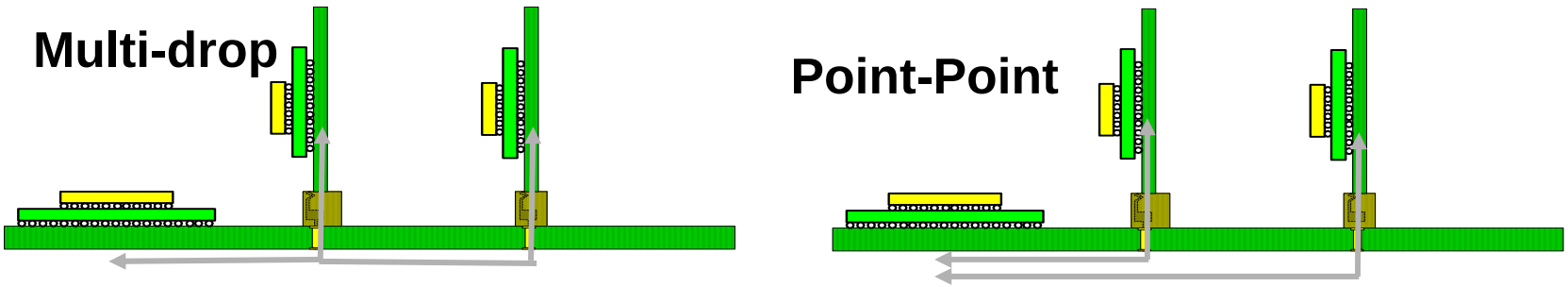
- Silicon Technology
  - Moore's Law
    - More transistors per area each generation
    - Transistor cost decreases each generation
    - Allows more complex IC design each generation
  - IC designs designs can compensate for predictable variations.
    - Loss equalization
      - Requires predictable loss(dielectric + conductor)
    - Narrow band encoding
      - Requires constant DK above fundamental clock freq
- Physical Interconnect solutions such as new materials to meet improved electrical properties will be under cost pressure from Si technology

Localized variations must be predictable

Signaling Technologies

Technology-Architecture Options

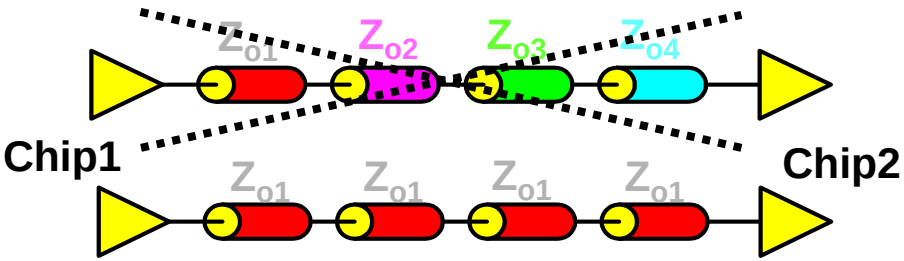
- Point-Point improves the channel performance.
  - Less pressure on physical ingredients
    - Packaging, Connectors, PCB
- Point-Point vs IO counts
  - IO counts increase if design at same data rates
  - Increase data rate and reduce IO count while maintaining bandwidth.

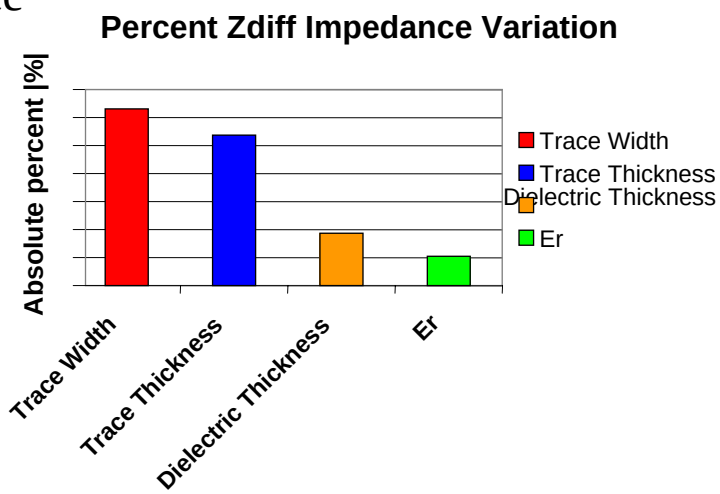


Point-point improves the channel

Signaling Architectures
Technology-Architecture Options

- Impedance (Zo) Uniformity
  - Maintain uniformity from chip to chip within the design.
    - Within differential pair matching
    - Package to Socket to PCB
  - Uniform Zo along transmission path (trace)
    - Fabrication feature control along trace
    - Consistent Zo layer to layer



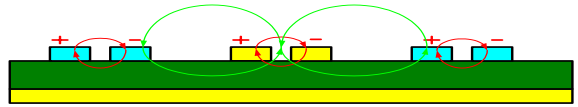


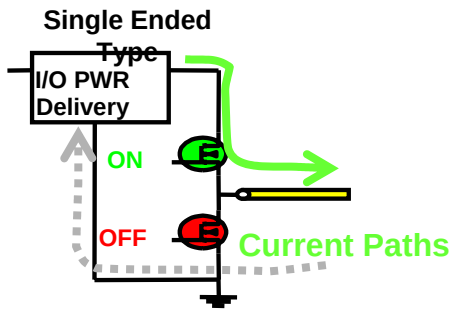
Uniformity of the PCB design is critical

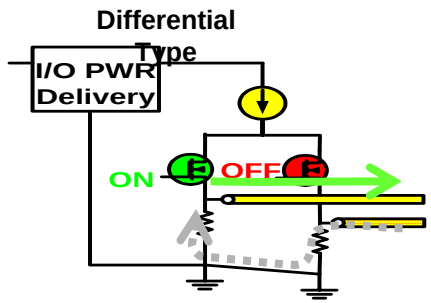
Signaling Architectures

Technology-Architecture Options

- Differential Signaling
  - Improves system noise immunity
  - Improves silicon I/O performance
    - Lowers I/O power delivery sensitivity
  - Improves Interconnect performance
    - Allows higher transmission loss thresholds
  - Added sensitivity to fabrication tolerances







Lower noise results in higher Performance

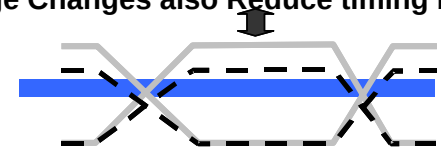
Signaling Architectures
Differential Signaling

- Differential signaling being used for data rates > ~1GT/s
- Differential interconnect signal quality defined by ‘eye’ opening
- Performance interaction ‘eye’ quality and receiver sensitivities

‘Eye’ Quality

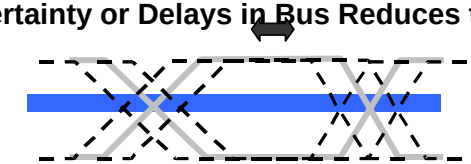
Voltage Changes also Reduce timing budgets

Dielectric & Conductor Loss
Zo Reflections,
Crosstalk, etc



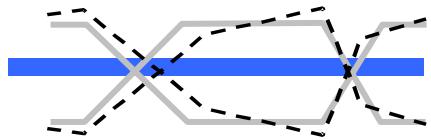
Timing Uncertainty or Delays in Bus Reduces timing budgets

Dk variations, Zo Reflections
trace vs clk flight time



Signal Transformation Reduces Timing and Voltage budgets

Dk variations w/ freq
Zo Reflections
ISI



Signaling Architectures
Summary

- High speed IO moving toward differential signaling

- Silicon solutions driving interconnect requirements
  - Dielectric constant uniformity
    - Within and across an IO bus
    - Constant with frequency
  - Minimimal impedance reflections
    - Impedance uniform along interconnect (trace)
    - Point to Point architectures
  - Deterministic losses required
    - Accurate predictability

PCB Fabrication Tolerances

Line Widths

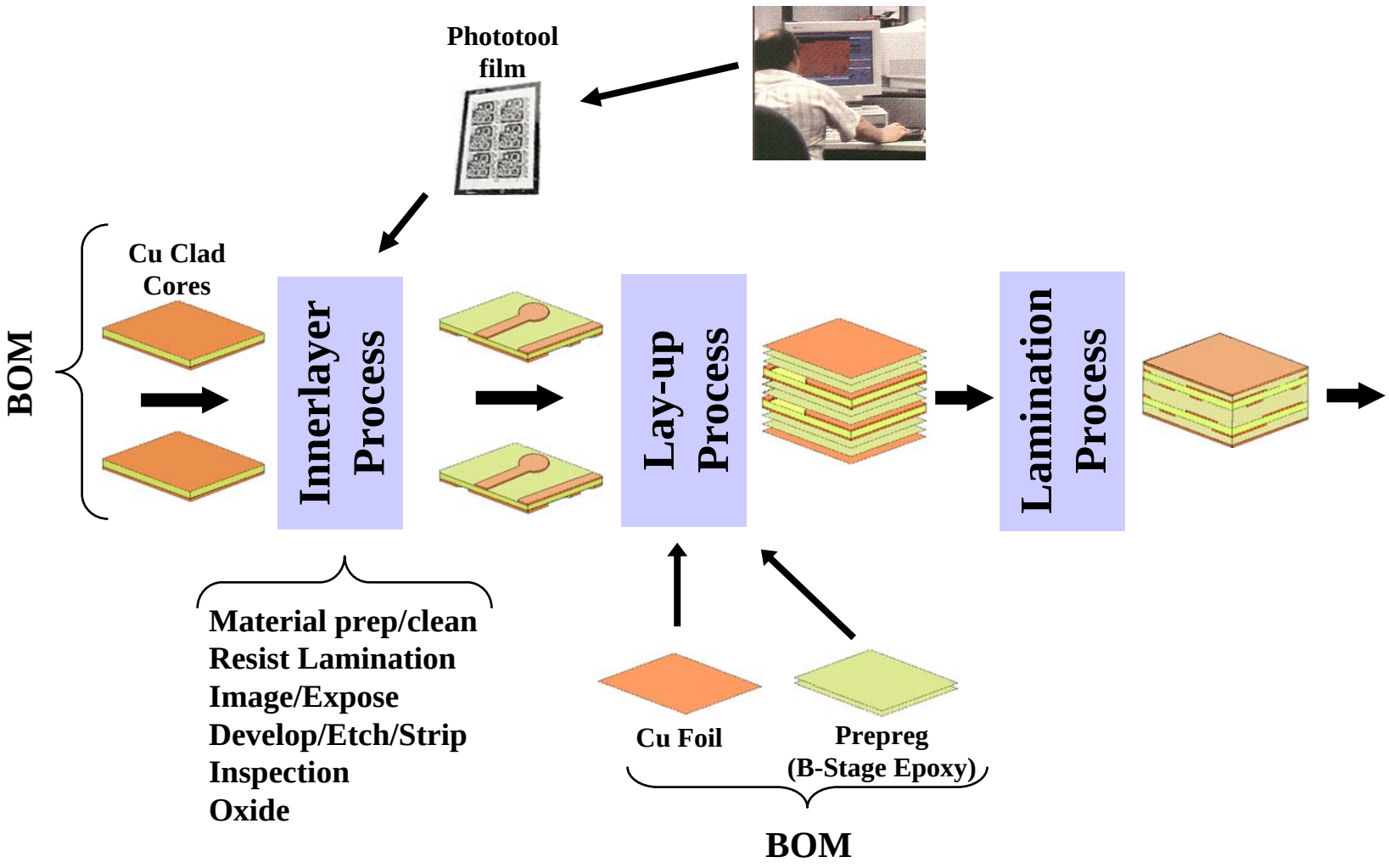
Line Defects

Trace Heights

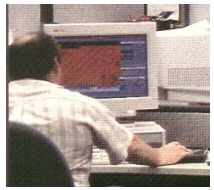
Material Thickness

Image Registration

Process Flow Overview

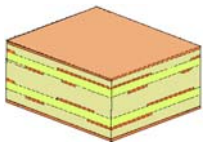


Process Flow Overview

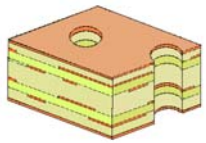


Drill Table

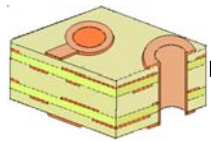
Phototool Film



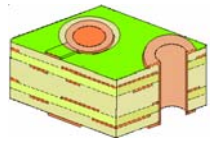
Drill Process



Outerlayer Process



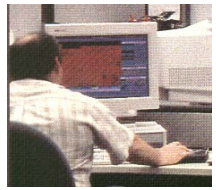
Soldermask Process



PTH/Strike Plate
Resist Lamination
Image/Expose
Develop
Pattern Plate
Strip/Etch/Strip
Inspection

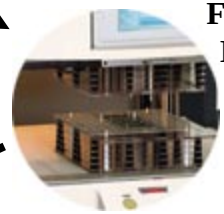
Soldermask Coat
Image/Expose
Develop
Nomen Screen

Process Flow Overview

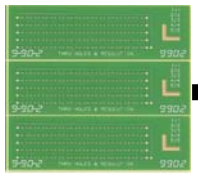


Netlist

Fixture Build



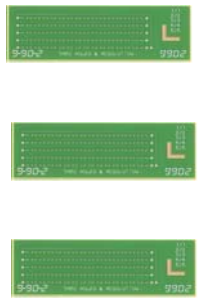
Route Profile



Surface Finish

HASL
Immer Au

Finishing Process



Score
Unplated Drill
Beveling
Route

Electrical Test

TDR
Serialization
Hi-Pot
Continuity

Surface Finish

OSP
Immer Ag
Immer Sn

Audit Shipping

PCB Fabrication Tolerances

Line Widths

Line Defects

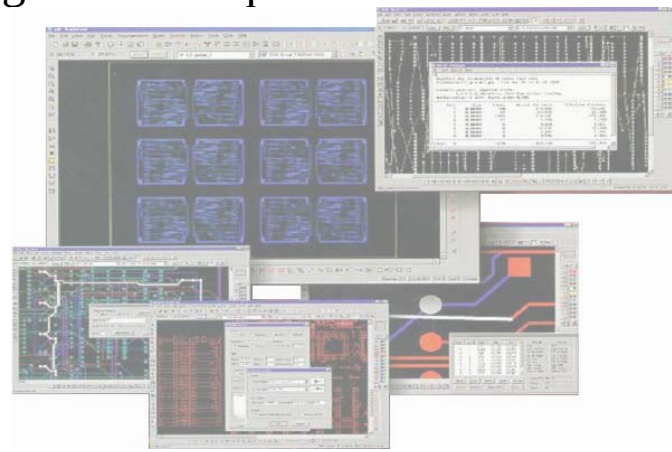
Trace Heights

Material Thickness

Image Registration

CAD to fabrication tools

- Gerber data sent to a PCB fabricator goes through a series of processes
  - DFM checks to ensure no violations
  - Drill size modification/selection to meet Finished hole specifications and optimize plated aspect ratio and drill registration
  - Line width modification to meet Zo requirements
  - Soldermask modifications to meet clearance/registration requirements
- Panelization of modified Gerber data
  - Stepped to maximize material utilization.
  - CAD definition of all tooling holes / targets
    - Imaging, alignment during fabrication.
  - Coupons added
    - (Zo, Registration controls, reliability, PTH, etc)
  - Thieving added to improve plating uniformity
  - Dam/Vents added to internal layers to optimize lamination



CAD to fabrication tools

- Plotters
  - Predominant plotters used by PCB fabricators run at 0.25mil or 0.125mil pixel size
  - Many plotters can switch between the two different resolutions.
    - 0.125 (1/8th)mil resolution requires 4x data transfer and ~4x plot time compared to 0.25 (1/2)mil
    - 0.125mil resolution usually reserved for fine lines (<3mil lines)
  - Play significant role in imaging capability
    - Line acuity (sharpness of transition between clear and black on film) affects line width tolerances and photoresist defects
    - Plotted shapes limited to increments of resolution
      - Such as 7.5mils, 3.75mils
      - NOT 4.9mils or 4.1mils

Designer Note: Keep all features on 1/4th mil increments

Innerlayer Processing: Develop/Etch/Strip

- Chemical process to develop resist, etch exposed Cu and strip off undeveloped resist.
- Two primary etch chemistries utilized
  - Cupric chloride (preferred because of slower etch rate and better control)
  - Ammoniacal etching
- Etching parameters
  - pH, pressure, line speed, temperature
  - Line speed usually selected as in-process control variable
- Etching different Cu weights or cores with unbalanced Cu
  - Line speed

    And/Or
  - Turning off selected sprayers within etch chamber

Innerlayer Line Widths

Variations Sources

- Phototool and Imaging
- Etcher line setup for Cu weight and circuit density
- Within panel variation also controlled by
  - Circuit density
  - Chemistry pooling factors

Develop/Etch/Strip

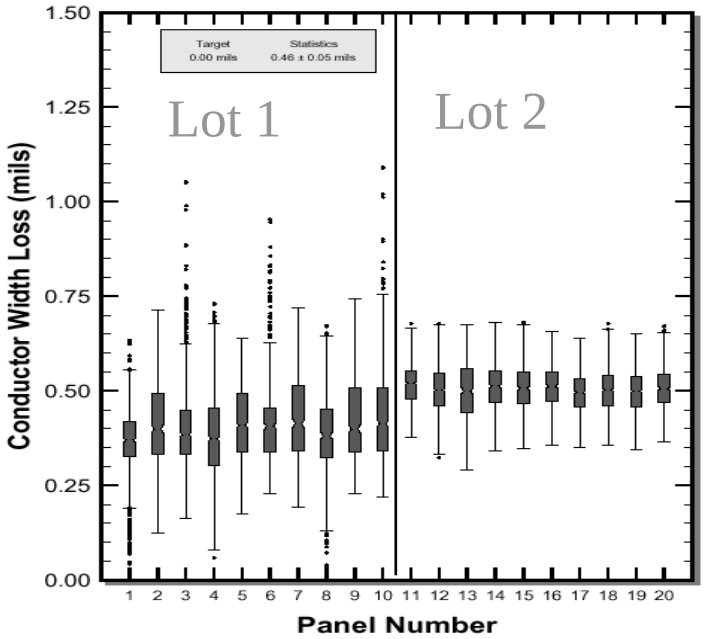
•Etching occurs with chemical etchant delivered through spray nozzles.
•Etcher chamber consists of multiple oscillating spraybars

•Etching process defined by
  - •Bath ph and temperature
  - •Spray pressure
  - •Nozzle placement and size
  - •Conveyor speed

Innerlayer: Line Widths

Typical High-End Supplier Data

Intra-panel variations (~50 test structures per panel)



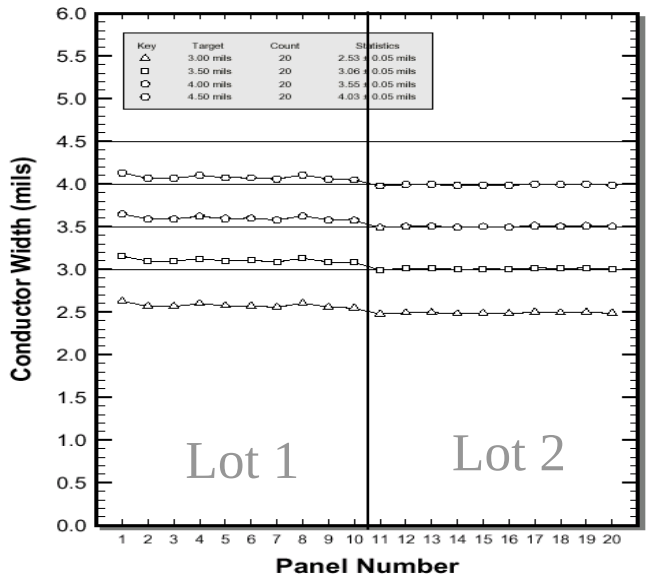
Different etcher – same supplier

Innerlayer Tolerance

~ +/-0.3-0.5mils @3σ

(review of 3 High-End suppliers over 12months)

Panel averages

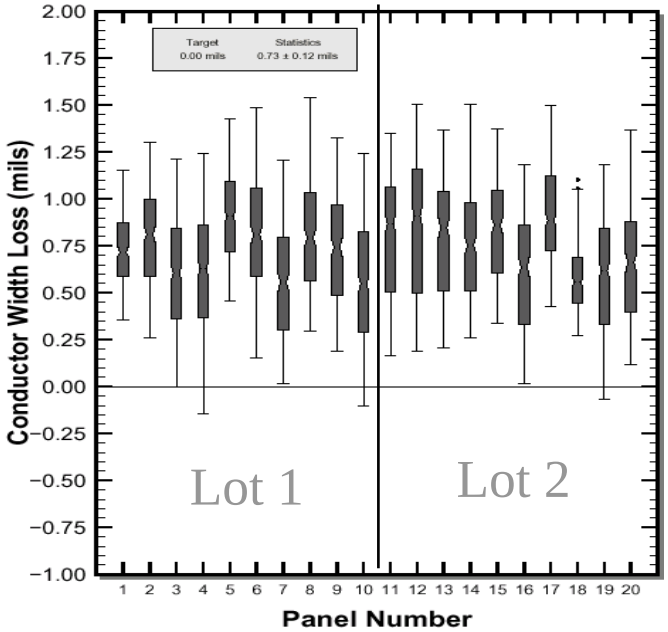


Designer Note: Line width tolerance (in +/-mils) is same for all line widths

Innerlayer Line Widths

Typical HVM Supplier Data

Intra-panel variations (~50 test structures per panel)

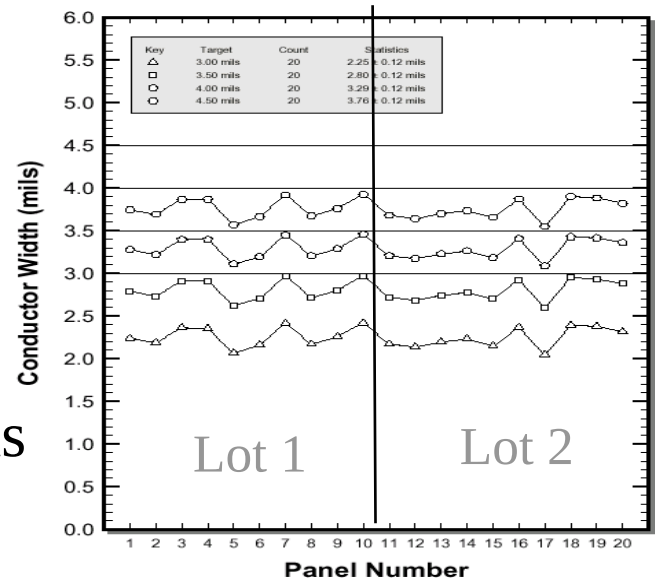


Innerlayer Tolerance

~ +/-0.50-1.0mils @3σ

(review of 9 HVM suppliers over 12months)

Panel averages

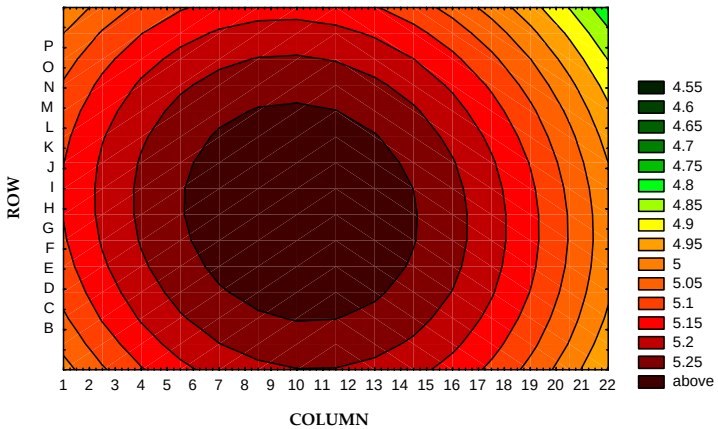


Significant panel to panel variations

Innerlayer Line Widths

Within Panel Line Width Variation

Lot average by location



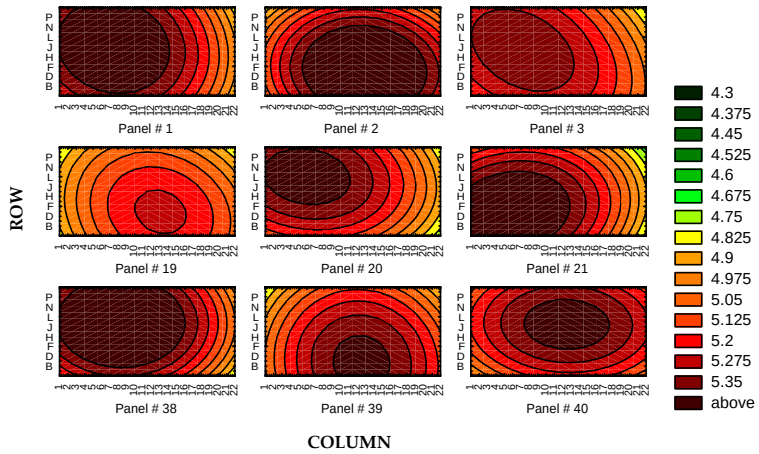
18x24 panel

Contours from 50 data points per panel.
-Shows localized uniformity can be fairly low.

•Signature of horizontal conveyor etching without intermittent sprays.

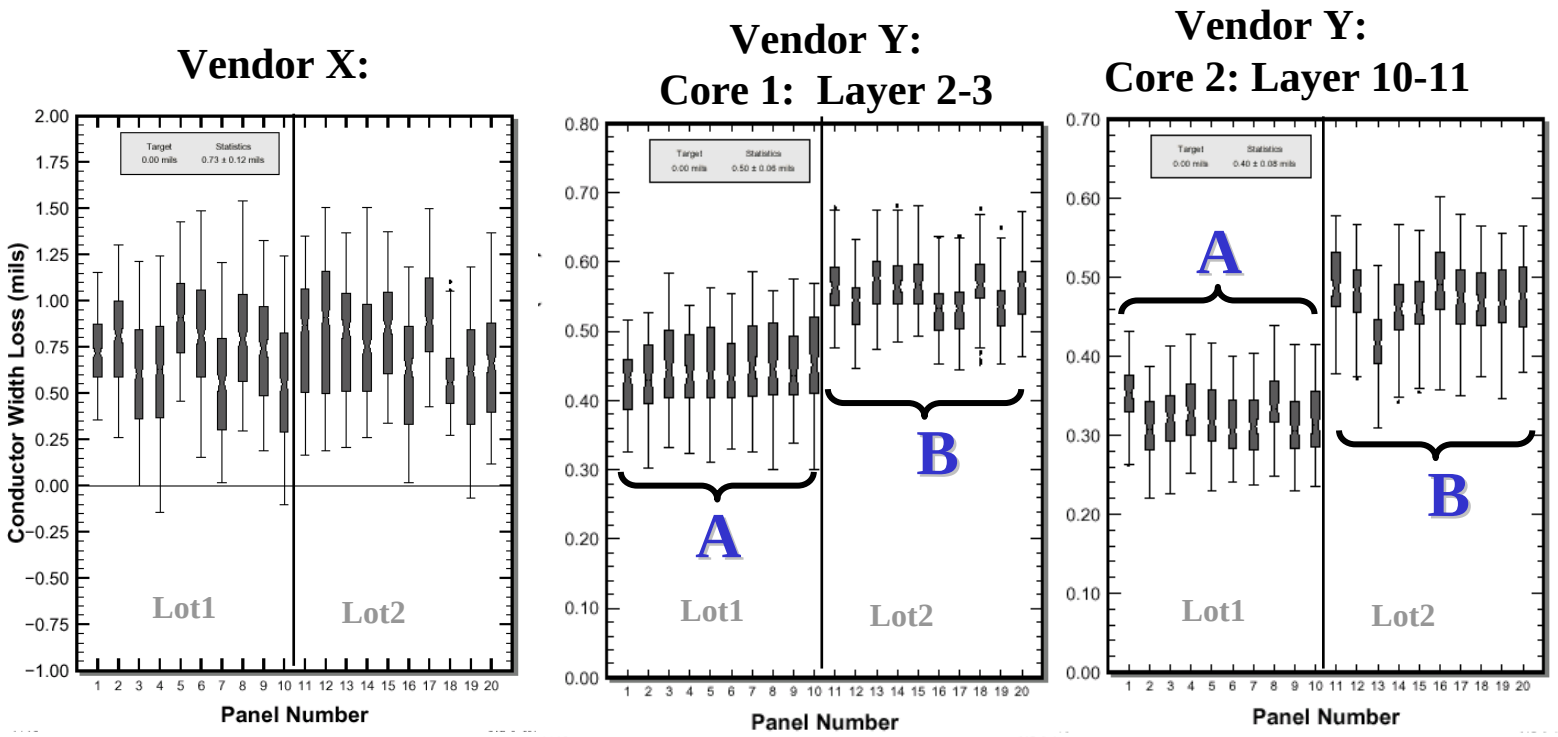
•Intermittent sprays can minimize trailing edge variations

Individual panel data



Innerlayer Line Widths

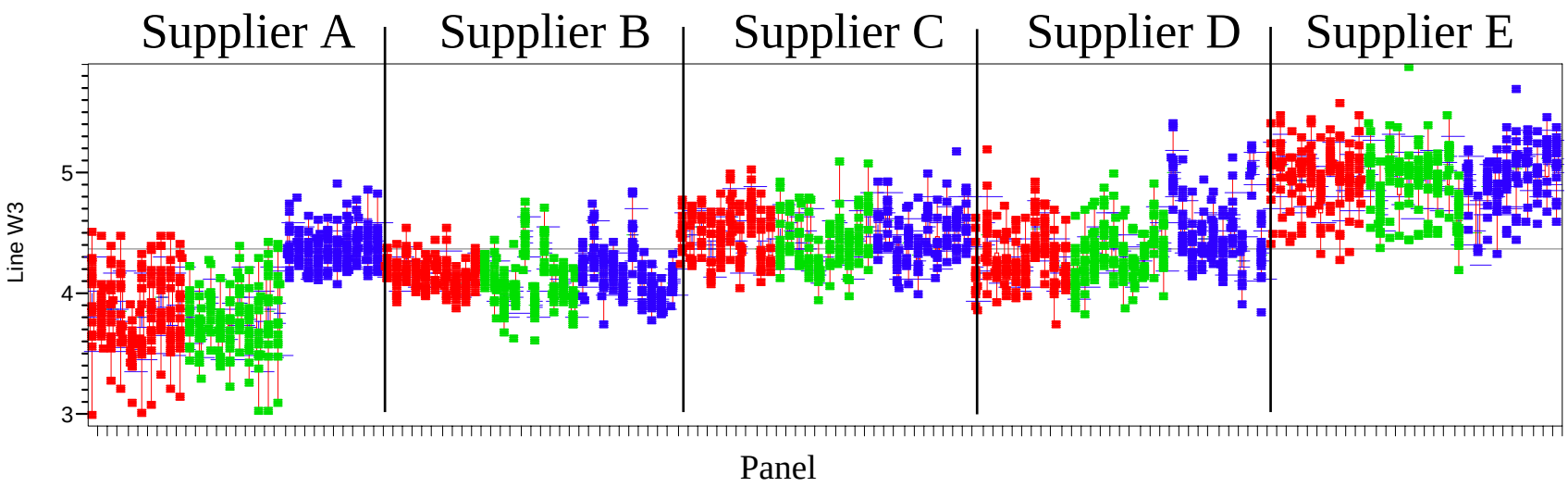
Lot-Lot and Layer-Layer Variations



- Mean shifts between lots not noticeable with Vendor X due to larger within panel variation.
- Panels run at same etcher set-up (different cores or layers) give consistent results (A vs B)
- Within panel variations dependent on supplier (process control)

Innerlayer Capability – Conductor Width

(Rev3 test board – Measured Data - 1oz foil)



- Notes:
  - Suppliers did not adjust film tools to achieve a specified line target.
  - Data on 1oz innerlayer copper

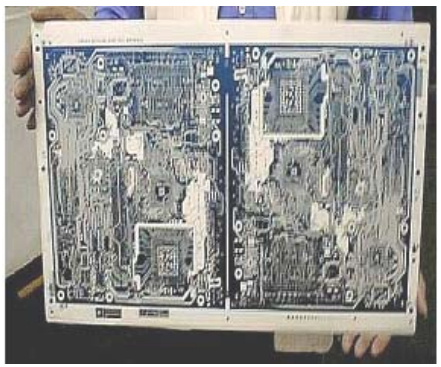
Innerlayer Line Widths

Key Modeling Points

- Supplier line width control across a lot ranges from **+/-0.25** to **+/-1.00mils** (3sigma analysis)
- Line width variation is uniform across all line widths
- Lot to lot variation more pronounced with suppliers who have lower within panel line width variation
- Majority of line width variation occurs on a single layer within an individual panel

Outerlayer Plating and Imaging: Pattern Plating

- Electrolytic Copper plating followed by Electrolytic Tin plating
  - Copper plating to increase the hole wall and circuitry copper thickness
    - Process time dependent on via aspect ratio and minimum Cu thickness
    - Copper grain structure dependent on deposition rate and bath additives
    - Reverse Pulse plating gaining popularity to control plating thickness uniformity.
  - Tin plated onto panel as an etch resist
    - Tin plating critical to control of opens within via
  - Vibration and agitation systems used in vertical lines to prevent air entrapment in holes
- Vertical equipment most standard due to long process times.



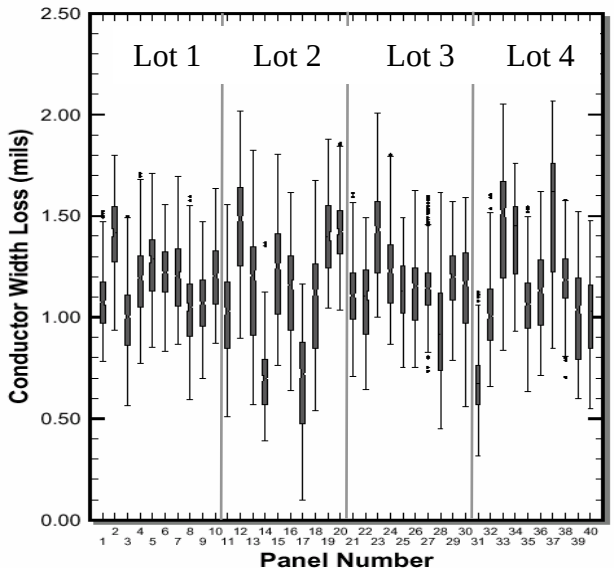
Plating

Outerlayer Plating and Imaging: Strip-Etch-Strip

- Final step in the formation of outerlayer circuitry
  - Process consists of three main sub-processes
    - Strip resist to expose unwanted Cu surface
    - Etch exposed Cu surface
      - Ammoniacal etching (alkaline)
    - Strip tin to expose desired Cu circuitry
  - Horizontal Conveyor line
- Controlling Line widths is similar to innerlayer DES (Develop-Etch-Strip) process
  - Conveyor speeds can be adjusted
  - Etch process defined by spray pattern, spray pressures, and temperatures, etc.
  - Plating thickness distribution across the panel also critical

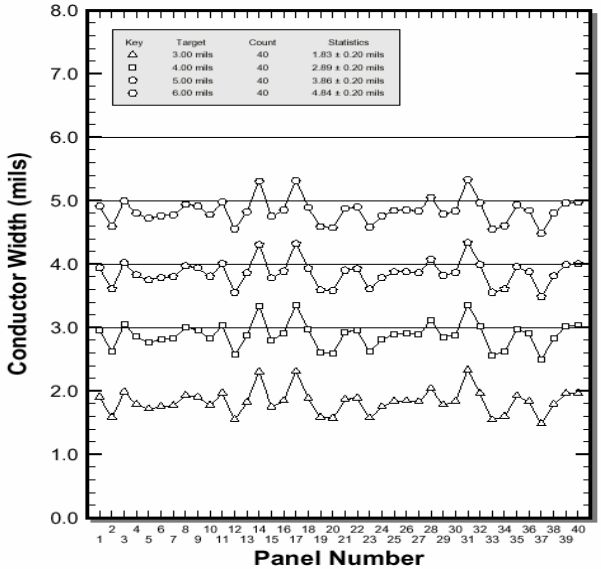
Outerlayer Line Widths
Typical HVM Supplier Data

Intra-panel variations (~50 test structures per panel)



Outerlayer Tolerance
~ +/-0.6-1.0mils @3σ
(review of 7 HVM suppliers over 12months)

Panel averages

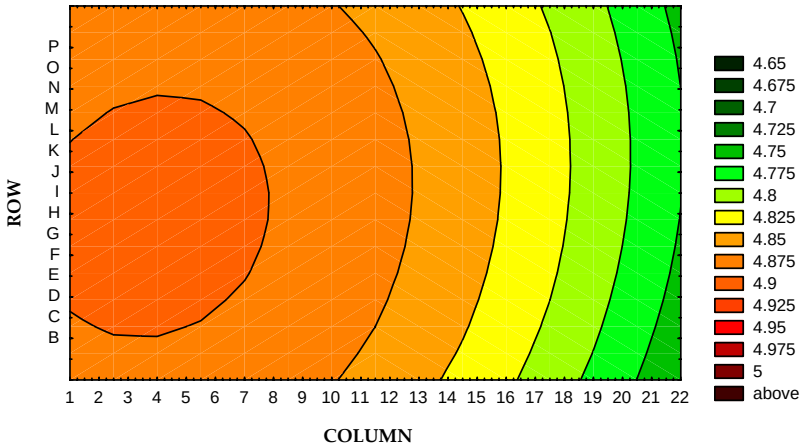


Significant portion of variation occurs within panel
Noticeable panel to panel nominal shifts

Outerlayer Line Widths

Within Panel Line Width Variation

Lot average by location



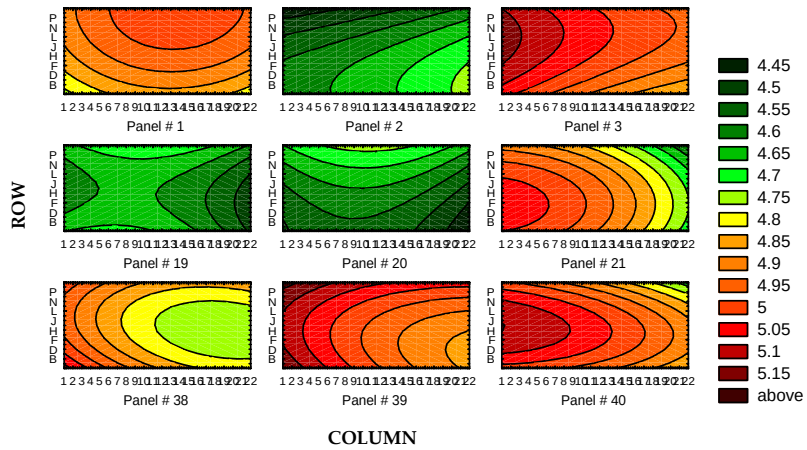
18x24 panel

Contours from 50 data points per panel.
-Shows localized uniformity can be fairly low.

•Lot average show signature of horizontal conveyor etching.

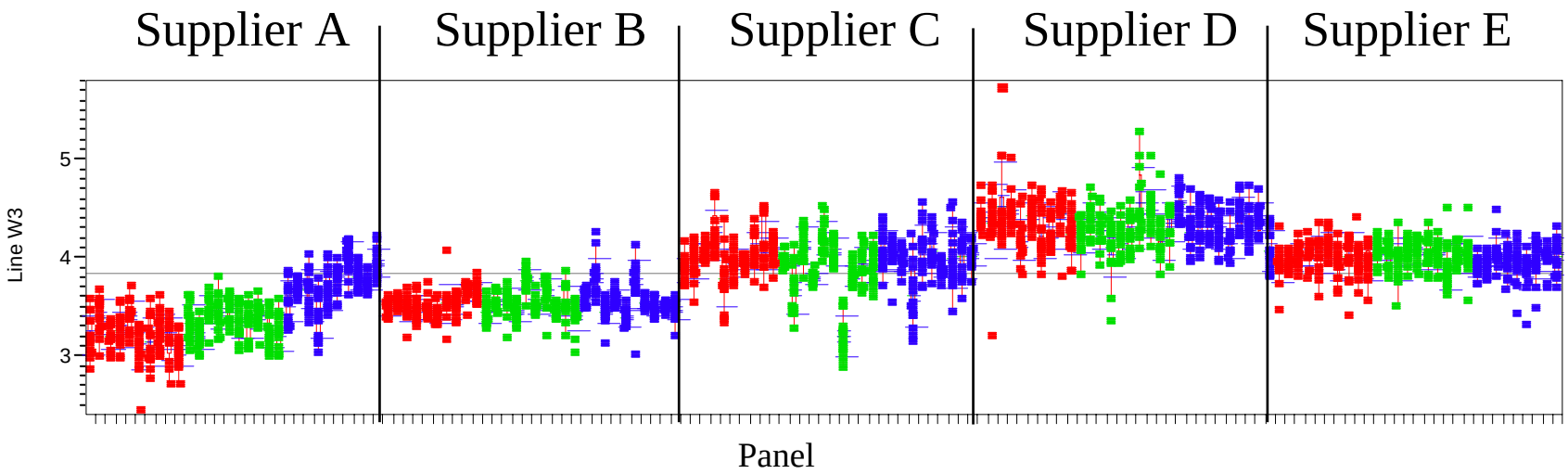
•Individual panels show effect of plating distributions across a plating bar (Field effects between anode-cathode)

Individual panel data



Outerlayer Capability – Conductor Width

(Rev3 test board – Measured Data)



- Notes:
  - Suppliers did not adjust film tools to achieve a specified line target.

Outerlayer Line Widths

Key Modeling Points

- Supplier line width control across a lot ranges from **+/-0.5 - +/-1.00mils** (3sigma analysis)
- Line width variation is uniform across all line widths
- Dependency of line width variation on plating aspect ratio at an individual supplier
- Spatial distribution of line width variation different than innerlayers and heavily dependent on Electroplating equipment configuration.

PCB Fabrication Tolerances

Line Widths

Line Defects

Trace Heights

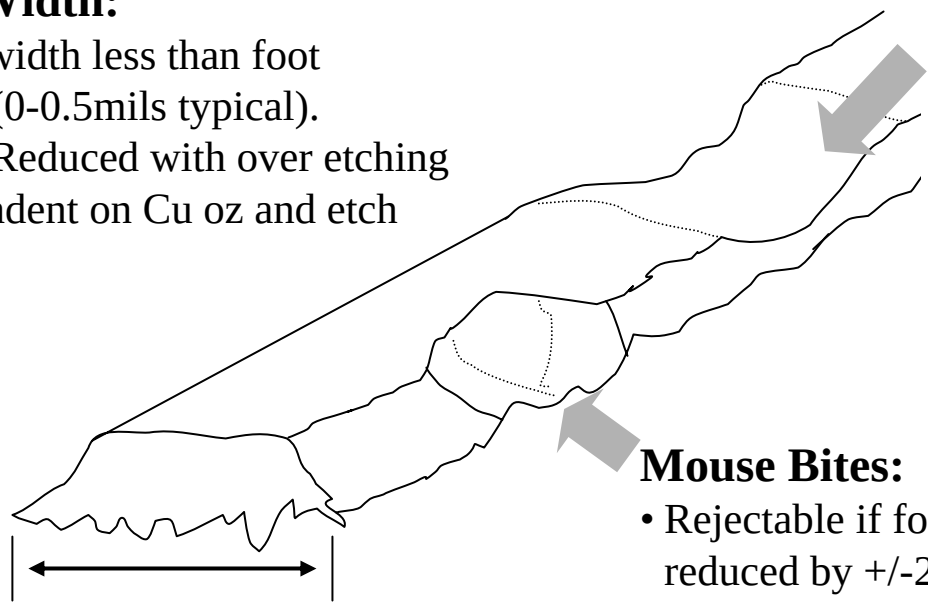
Material Thickness

Image Registration

Line Defects:
Localized width variations

Top Width:

- Top width less than foot
  - (0-0.5mils typical).
  - Reduced with over etching
- Dependent on Cu oz and etch factor.



Depression:

- Close to full width - reduced height.
- Unacceptable per IPC
- Difficult to catch with AOI

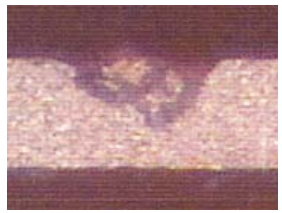
More common than admitted

Mouse Bites:

- Rejectable if foot of trace is reduced by +/-20%.
- Many shops will ship if reductions <50%

Measured Width:

- Rejectable per IPC if +/-1mil or +/-20% from design.
- Line width can vary up to +/- 0.3-0.5 mils along trace length.



Line Defects

Key Modeling Points

- Acceptable and Unacceptable trace variations exist on shipped product
- Line defects will impact Impedance and signal reflections
- Dimensions typically small enough not to influence bus performance at <5-10GHz

PCB Fabrication Tolerances

Line Widths

Line Defects

Trace Heights

Material Thickness

Image Registration

Trace Heights
Base Foil only

- Cu foil available in different standard thicknesses
  - Thickness based on #oz per sqft
  - 1oz = ~1.3-1.4mils in initial thickness
  - 0.5,1,2oz foils most common
  - ¼,$^{3}/_{8}$,3oz foils available
- Cu foil suppliers
  - Control thickness very well
  - Always on very low end of allowable spec (Extra Cu = lost profit to Cu foil supplier)

Trace Heights
Base Foil only

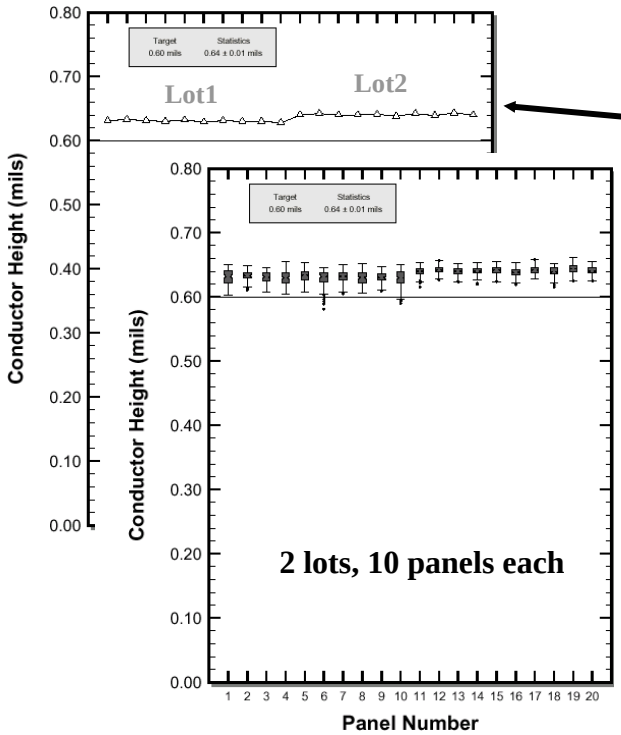
- Main variations within PCB fabrication is oxide or oxide alternative processes
  - Oxide etch usually in range of 30-70uin
    - Lot-Lot variation based on pH control
    - Panel-Panel and Within panel variation based on dosing control and bath agitation
  - Panel may see multiple pass through oxide process for rework causing lot-lot shifts
- Some foils require removal chromate conversion coatings.

Trace Heights

Base Foil Data after Process

Designer Note: Cu foil thickness within panel and between lots
<+/-0.05-0.10mils on 1/2oz
<+/-0.10-0.25mils on 1oz

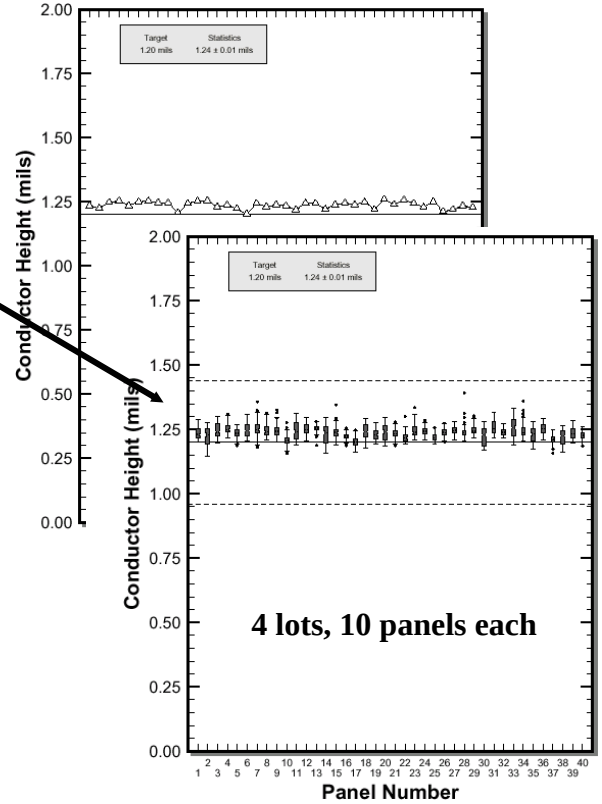
Vendor A:



Panel averages

Within panel values

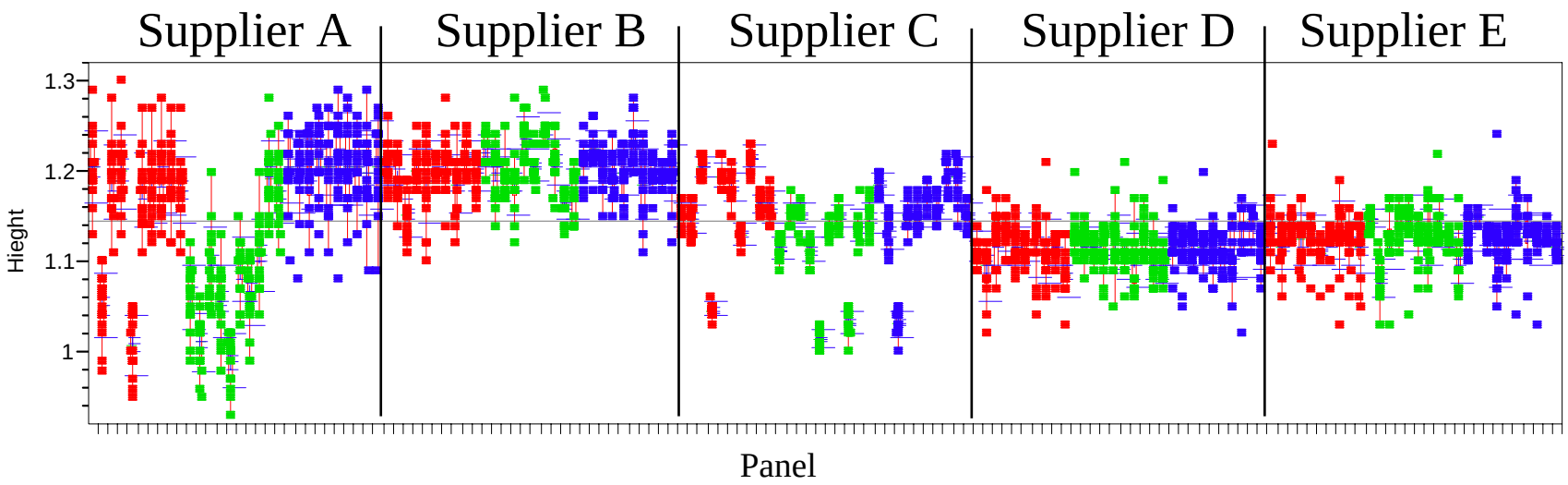
Vendor B:



Vendor A lot1 experienced a oxide rework process (2nd pass through oxide)

Innerlayer Capability - Conductor Height

(Rev3 test board – Measured Data – 1oz foil)

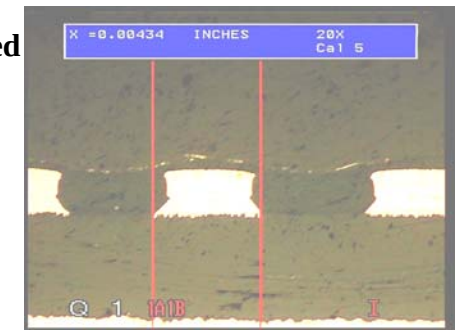


- Notes:
  - Vendor A had rework issues (I.e. foils twice through oxide process) on lots 1 and 2

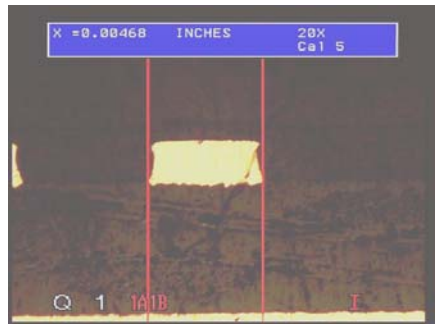
Trace Heights
Plated Cu

- Plating thickness distribution dependent on local circuit density across panel
- Dependent on drill size and panel thickness (aspect ratio)
  - Small vias and/or thicker PCB (High Aspect ratio) requires a longer plating time to get minimum acceptable Cu in center of via.
- Plating thickness distribution also dependent on anode/cathode placement within plating tank.
  - Many vertical plating tanks hold 4-8panels across
  - Distribution not uniform across tank
- Trace shape dependent on thickness and etching process.

Underetching resulted in non-rectangular profile. Top rectangular section resulting from resist profile



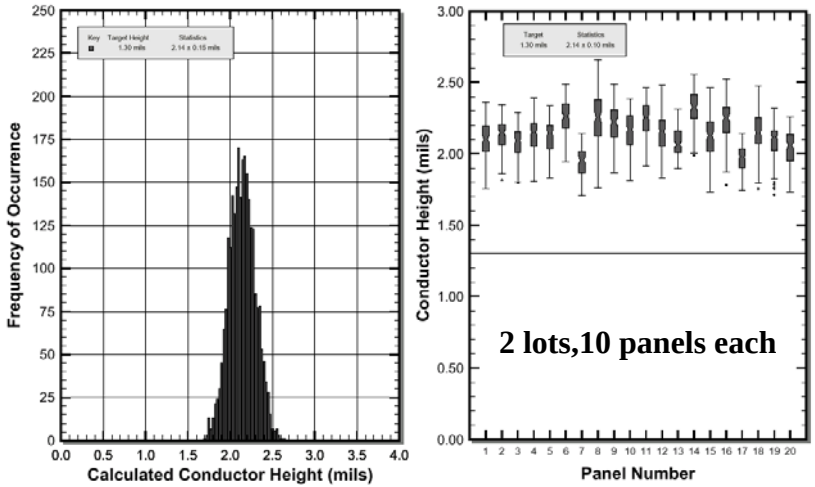
Overetching resulted in top and bottom close in width and trace almost rectangular.



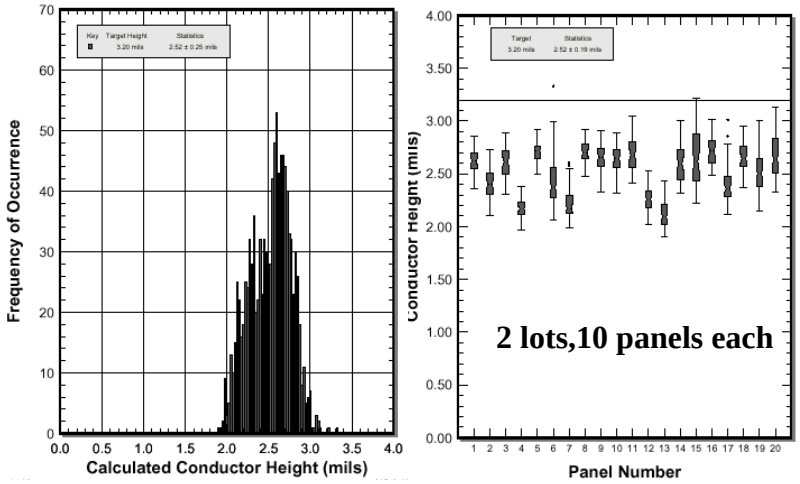
Trace Heights: Plated Cu

- All suppliers achieve a different average plating thickness.
  - 1st priority of plating is to achieve minimum Cu thickness within the vias
  - Plating surface thickness not adjusted to achieve a nominal
  - Increased Cu plating thickness will increase reliability of PTH
- High-End suppliers may not have lower thickness variation across a lot or panel.
- Reverse Pulse Plate systems being installed in both HVM and High-End fabricators to address thickness issues and high-aspect ratio plating.

Vendor A: **Base foil = 0.5oz (0.65mil)**

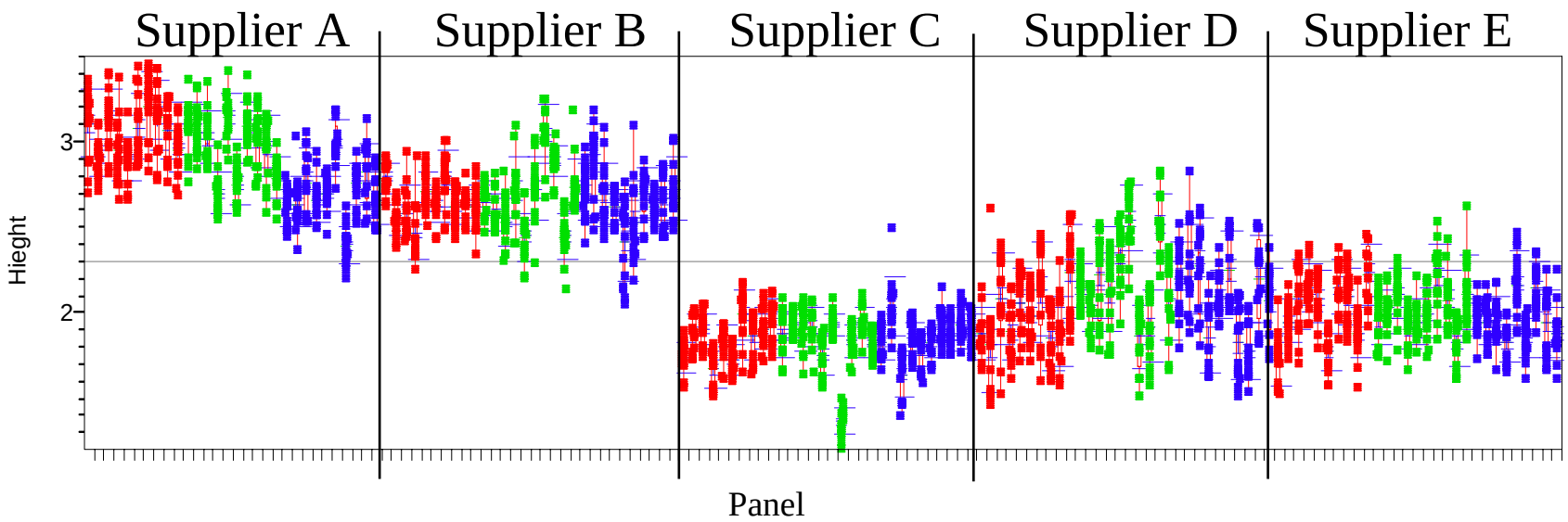


Vendor B: **Base foil = 0.5oz (0.65mil)**



Outerlayer Capability – Conductor Height

(Rev3 test board – Measured Data)



- Notes:
  - All vendors started with 1.0oz foil
  - Suppliers C and E utilize a copper foil reduction prior to plating which lowers the overall copper thickness

Trace Height
Key Modeling Points

- Innerlayer / Base foil very tightly controlled
- Innerlayer / Base foil variation and lot-lot variation predominantly fabricator process dependent
- Plated trace thickness has high variation

PCB Fabrication Tolerances

Line Widths

Line Defects

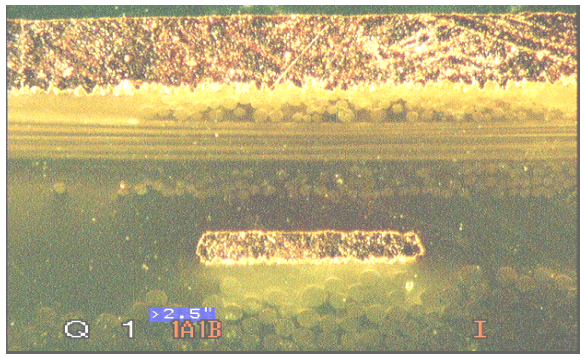
Trace Heights

Material Thickness

Image Registration

Dielectric Thickness Variation within FR4 material

- Dependent on glass thickness and resin amount
- Core thickness defined by laminate supplier – not dependent on PCB fabricator
- Pressed thickness of Prepreg
  - Cu Thickness
  - Circuit density



Partial Cross section of laminated PCB

Designer Note: Within an individual panel: thickness and Zo variations are minimized by uniform layout-circuit density

Laminate Thickness

Sample FR4 Material Table

Dielectric Properties Table - N4000-2, N4000-6, N4000-6FC

12/19/00

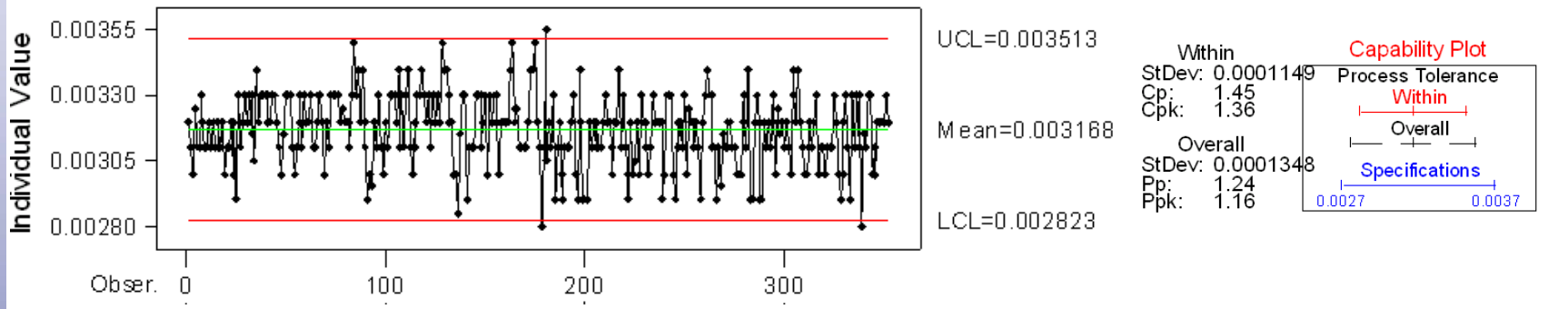
LAMINATE

Thickness	& Tolerance	Construction	RC	1MHz	1 GHz
0.002	± 0.0005	1 x 106	69.0%	3.84 ± 0.34	3.63 ± 0.36
0.003	± 0.0005	1 x 1080	62.0%	4.00 ± 0.33	3.80 ± 0.34
0.004	± 0.0005	1 x 2113	54.5%	4.19 ± 0.36	4.00 ± 0.38
0.004	± 0.0005	1 x 106 + 1 x 1080	57.7%	4.11 ± 0.32	3.91 ± 0.34
0.004	± 0.0005	1 x 2116	43.0%	4.54 ± 0.54	4.37 ± 0.57
0.005	± 0.0005	1 x 106 + 1 x 2113	52.8%	4.24 ± 0.34	4.05 ± 0.36
0.005	± 0.0005	1 x 2116	51.8%	4.26 ± 0.35	4.08 ± 0.37
0.006	± 0.0005	1 x 1080 + 1 x 2113	52.2%	4.25 ± 0.32	4.06 ± 0.34
0.006	± 0.0005	1 x 106 + 1 x 2116	50.8%	4.29 ± 0.33	4.11 ± 0.35
0.006	± 0.0005	2 x 2113	43.5%	4.52 ± 0.43	4.35 ± 0.46
0.006	± 0.00075	1 x 1500	41.7%	4.58 ± 0.57	4.41 ± 0.60
0.007	± 0.00075	2 x 2113	49.6%	4.33 ± 0.39	4.14 ± 0.41
0.008	± 0.00075	1 x 7628	44.4%	4.49 ± 0.44	4.32 ± 0.47
0.008	± 0.00075	2 x 2116	43.0%	4.54 ± 0.46	4.37 ± 0.49
0.008	± 0.00075	1 x 2116 + 1 x 2113	48.6%	4.36 ± 0.38	4.18 ± 0.40
0.008	± 0.00075	1 x 7629	42.6%	4.55 ± 0.47	4.38 ± 0.50
0.009	± 0.00075	2 x 2116	47.8%	4.38 ± 0.37	4.20 ± 0.39
0.010	± 0.001	2 x 2116	51.8%	4.26 ± 0.35	4.08 ± 0.37
0.010	± 0.001	1 x 7628 + 1 x 1080	45.0%	4.47 ± 0.44	4.29 ± 0.47
0.010	± 0.001	1 x 7635	47.5%	4.39 ± 0.41	4.21 ± 0.43
0.012	± 0.001	2 x 1080 + 1 x 7628	45.5%	4.46 ± 0.40	4.28 ± 0.43
0.014	± 0.001	2 x 7628	38.8%	4.69 ± 0.48	4.53 ± 0.51

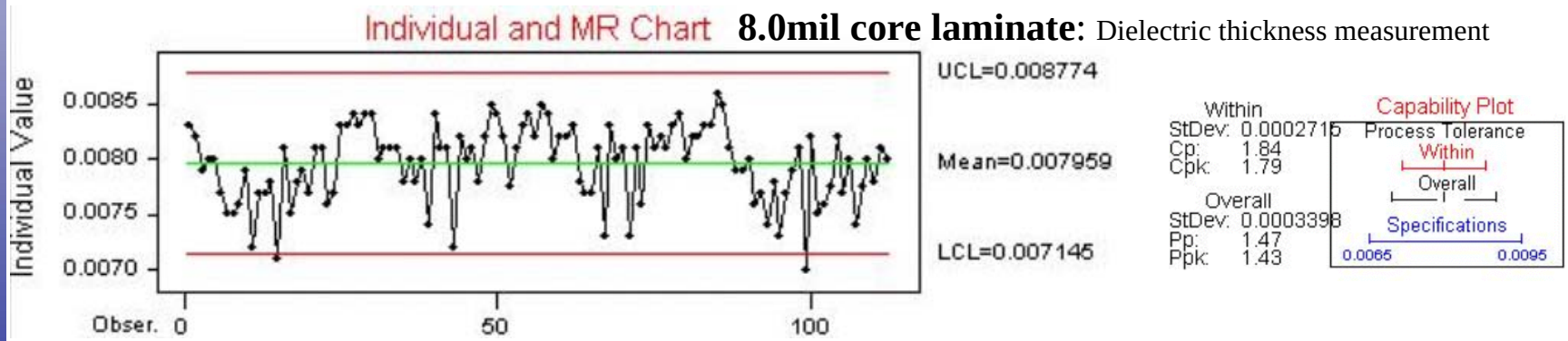
Courtesy of ParkNelco

Dielectric Thickness Variations in Laminate Cores

Sample Laminate Thickness data (ISOLA Laminates Jan2001)



3.2mil core laminate: Dielectric thickness measurement

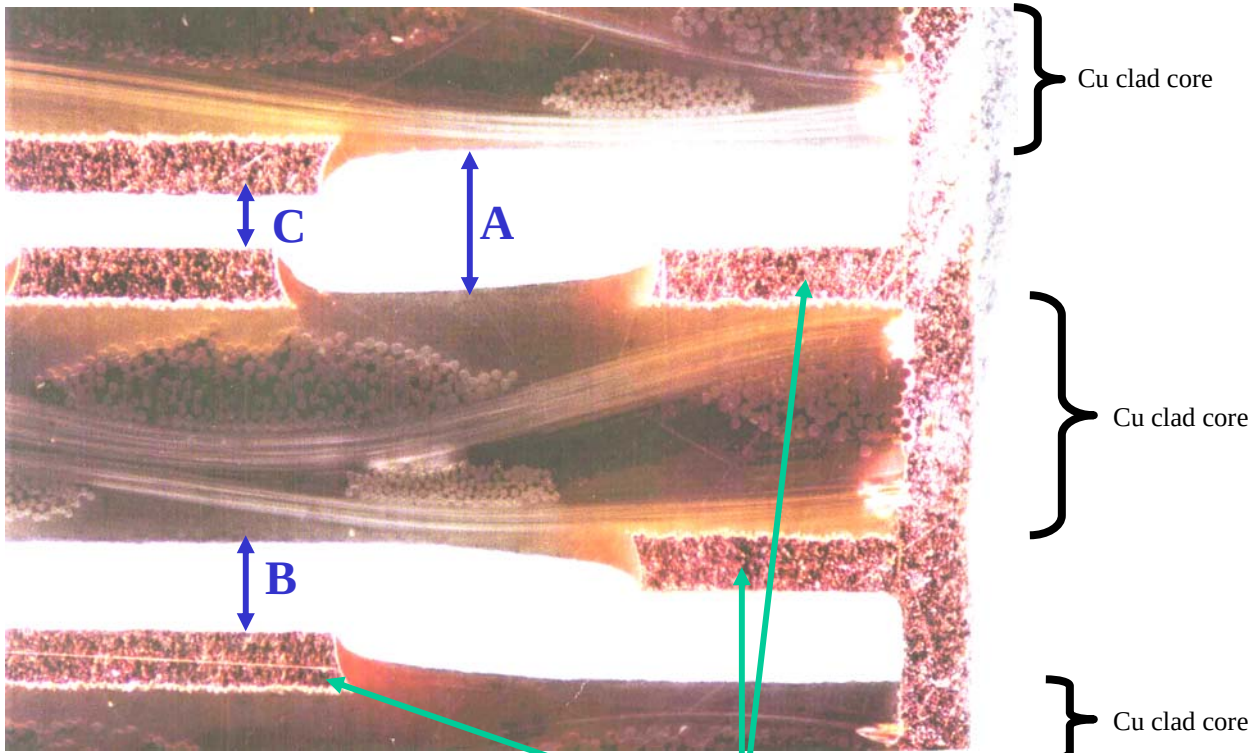


8.0mil core laminate: Dielectric thickness measurement

Designer Note: Laminate Suppliers holding published specification tolerances.

Dielectric Thickness Variations from Press Lamination

- Circuit features are pressed / embedded into softened resin of the prepreg material during lamination cycle.



Speedboard C (non-FR4) prepreg
(shows results from lamination clearer than FR4)

A: Prepreg thickness between two cores clear of Cu

B: Prepreg thickness between Cu feature are core clear of Cu

C: Prepreg thickness between two Cu features.

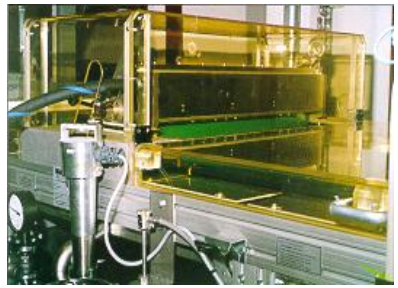
Dielectric Thickness

Key Modeling Points

- Dielectric Cores meet material supplier tolerances
- Prepreg / adhesive layer thickness
  - Wide supplier – supplier variations
  - Tolerance larger than for cores

Soldermask: Coating

- Liquid resists
  - Different application methods
    - Curtain coating
      - One side at time, requires baking/drying between each coat
      - Thickness uniformly good; but, trailing edge of cu feature/trace difficult to get full coverage
    - Spray systems
      - Same thickness issues of Curtain coating
      - Both sides can be coated at same time
    - Screening/Roller coating
      - Both sides can be coated at same time
      - Good coverage on all Cu feature/trace edges
      - Thicker resist or pooling along trace edges
  - Require tack back prior to image exposure
    - High emission release during drying/cure
- Dry film resists
  - Applied using hot roll lamination - same as etch resist films
  - Issue with conformance
  - Lower adhesion strength than most liquid resists

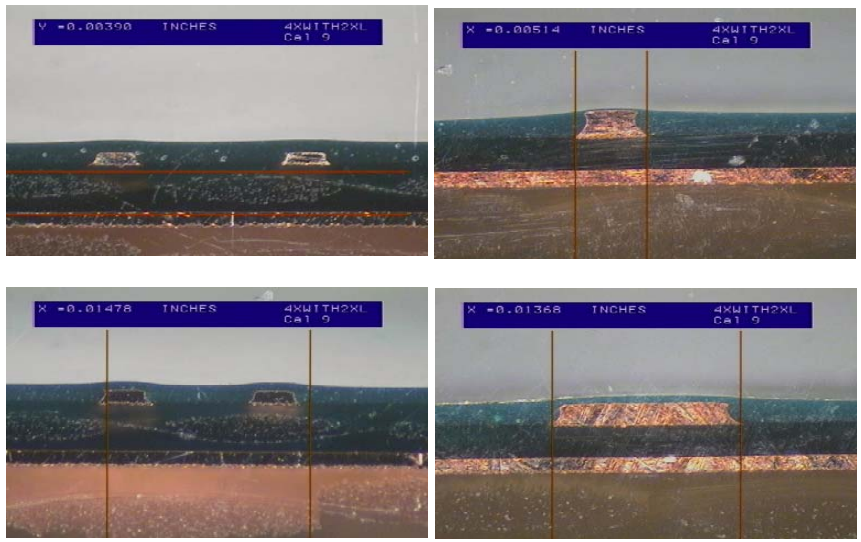


Curtain Coater

Screen/Roller Coater

Soldermask Thickness

- Over trace
  - As low as 0.1mil over narrow traces
  - Thickness slightly higher on higher traces by 0.1-0.2mils
  - As high as 1.3mil
- Over Laminate
  - Thickness approx. equal to thickness of trace for roller coat
  - Larger variation lot-lot and supplier-supplier on curtain coat



Soldermask Thickness

Key Modeling Points

- Thickness typically tracks trace thickness
- Soldermask over copper varies from 0.1 to 1.3 mils
  - Local variations dependent on plating thickness and warpage variations. (especially roller coat processes)

PCB Fabrication Tolerances

Line Widths

Line Defects

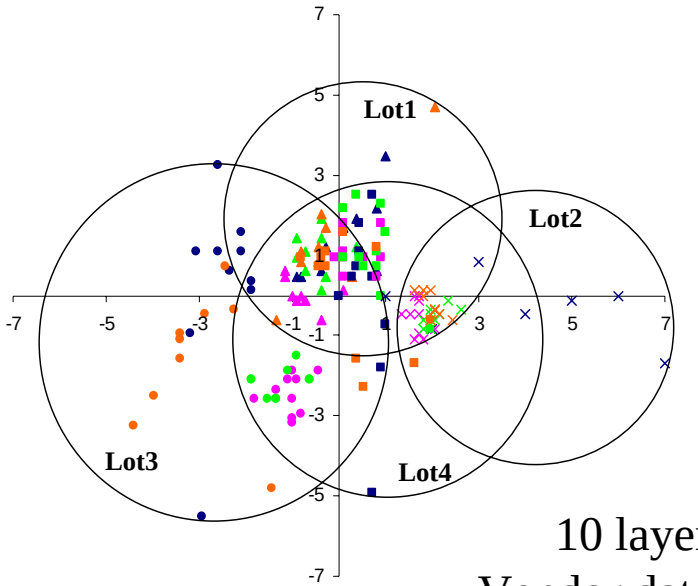
Trace Heights

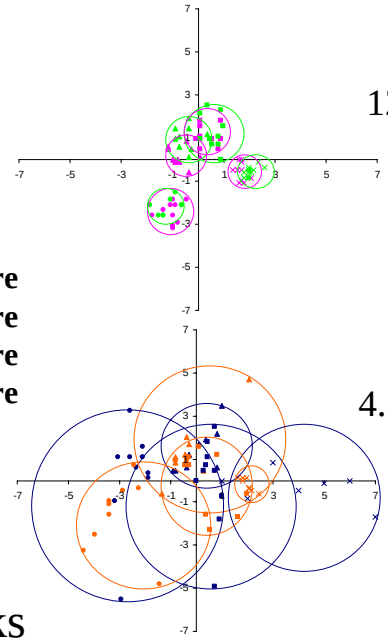
Material Thickness

Image Registration

Layer-Layer Registration

- Pad stack registration
  - Typically more movement variance with thinner cores
  - Dependent on Lamination cycle and tooling system
  - Dependent on retained Cu and nearest prepreg styles.





12mil cores

4.5mil cores

10 layer brd (4lots)
Vendor data across 6weeks

Layer-Layer Registration
Key Modeling Points

- Layer to layer
  - Across an innerlayer core <+/- 1.0 -2.0mils
  - Across prepreg +/-4.0-6.0 mils
- Variation has a shift, scaling, and rotation component
  - Minimized at center of fabrication panel
  - Maximized at edges of fabrication panel
- Broadside Differential pairs should be routed across innerlayer cores whenever possible.

PCB Impedance

Microstrip

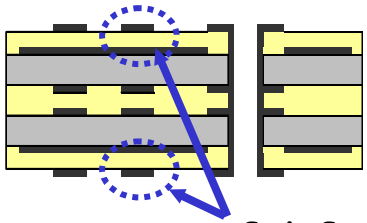
Stripline

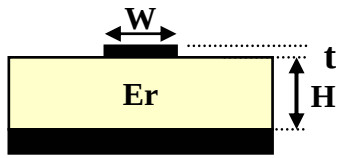
Edge-Coupled Differential

Broadside Coupled Differential

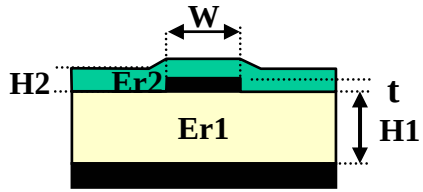
Design Considerations

uStrip Structures





Conventional microStrip



Embedded microStrip

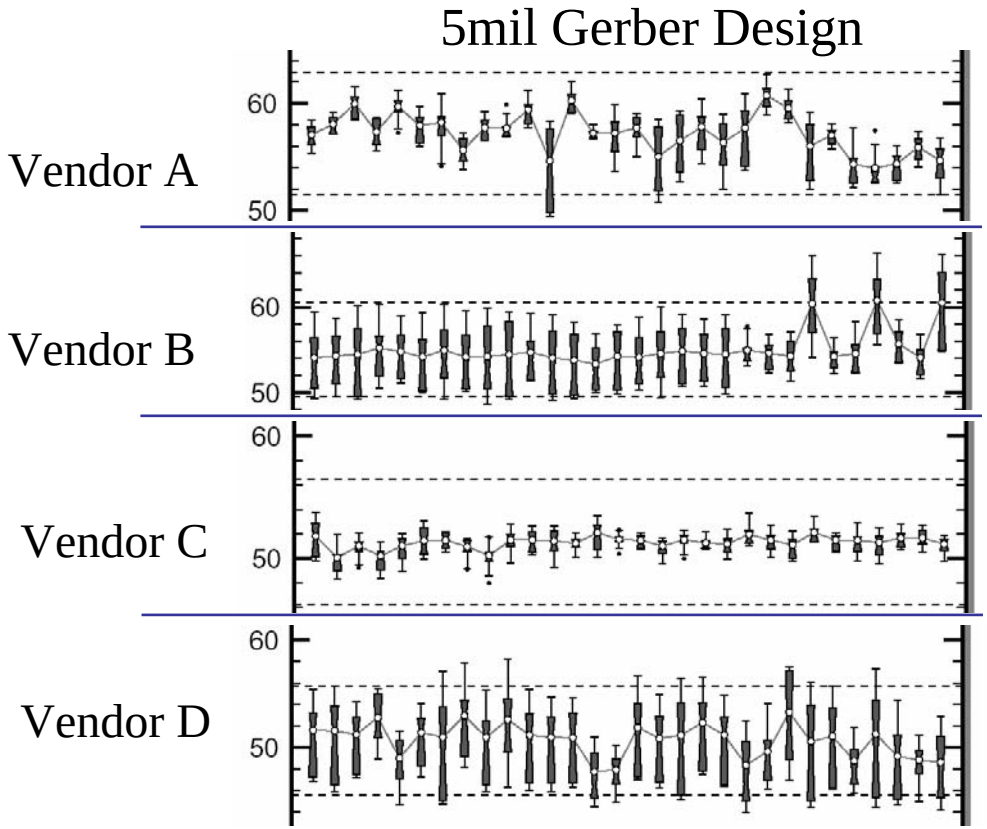
(Typical model with second dielectric as soldermask)

- Dielectric between trace and ground is typically 1 or 2 plys of laminated prepreg.
- uStrip affected by following fabrication processes
  - Material
    - resin control (Er)
    - Glass & resin control (dielectric thickness)
  - Lamination (dielectric thickness)
  - Plating thickness (conductor height)
  - Outerlayer imaging (conductor width)
  - Strip Etch Strip (conductor width)
  - Soldermask (soldermask thickness)

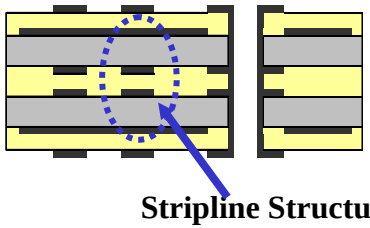
uStrip Tolerances: Measured Data

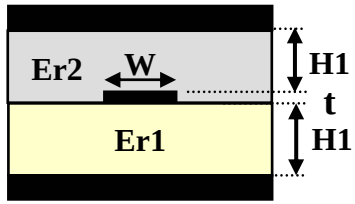
- Most vendors capable of +/-(8 to 10)% within lot
- Lot to Lot variation will add 2-5%

Controlling target by stackup and Gerber only will result in additional +/-10% difference between suppliers

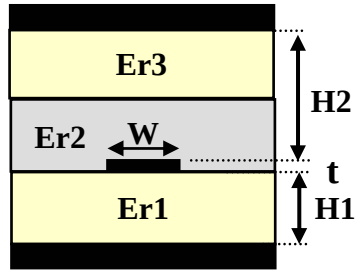


Stripline Structures





Centered Stripline



Offset Stripline

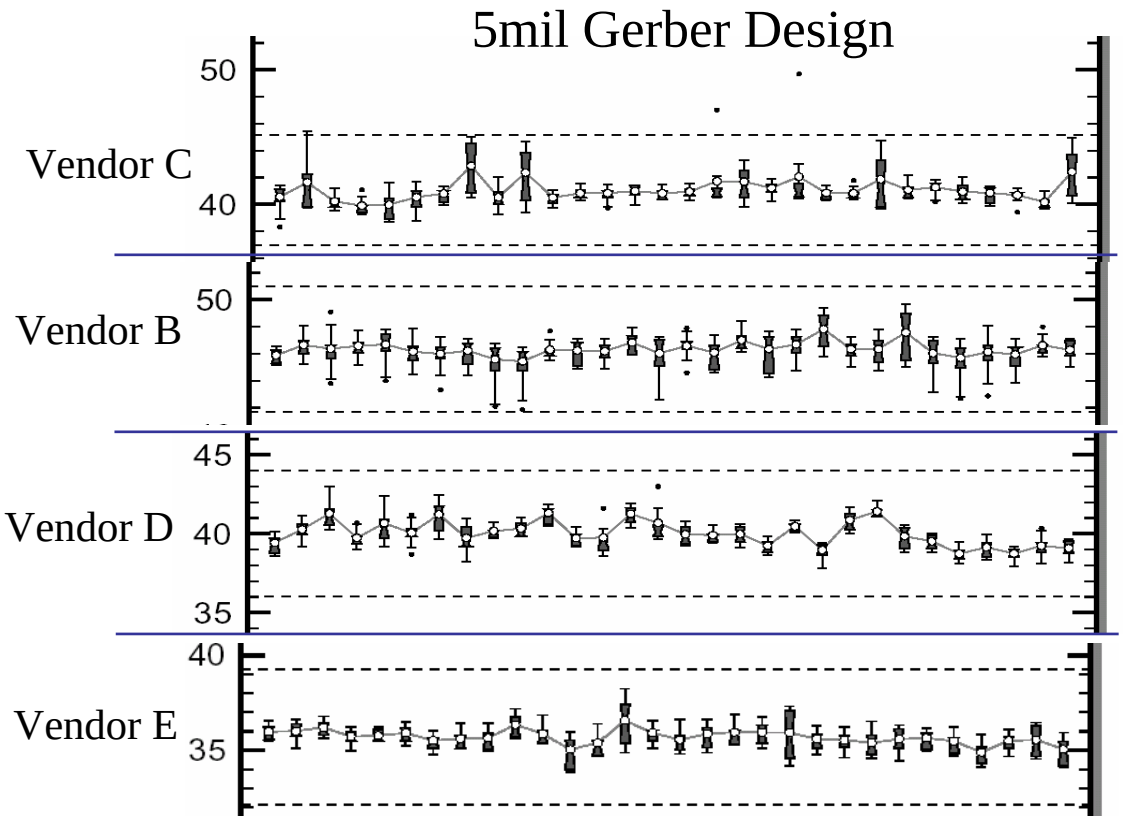
- Centered stripline typically is built using a core and a prepreg opening
- Offset stripline will typically consist of either 2 cores and a prepreg opening or 1 core and 2 prepreg openings.
- Stripline affected by following fabrication processes
  - Material selection
    - resin control (Er)
    - Glass & resin control (dielectric thickness)
  - Lamination (dielectric thickness)
  - Innerlayer imaging (conductor width)
  - Develop Etch Strip (conductor width)
  - Oxide process (conductor height)

Stripline Tolerances: Measured Data

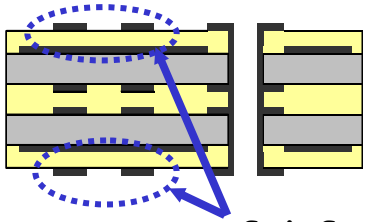
- Most vendors capable of +/-(5 to 8)% within lot
- Lot to Lot variation will add 2-5%

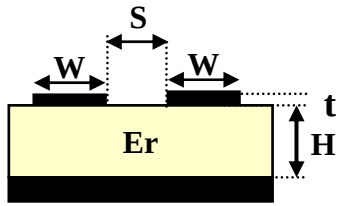
5mil Stripline yielded low
Zo based on stackup design

2-3mil
4-5mil

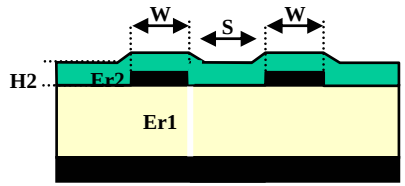


Differential uStrip Structures





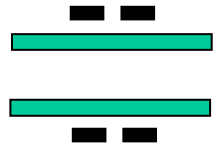
Conventional
Differential microStrip



Embedded
(Typical model with second dielectric as soldermask)

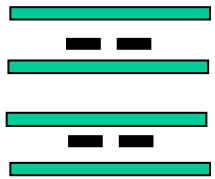
- Structure very close in fabrication as uStrip
- Additional sensitivity to parameters
  - Trace Spacing
  - Trace Height (Plating)
  - Soldermask affect on effective Er
- Center to center spacing of traces remain fixed
  - Trace + Space = constant
- Plating height variation very very significant in tolerance control

Measured Capability



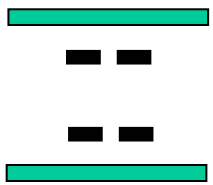
uStrip +/- 18-24%

	Ave	Max
Lot variation	+/- 13.5 ohm	+/- 17.1 ohm
Lot-Lot (mean shift)	+/- 1.0 ohm	+/- 1.0 ohm
Measurement Correlation(1)	+/- 0.7 ohm	+/- 2.6 ohm
Lot mean to target mean	+/- 3.0 ohm (est)	



Stripline +/-11-16%

	Ave	Max
Lot variation	+/- 7.5 ohm	+/- 11.0 ohm
Lot-Lot (mean shift)	+/- 0.7 ohm	+/- 0.7 ohm
Measurement Correlation (1)	+/- 0.7 ohm	+/- 2.6 ohm
Lot mean to target mean	+/- 2.0 ohm (est)	



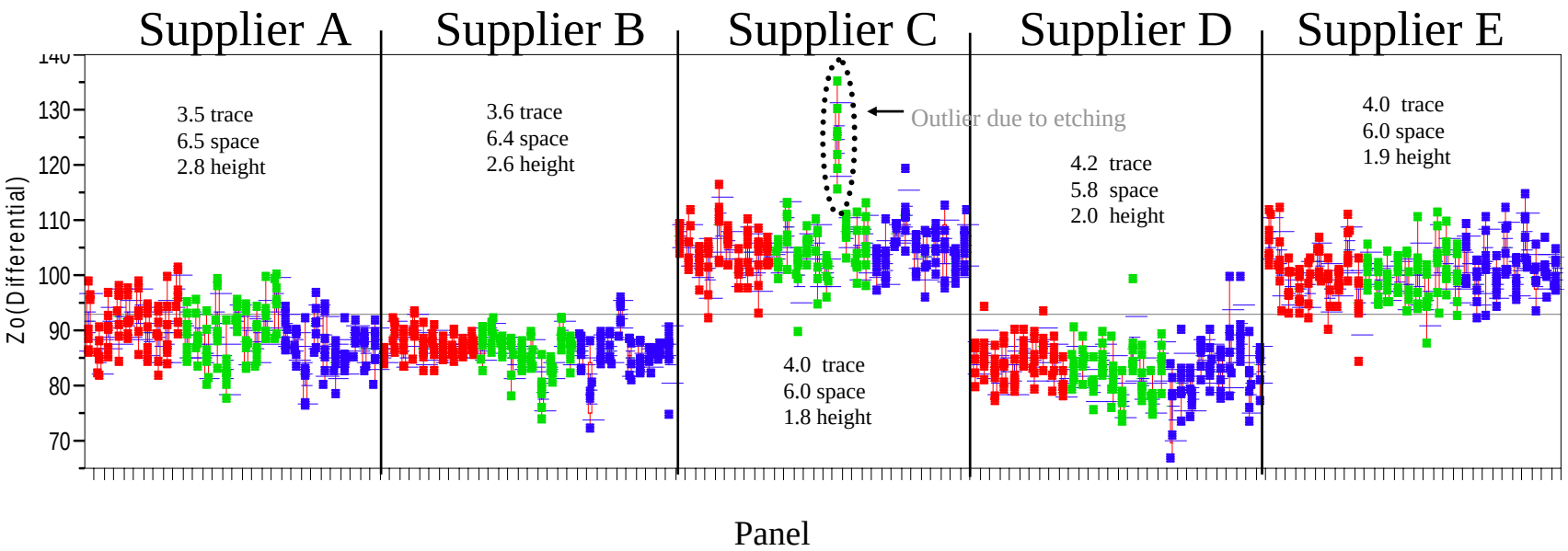
Offset Stripline +/- 9.5-16

	Ave	Max
Lot variation	+/- 6.0 ohm	+/- 11.0 ohm
Lot-Lot (mean shift)	+/- 0.7 ohm	+/- 0.7 ohm
Measurement Correlation (1)	+/- 0.7 ohm	+/- 2.6 ohm
Lot mean to target mean	+/- 2.0 ohm (est)	

Lot variations based on +/-3sigma

(1) Measurement offset including repeatability and correlation variance

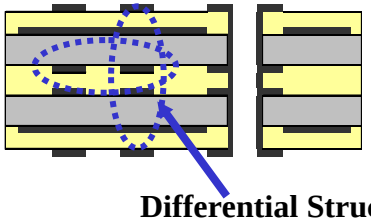
uStrip by Vendor and Fabrication Lot

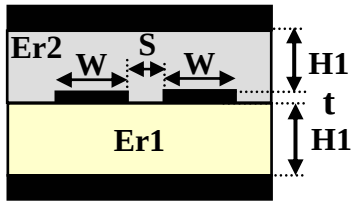


Data on fixed design, supplier's were not allowed to center Zo

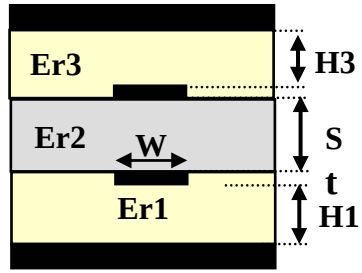
- Notes:
  - Within Board variation is bulk of lot variation
  - Lot to Lot variations fairly small.
  - Within Lot variations across all suppliers
    - Minimum 3.5sigma
    - Average 4.5sigma
    - Max 5.7sigma

Differential Stripline Structures





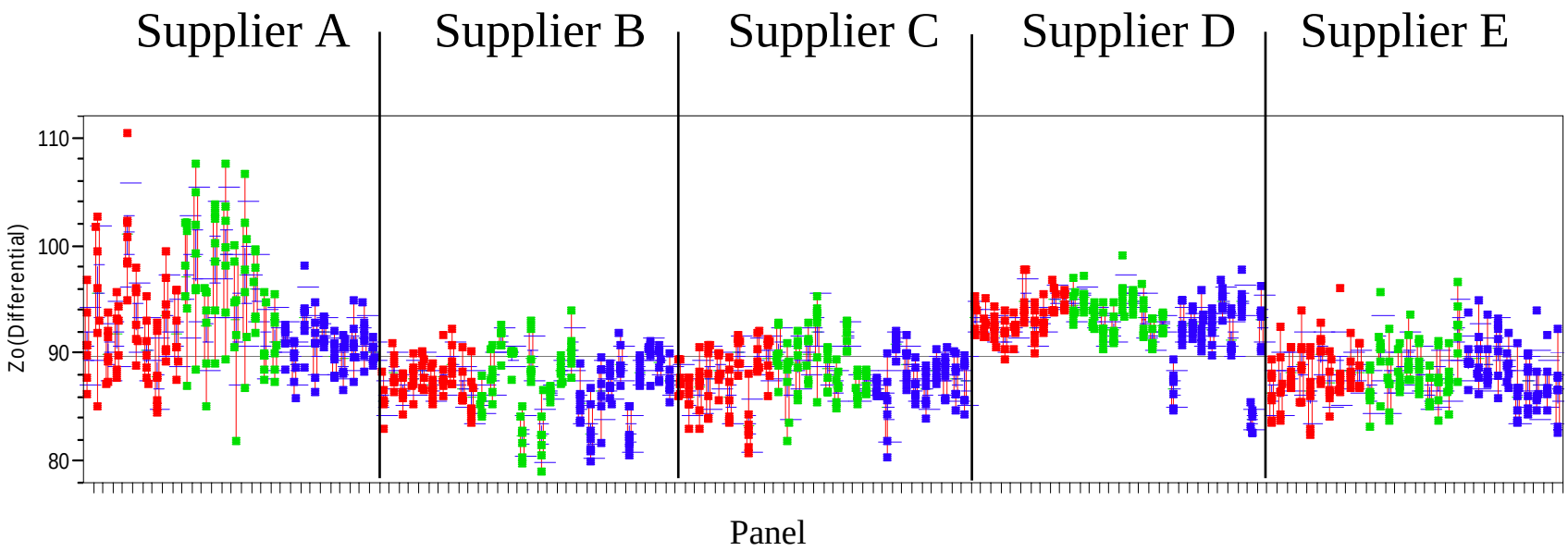
Edge Coupled



Broadside

- Structures resemble stripline and offset stripline structures
- Additional sensitivity to parameters
  - Lamination or Core thickness (Spacing between conductors)
  - Registration
    - Front-Back imaging across core
    - OR Material movement during lamination
- Placing traces across core minimizes spacing variation and registration variation.
  - Never couple broadside differential signals across prepreg.
  - Thickness variation of core controlled by laminate material supplier not PCB fabricator

Centered Stripline by Vendor and Fabrication Lot

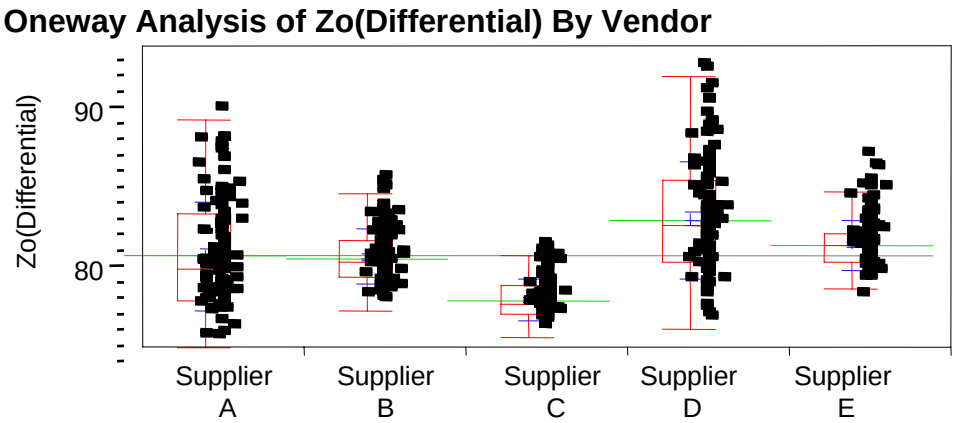


Data on fixed design, supplier's were not allowed to center Zo

- Notes:
  - Within Board variation is bulk of lot variation
  - Lot to Lot variations fairly small.
  - Two lots from one supplier definitely out compared to all other lots.
  - Innerlayer Copper foil very tightly controlled compared to plated Copper.

Differential Broadside Stripline Tolerances

- Suppliers at +/-5-11% tolerance
- Data only for pairs across an internal core
  - Layer-layer registration constrained to +/-2mil
  - Thickness controlled by core



Means and Std Deviations

Level	Number	Mean	Std Dev	Std Err Mean
Supplier A	89	80.6712	3.40571	0.36100
Supplier B	89	80.5391	1.73302	0.18370
Supplier C	90	77.9021	1.28091	0.13502
Supplier D	90	82.9682	3.69469	0.38945
Supplier E	90	81.3433	1.60366	0.16904

Data include layer-layer misregistration of +/-2mils

Note: Diff Zo targets not specified on print. Diff Zo was controlled via stack-up specification

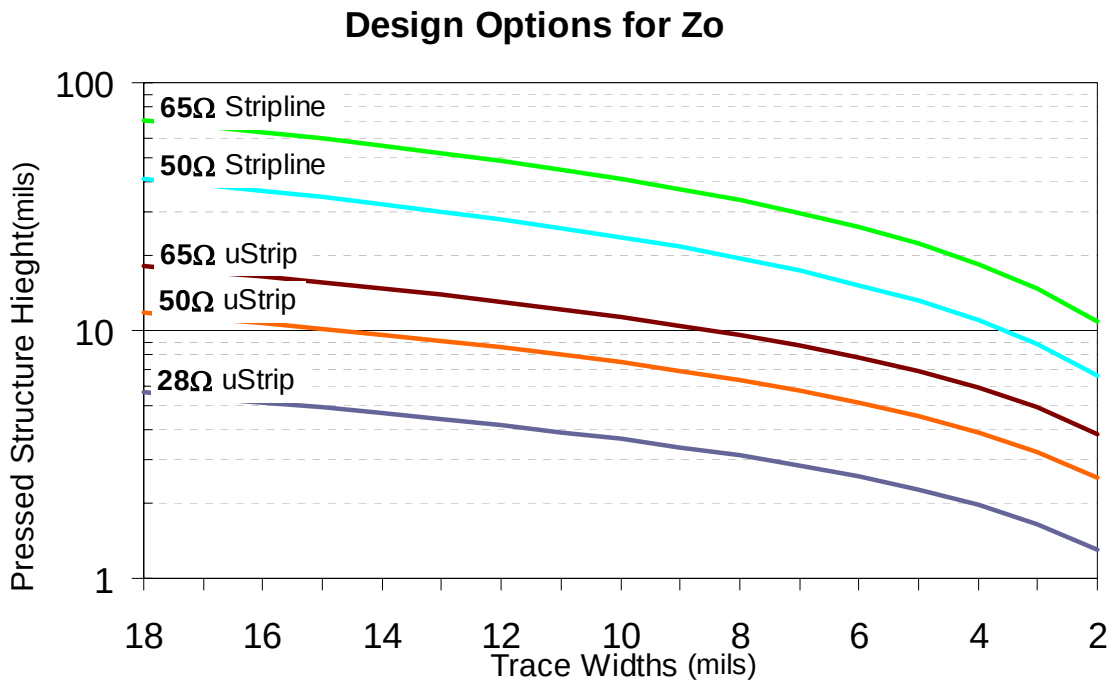
Design Considerations

- Impedance Control is influenced by the design
  - Wider lines imply thicker dielectrics and tighter overall control
  - Stripline typically have better impedance control than ustrip designs for a given trace width

- Impedance not only criteria when selecting line width
  - Multiple Zo targets on same layer
  - Line width capability of supplier
  - Managing packaging routing and layer count

Design Considerations

- Trace width and dielectric height combination selected to meet multiple criteria
  - Routing requirements
  - Required layers and total thickness requirements
  - Ability to route multiple nominal Zo's on single layer



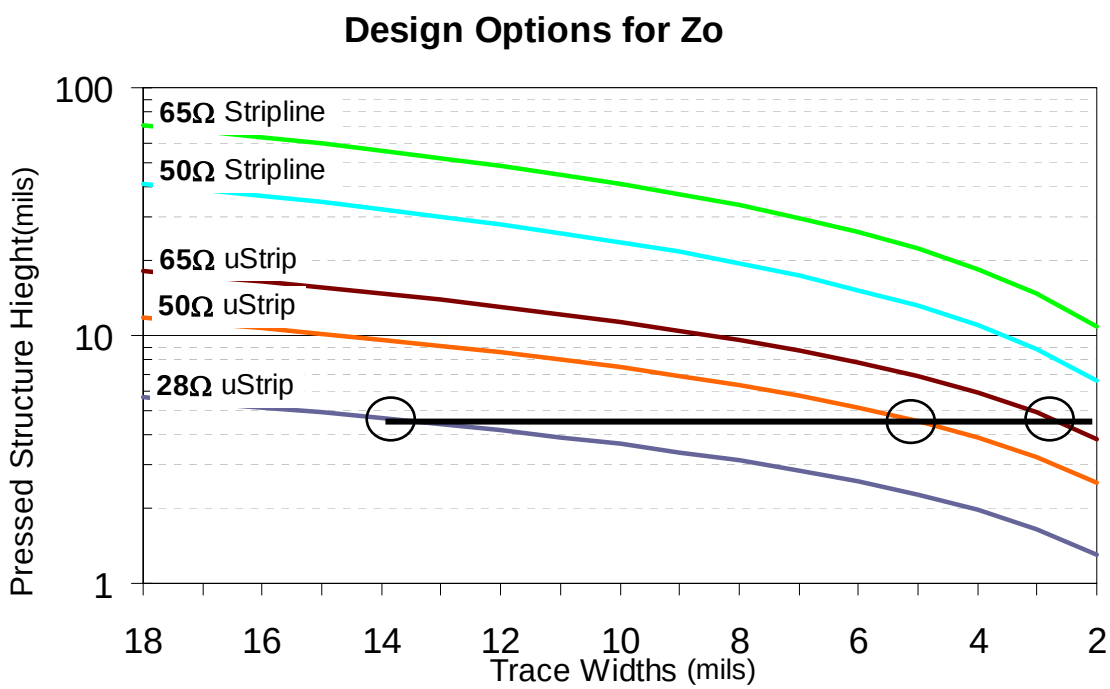
Design Considerations

High and Low Zo (example 28ohm and 65ohm) not always practical on same layer.

Example: A Desktop ustrip design using Rambus design

Rambus traces 14mils

Layer 1 to Layer 2 dielectric spacing ~4.2 mils

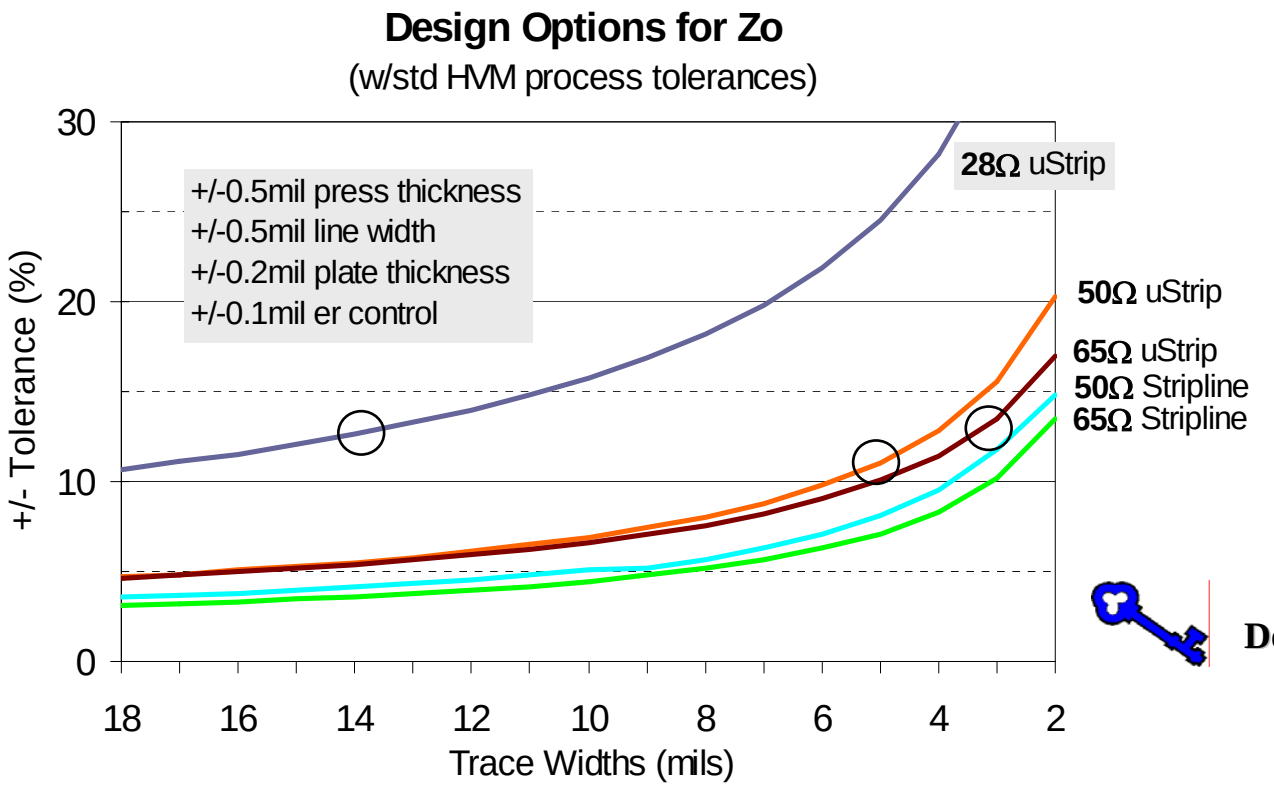


50ohm (5-5.25mil trace) could be designed on same layer

65ohm (2.75-3.33mil trace) would violate most HVM capability

Design Consideration

- PCB Supplier's ability to maintain a (+/-%) Zo tolerance varies with Zo design.

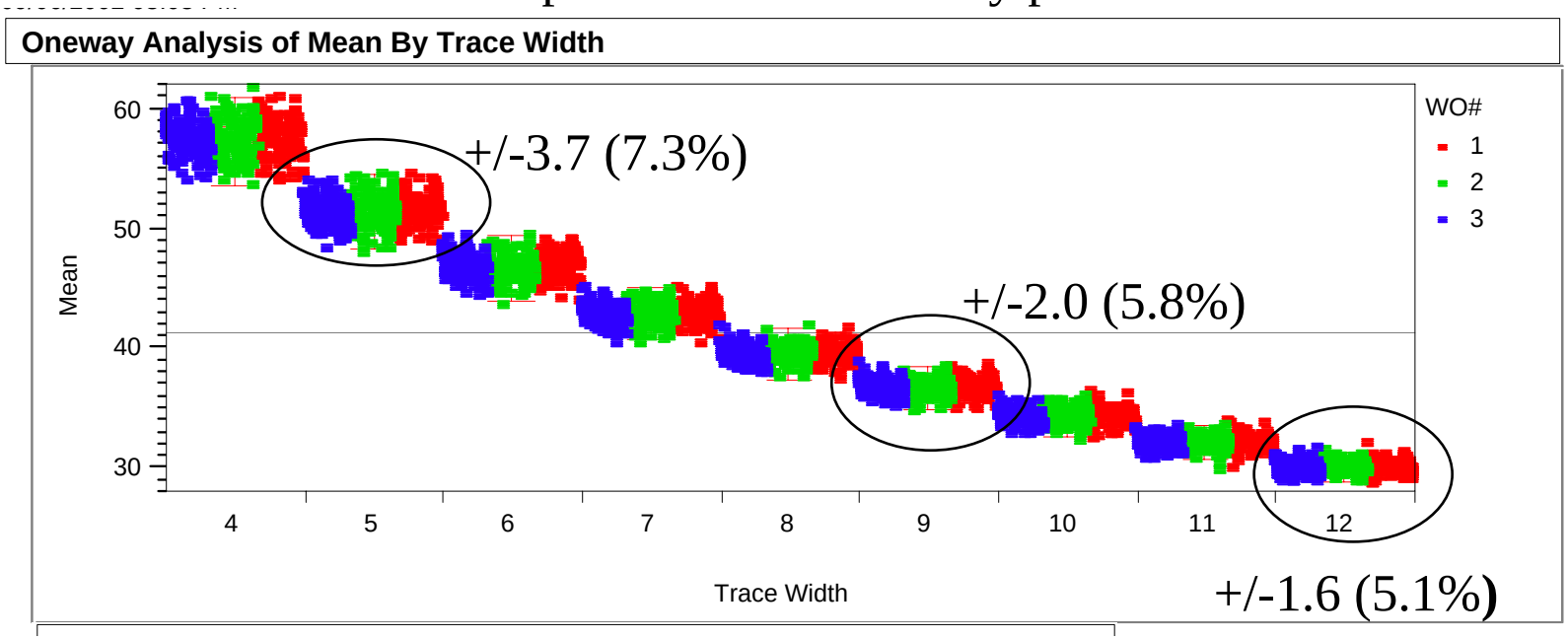


Designer Note: Stripline structures tighter tolerance.

Design Consideration

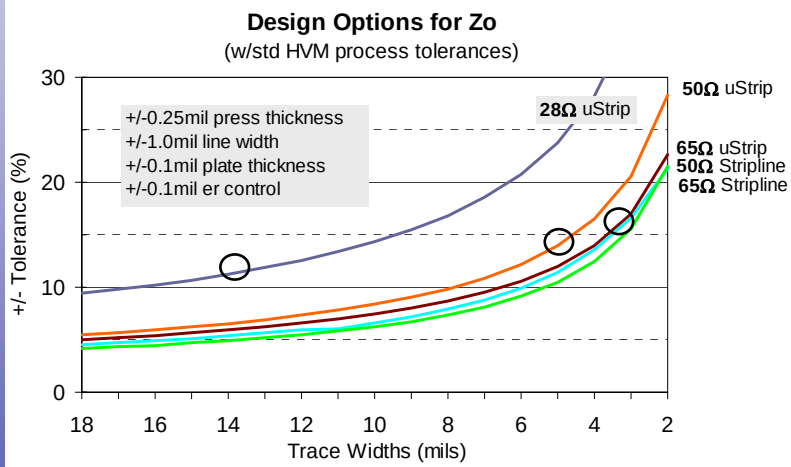
- Tolerance Comparison of uStrip with 1080 prepreg
- Wider lines => lower impedance and lower tolerance

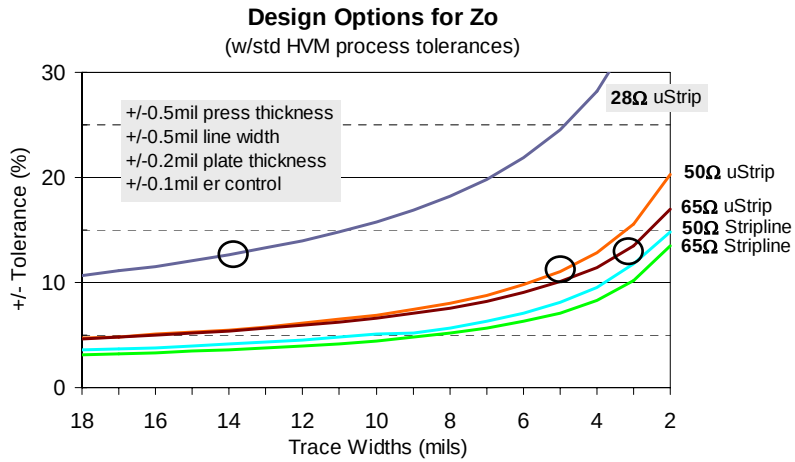
uStrip Test Board Data: By panel and lot



Design Consideration

- PCB Supplier's ability to maintain process control will also affect overall Zo tolerance.





Designer Note: Different Fabricator capability will also translate into which Zo target will have the most variation on an individual layer

PCB Materials

Copper

Surface Finishes

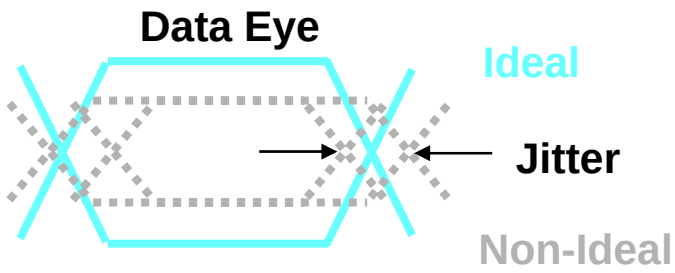
Dielectric Materials

Spatial Properties

PCB Material Impacts

Transmission line loss

- Losses
  - Accurate HVM loss prediction is essential
    - Requires an understanding of both conductor and dielectric loss contributions as a function of frequency.



Accurate loss prediction is important to estimate bus performance

PCB Materials

Copper

Surface Finishes

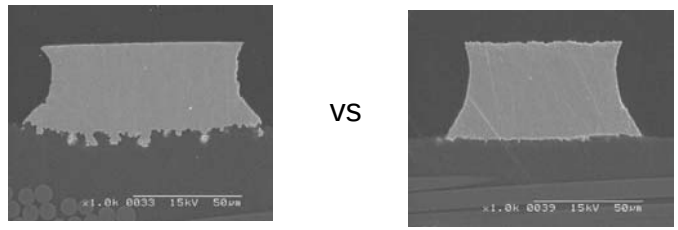
Dielectric Materials

Spatial Properties

PCB Material

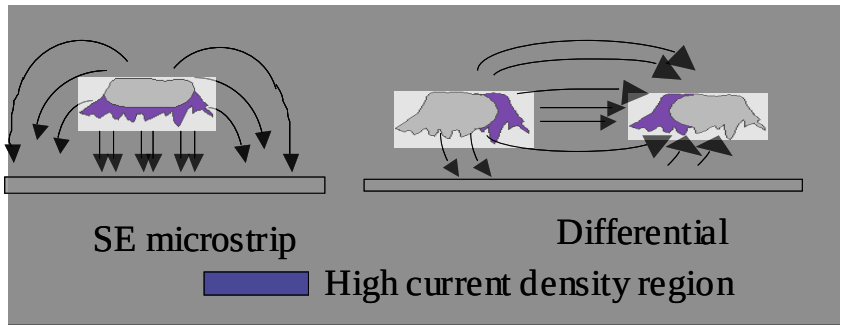
Copper Foil and Metallization

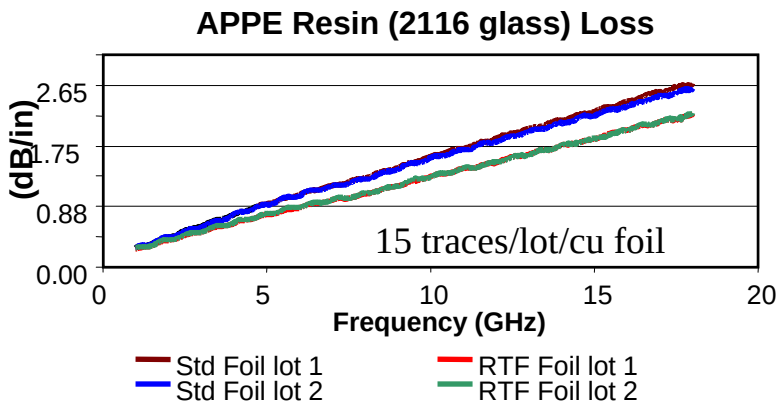
- Cu roughness significant contributor
  - Cu tooth
  - Oxide/Oxide Alternative surface prep
- Surface finish characterization
  - Higher Impact on Differential Designs



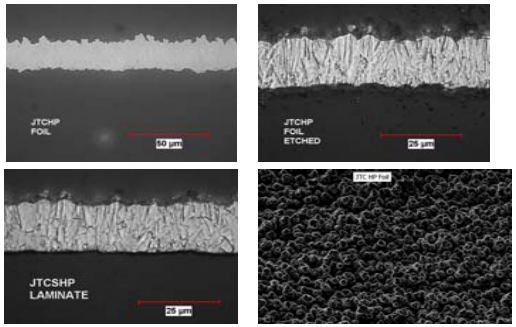
vs

RTF vs Std => 0.3dB/in on uStrip @10GHz

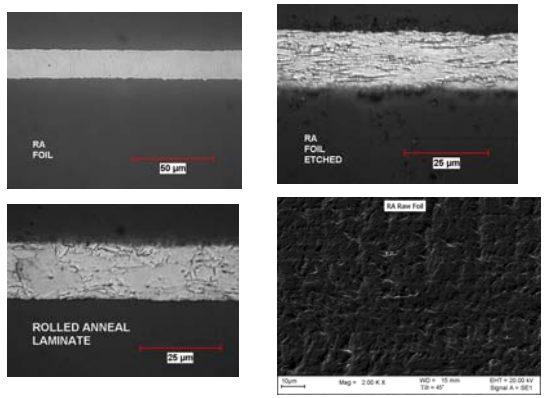




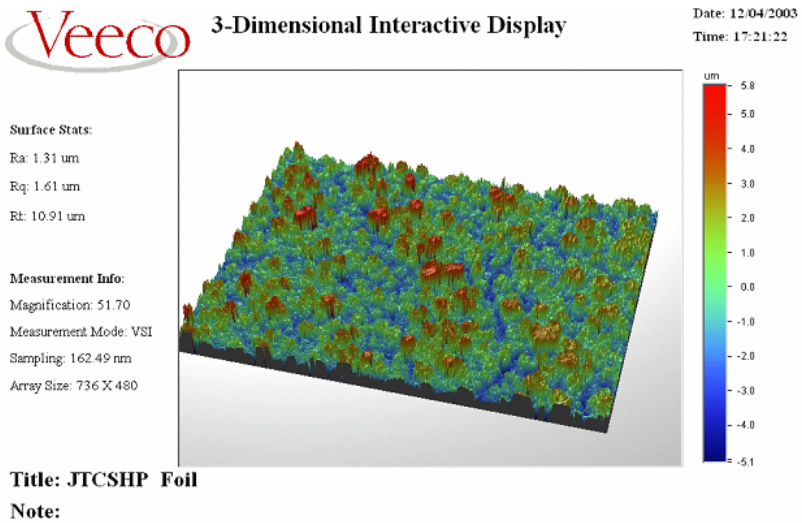
PCB Materials: Copper Foil Types

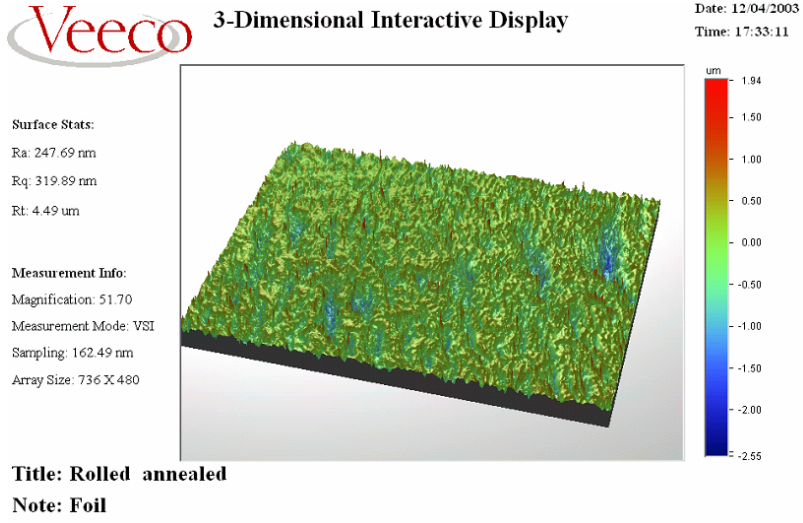


JTCSHP:
High Profile, Heavy Nodule Bond Treatment
Profilometer Roughness R_a 0.75 µm, R_{tm} 6.3 µm

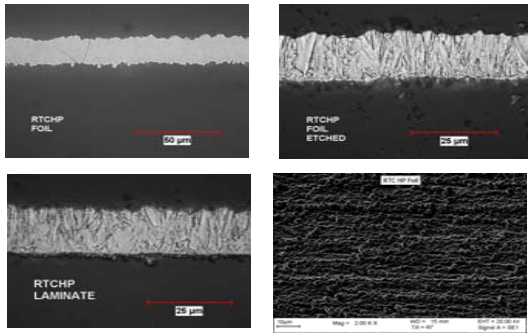


Rolled Copper Foil:
Without nodular bond treatment
Profilometer Roughness R_a 0.39 µm, R_{tm} 3.2 µm

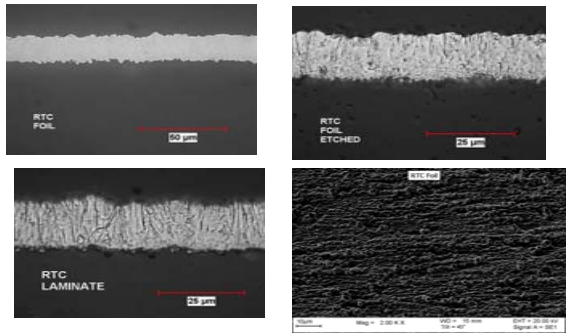




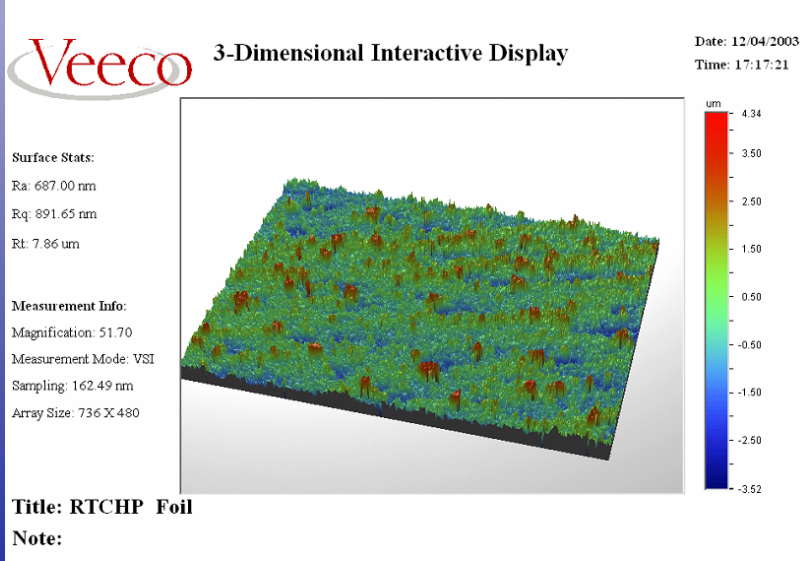
PCB Materials: Copper Foil Types

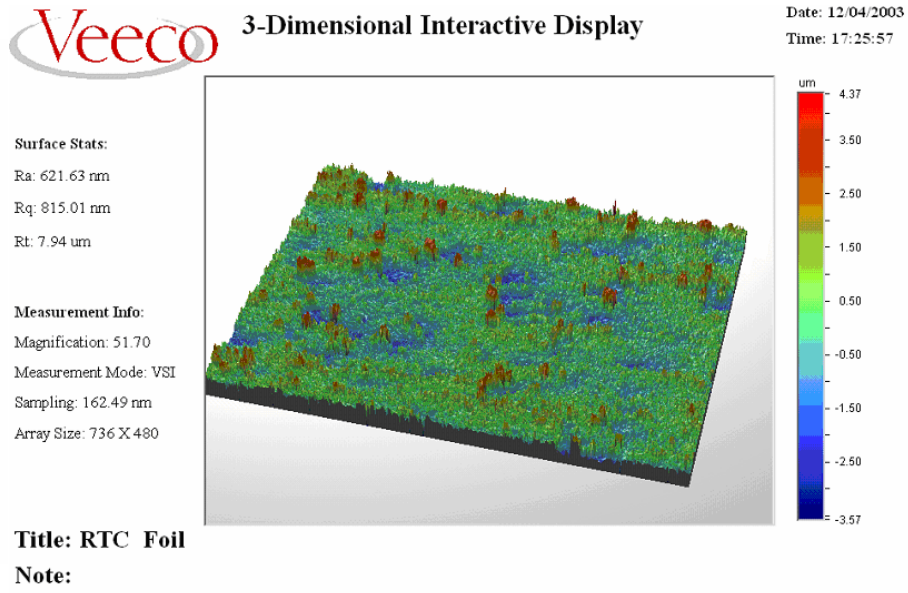


RTCHP:
Shiny side heavy nodule bond treatment
Profilometer Roughness R_a 0.60 µm R_{tm} 5.1 µm

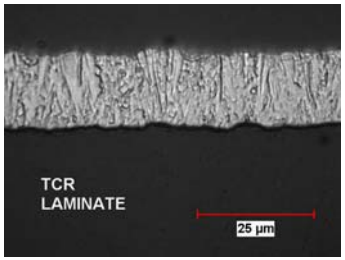


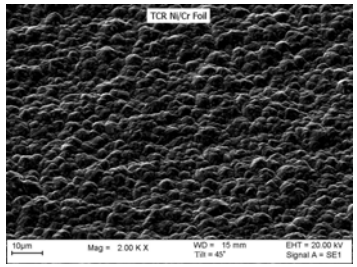
RTC:
Shiny side nodule treated foil.
Profilometer Roughness R_a 0.45 µm, R_{tm} 3.6 µm





PCB Materials: Copper Foil Types

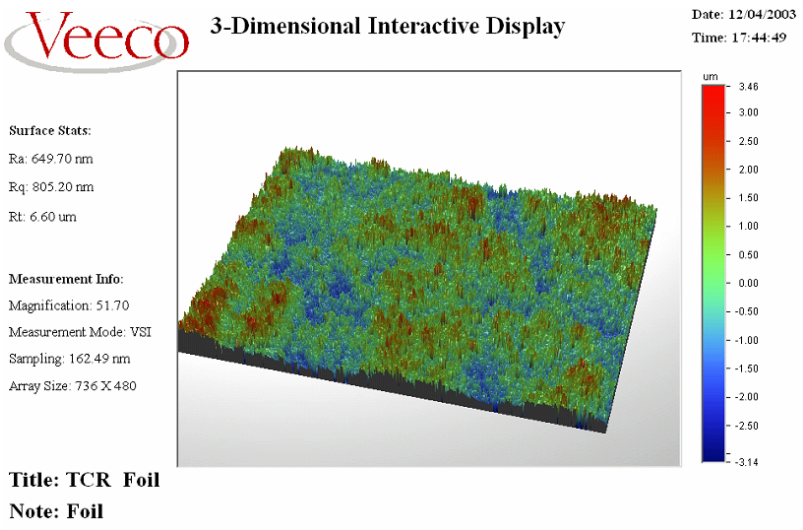


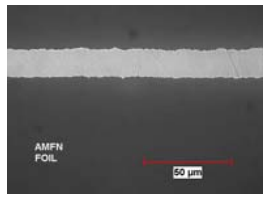


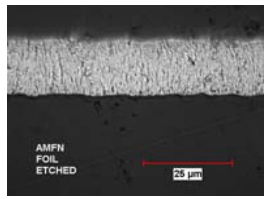
TCR:

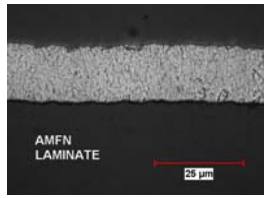
Resistor layer on matte profile with no nodule bond treatment

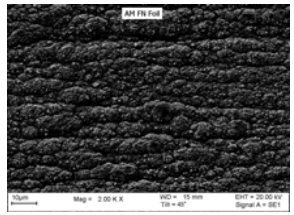
Profilometer Roughness R_a 0.50 µm, R_{tm} 4.5 µm











AMFN:

Very low profile foil, fine nodule bond treatment

Profilometer Roughness R_a 0.48 µm, R_{tm} 3.8 µm

PCB Materials: Copper Foil

- Physical Summary of Copper foil types

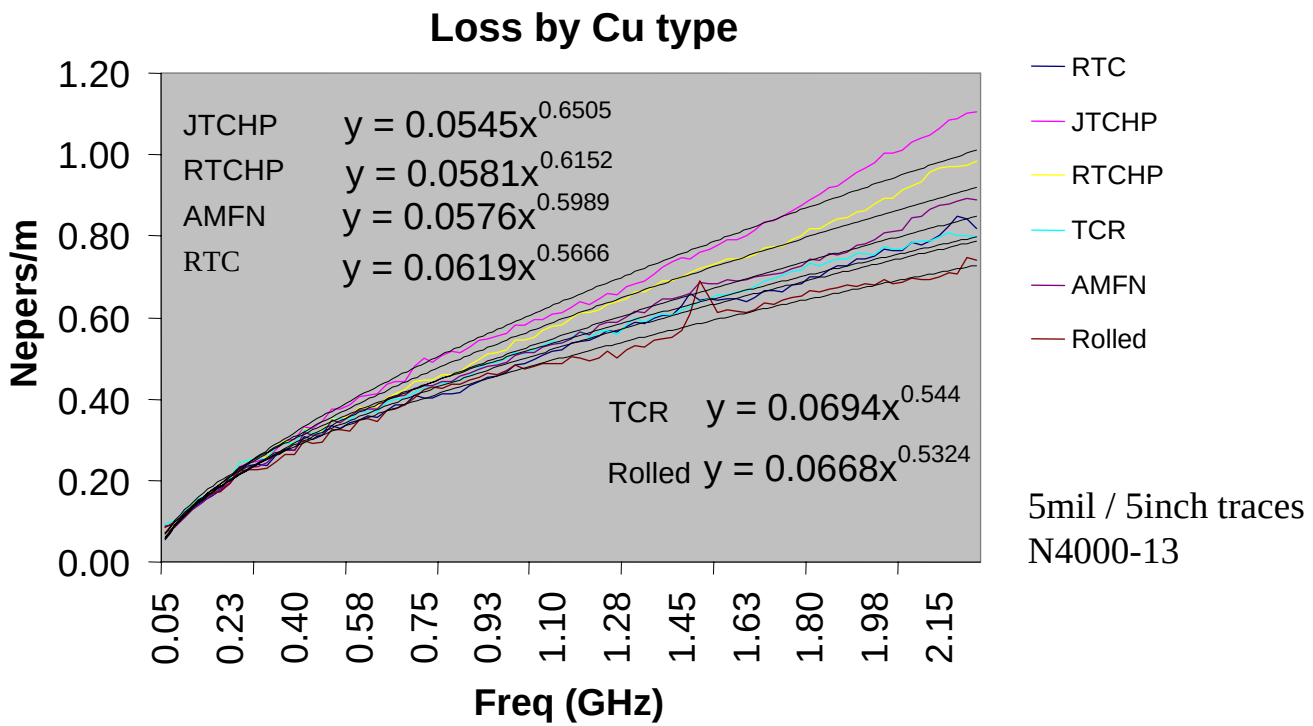
Sample	Resistance (uOhms-cm)	Conductance (Mhos/m)	Ra(Veeco) Rms nm	Ra (mech) Rms nm	Rt Peak-Peak (um)
JTCHP	1.88	53200000	1310	750	10.9
RTCHP	1.85	54050000	687	450	7.9
AMFN	1.90	52630000	n/a	480	n/a
RTC	1.82	55250000	621	600	7.9
TCR	1.76	56820000	650	500	6.6
Rolled	1.71	58480000	248	390	4.5

Gould coppers

Notes: AMFN is an oxide enhanced foil for improved adhesion
TCR has ultra thin Ni-Cr layer for embedded resistor applications

PCB Materials: Cu Foil Comparison : 0-2GHz

- Copper foil type will affect low frequency response



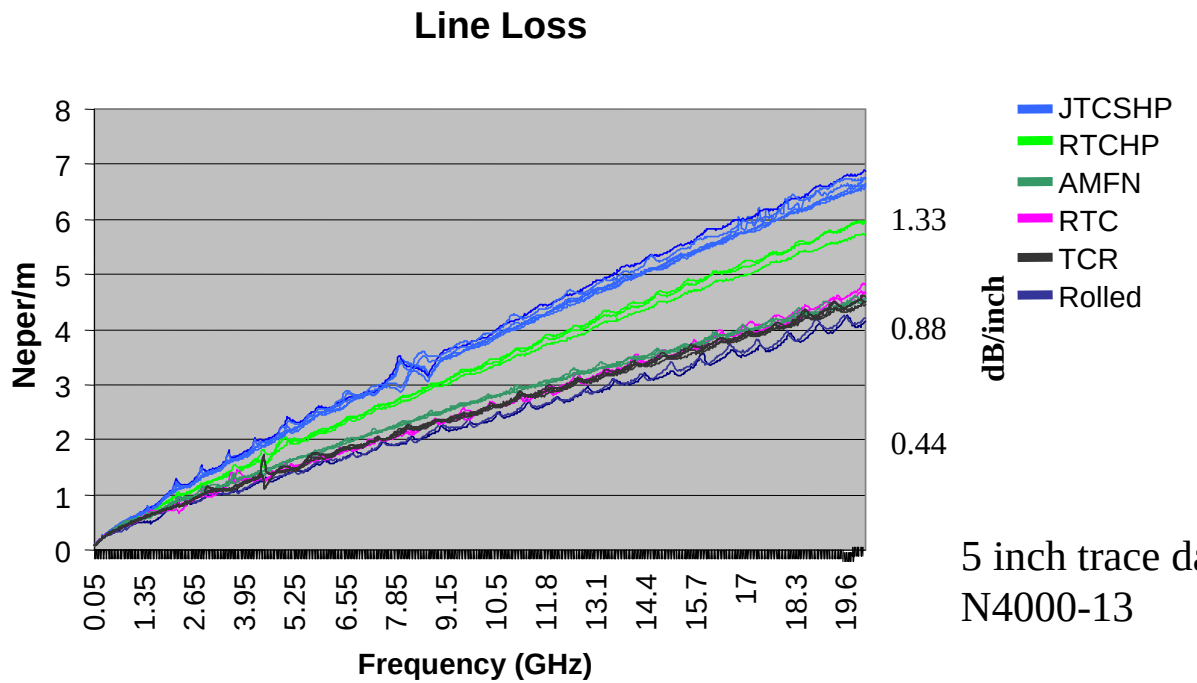
5mil / 5inch traces
N4000-13

Roughness will affect low frequency curve fit power factor

PCB Materials: Cu Foil Comparison : 0-20GHz

• Difference in loss between copper types approximately linear with frequency.

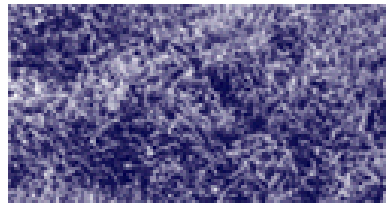
Low Profile RTC behaved close to Rolled



5 inch trace data
N4000-13

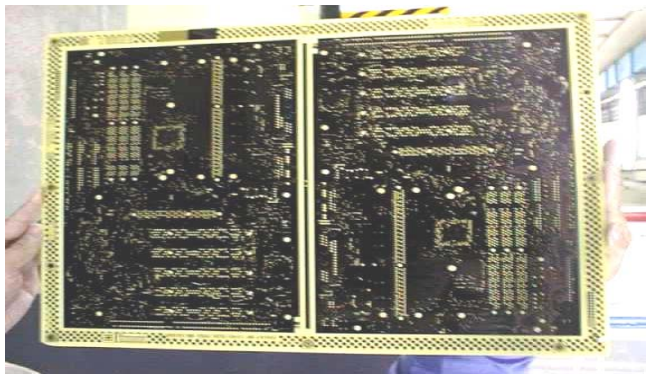
PCB Materials: Copper Oxide/Oxide Alternatives

- Prepare the copper surface for enhancing adhesion strength with prepreg.
- Several types of processes
  - Most widely used is Brown or Black oxide
  - Oxide replacement processes gaining acceptance
    - Typically a grain boundary etch to roughen Cu foil
    - Faster process time lend to use of horizontal conveyor equipment

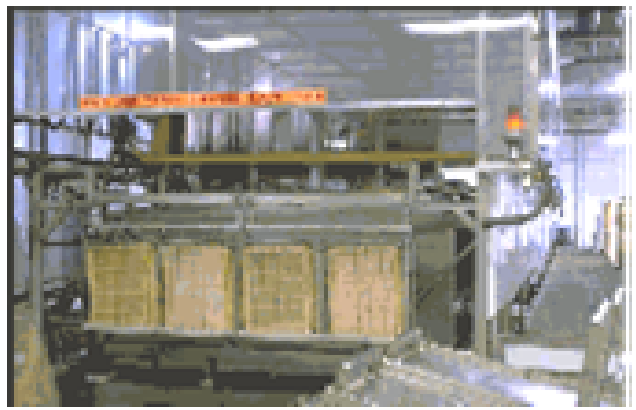


Black oxide crystal structure

- Most PCB shops apply Post Dip treatment (proprietary chemical) to eliminate pink ring defect.



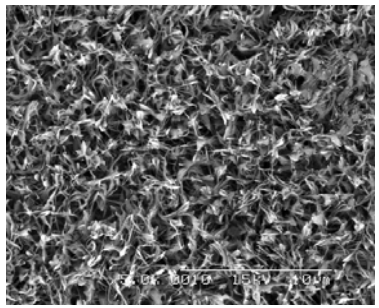
Black oxide panel after processing

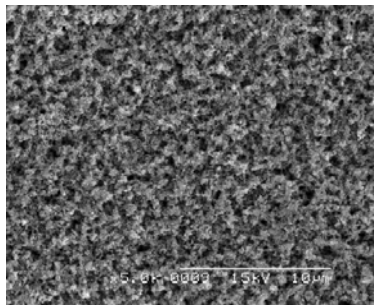


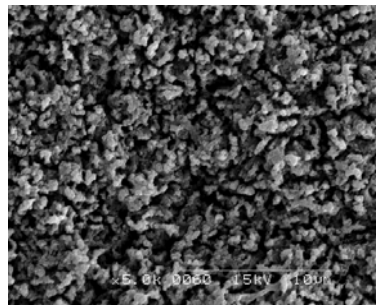
Vertical lines utilize baskets to
Process in an automated batch mode

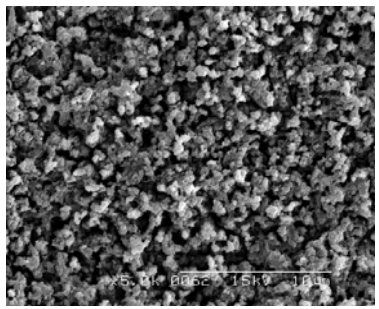
PCB Materials: Copper Oxide/Oxide Alternatives

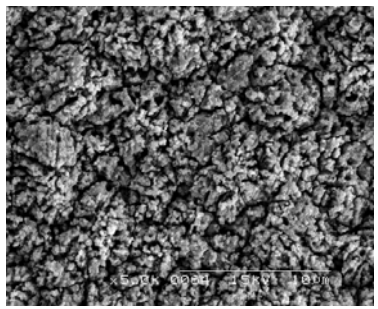
- **Process Comparisons (SEM)**

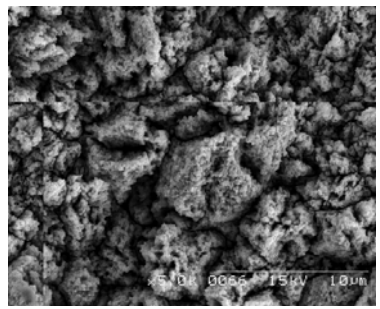

Black Oxide at x5K


Oxide Dissolution at x5K


Oxide Alternative at x5K
(Standard Process)


Oxide Alternative at x5K
(Standard Process + 1 Rework)


Low-Etch Oxide Alternative at x5K
(Standard Process)

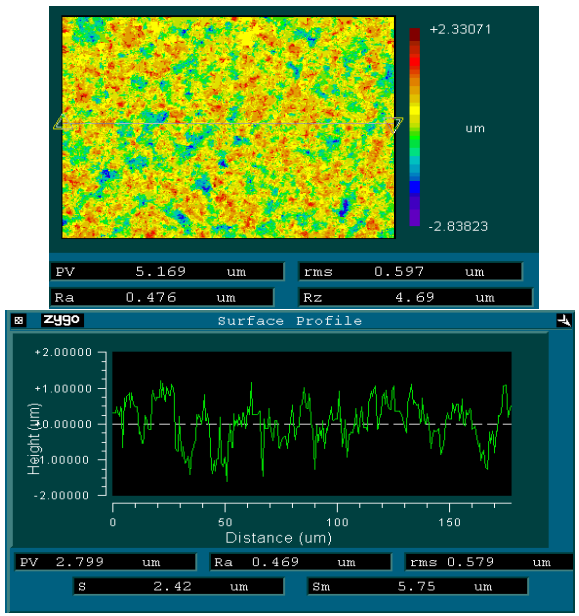

Low-Etch Oxide Alternative at x5K
(Standard Process + 2 Reworks)

Note: Black Oxide and Oxide Dissolution surface after rework identical to initial first pass surface topology

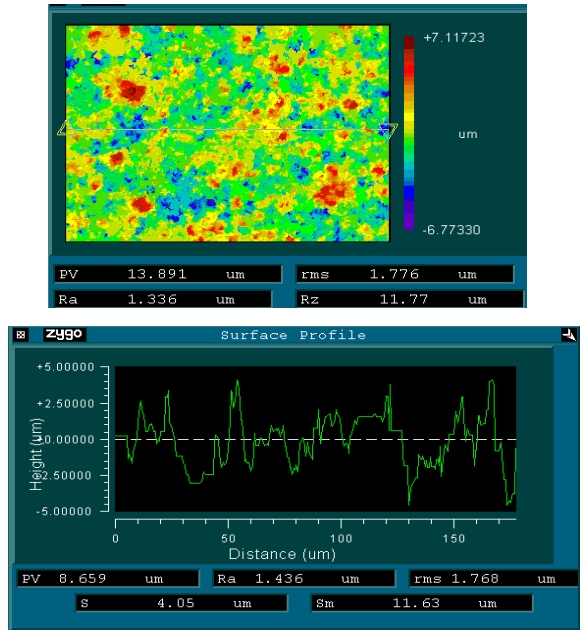
PCB Materials: Copper Oxide/Oxide Alternatives

- **Affect of Process variations and Rework Comparisons (ZYGO) Laser Profilometry**

Light Etch Oxide Alternative: Process D



1 pass (Normal Process)



2 pass (Normal Process + 2 reworks)

PCB Materials: Copper Oxide/Oxide Alternatives

- **Physical Measurement Comparison**

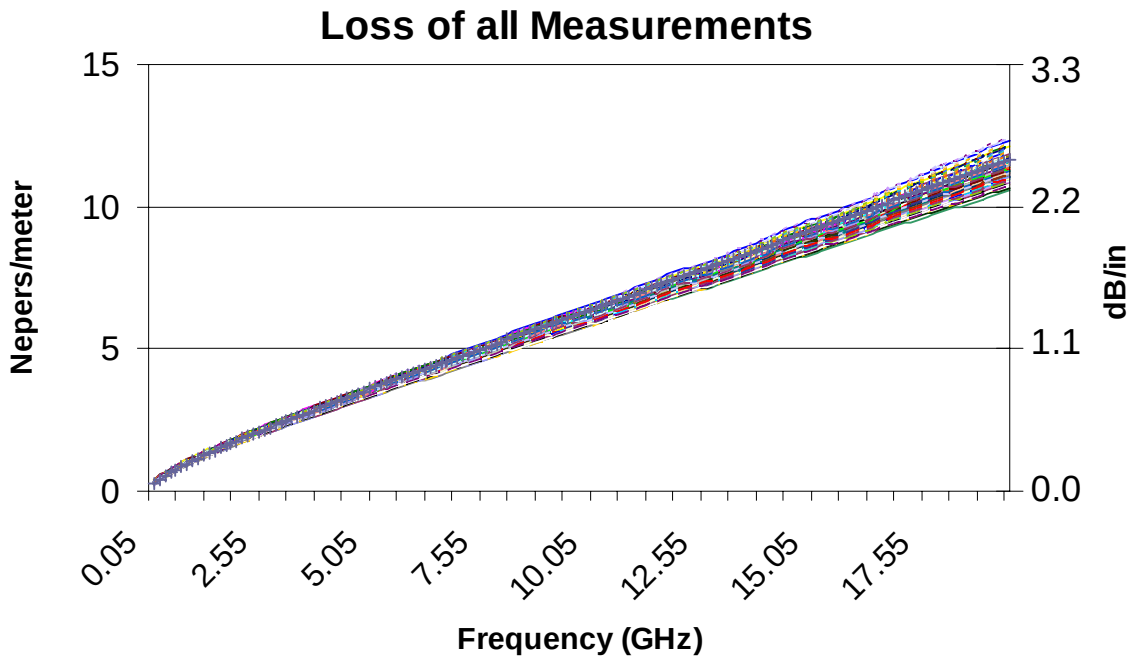
Process ID	Process	Reworks	Ra (um)	Rms (um)	Ave Trace Width (mils)	Ave Trace Height (mils)
A	*Black Oxide*	0	n/a	n/a	4.3	0.68
A	*Black Oxide*	1	n/a	n/a	3.5	0.55
B	*Oxide Dissolution*	0	n/a	n/a	3.9	0.61
B	*Oxide Dissolution*	1	n/a	n/a	3.3	0.45
C	*Oxide Alternative*	0	0.505	0.659	4.2	0.66
C	*Oxide Alternative*	1	0.681	0.922	3.6	0.57
D	*Low-Etch Oxide Alternative*	0	0.469	0.579	4.5	0.71
D	*Low-Etch Oxide Alternative*	1	0.531	0.683	3.9	0.61
D	*Low-Etch Oxide Alternative*	2	1.436	1.768	3.8	0.59

Target: 4.5mil width
½ oz copper

Different Oxide/Oxide alternative processes yield different roughness and different copper thickness and widths

PCB Materials: Copper Oxide/Oxide Alternatives

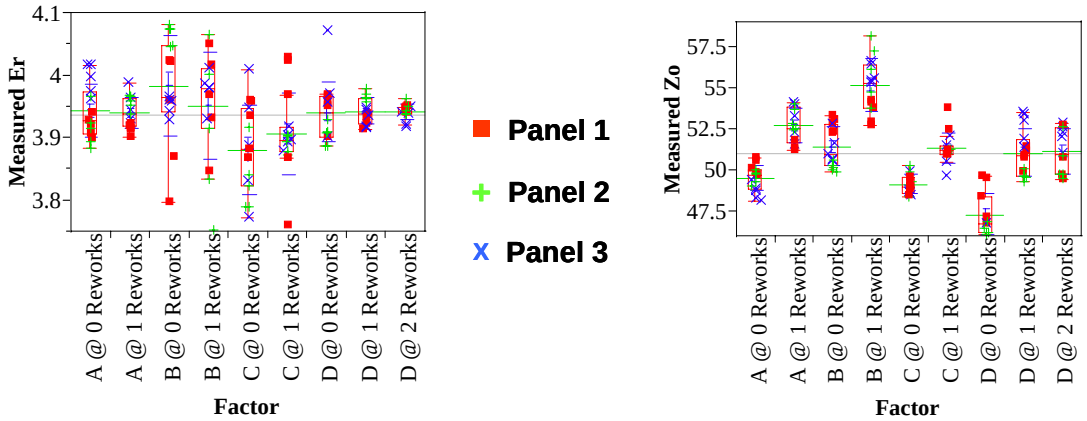
•High Frequency loss differences between different oxide/oxide alternatives not noticed in stripline configurations.



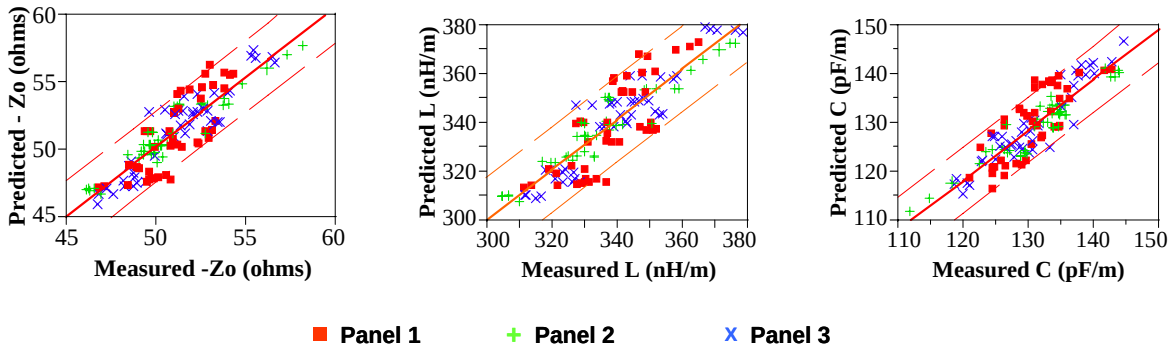
Some Variation between measurements: Range ~0.7dB/in at 20GHz

PCB Materials: Copper Oxide/Oxide Alternatives

- Extracted values at 2.5GHz



- Measured vs Calculated (text book equations: 'Hall, Hall, McCall')



Er consistent with previous spatial data

Zo, C, L tracked with changes in physical geometry

PCB Materials

Copper

Surface Finishes

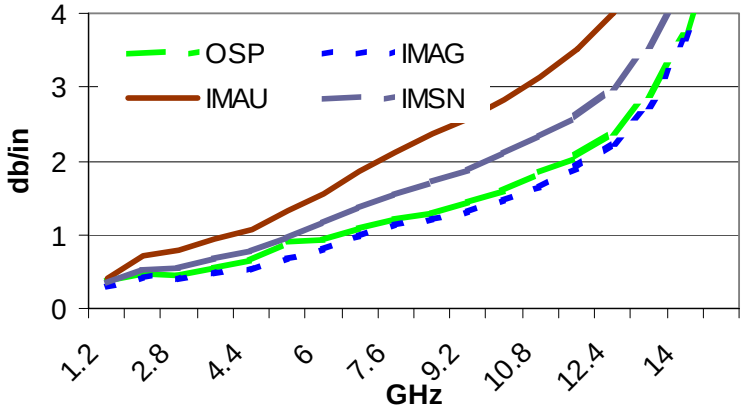
Dielectric Materials

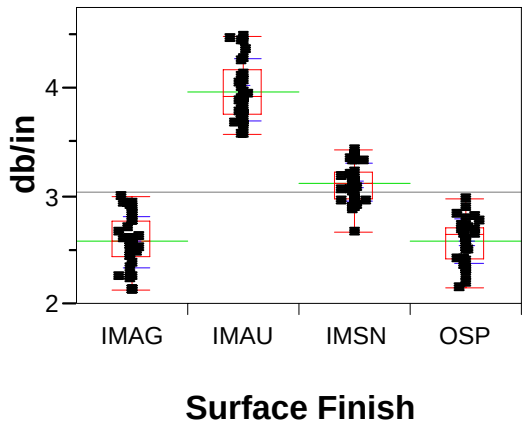
Spatial Properties

PCB Materials: Surface Finishes

- Surface finish will impact loss
  - Primarily on Edge-coupled differential pairs
- Immersion Ag has approx. properties of bare copper (OSP)

Differential loss – measured as co-planar structures





Average dB Loss on
N4000-13 @ 12.4GHz

PCB Materials

Copper

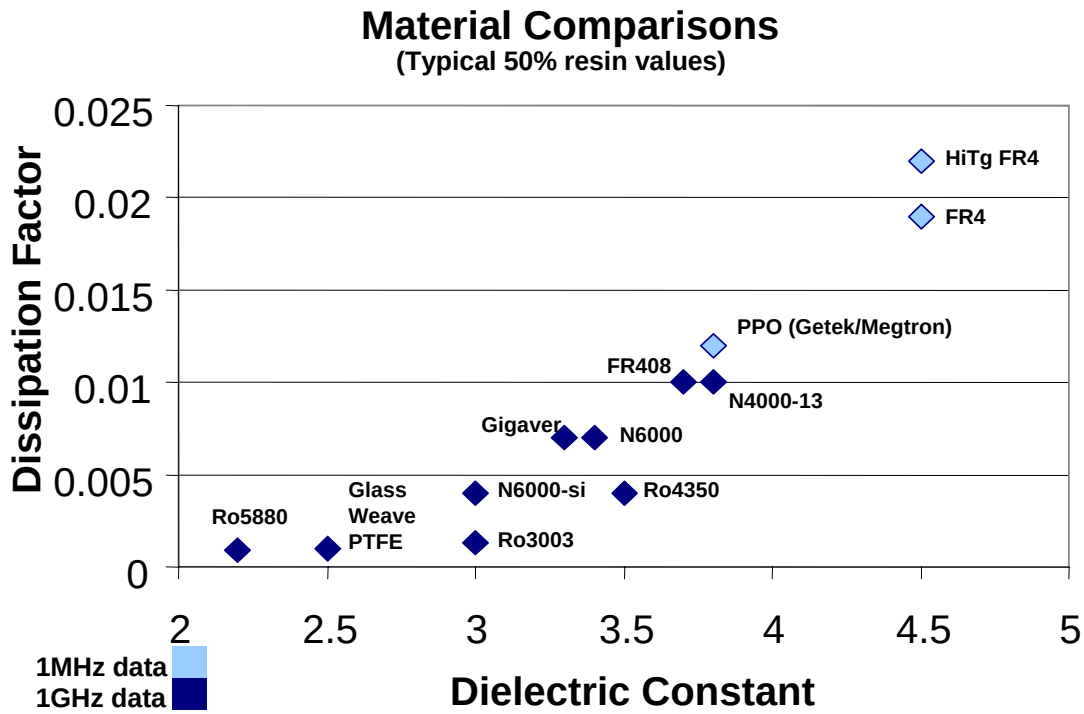
Surface Finishes

Dielectric Materials

Spatial Properties

Comparison Chart

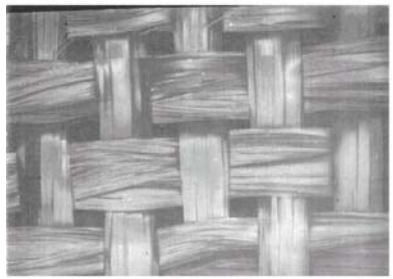
(sample of available materials)



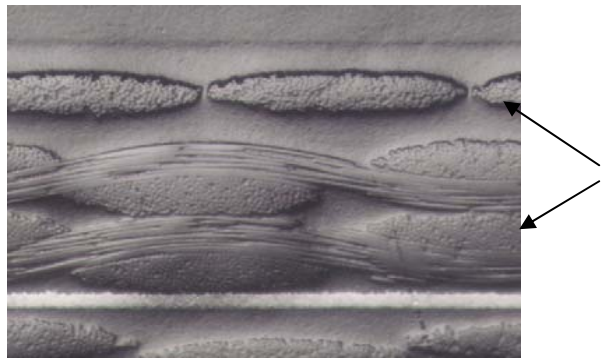
Material properties can be modified by changing resin coated on glass fabric or changing both the resin and reinforcement material

Dielectric Constant

- Dependent on Ratio of glass to resin
  - FR4 Resin: Er ~3.2
  - Glass cloth: Er ~5.6
    - Added for mechanical stability
    - Many different glass cloths
      - Size of fibers
      - #of fibers per bundle
    - Resin ratio control to meet thickness requirements



Glass cloth prior to resin coating



Two glass cloth types

Partial Cross section of laminated PCB

Bulk Dielectric Constant versus Glass Style

Sample FR4 Material Table

Dielectric Properties Table - N4000-2, N4000-6, N4000-6FC

12/19/00

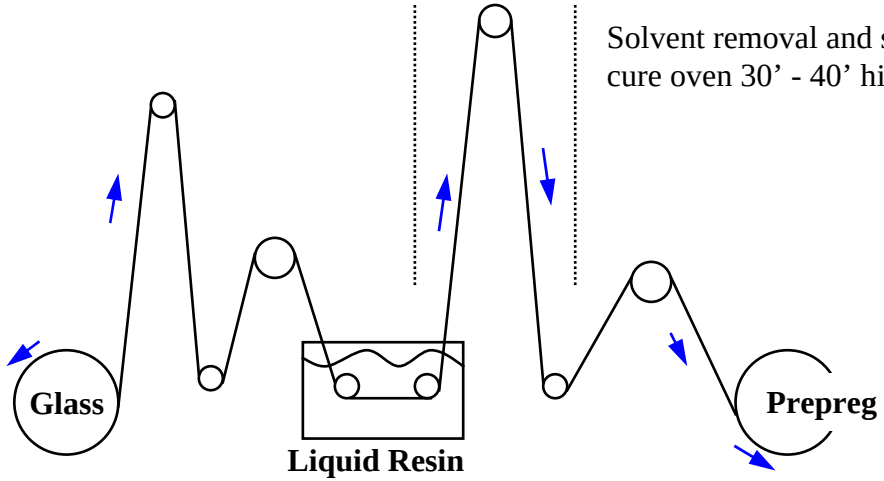
LAMINATE

Thickness	& Tolerance	Construction	RC	1MHz	1 GHz
0.002	± 0.0005	1 x 106	69.0%	3.84 ± 0.34	3.63 ± 0.36
0.003	± 0.0005	1 x 1080	62.0%	4.00 ± 0.33	3.80 ± 0.34
0.004	± 0.0005	1 x 2113	54.5%	4.19 ± 0.36	4.00 ± 0.38
0.004	± 0.0005	1 x 106 + 1 x 1080	57.7%	4.11 ± 0.32	3.91 ± 0.34
0.004	± 0.0005	1 x 2116	43.0%	4.54 ± 0.54	4.37 ± 0.57
0.005	± 0.0005	1 x 106 + 1 x 2113	52.8%	4.24 ± 0.34	4.05 ± 0.36
0.005	± 0.0005	1 x 2116	51.8%	4.26 ± 0.35	4.08 ± 0.37
0.006	± 0.0005	1 x 1080 + 1 x 2113	52.2%	4.25 ± 0.32	4.06 ± 0.34
0.006	± 0.0005	1 x 106 + 1 x 2116	50.8%	4.29 ± 0.33	4.11 ± 0.35
0.006	± 0.0005	2 x 2113	43.5%	4.52 ± 0.43	4.35 ± 0.46
0.006	± 0.00075	1 x 1500	41.7%	4.58 ± 0.57	4.41 ± 0.60
0.007	± 0.00075	2 x 2113	49.6%	4.33 ± 0.39	4.14 ± 0.41
0.008	± 0.00075	1 x 7628	44.4%	4.49 ± 0.44	4.32 ± 0.47
0.008	± 0.00075	2 x 2116	43.0%	4.54 ± 0.46	4.37 ± 0.49
0.008	± 0.00075	1 x 2116 + 1 x 2113	48.6%	4.36 ± 0.38	4.18 ± 0.40
0.008	± 0.00075	1 x 7629	42.6%	4.55 ± 0.47	4.38 ± 0.50
0.009	± 0.00075	2 x 2116	47.8%	4.38 ± 0.37	4.20 ± 0.39
0.010	± 0.001	2 x 2116	51.8%	4.26 ± 0.35	4.08 ± 0.37
0.010	± 0.001	1 x 7628 + 1 x 1080	45.0%	4.47 ± 0.44	4.29 ± 0.47
0.010	± 0.001	1 x 7635	47.5%	4.39 ± 0.41	4.21 ± 0.43
0.012	± 0.001	2 x 1080 + 1 x 7628	45.5%	4.46 ± 0.40	4.28 ± 0.43
0.014	± 0.001	2 x 7628	38.8%	4.69 ± 0.48	4.53 ± 0.51

Courtesy of ParkNelco 2002

Designer Note: Dielectric Constant is a function of resin ration not core thickness

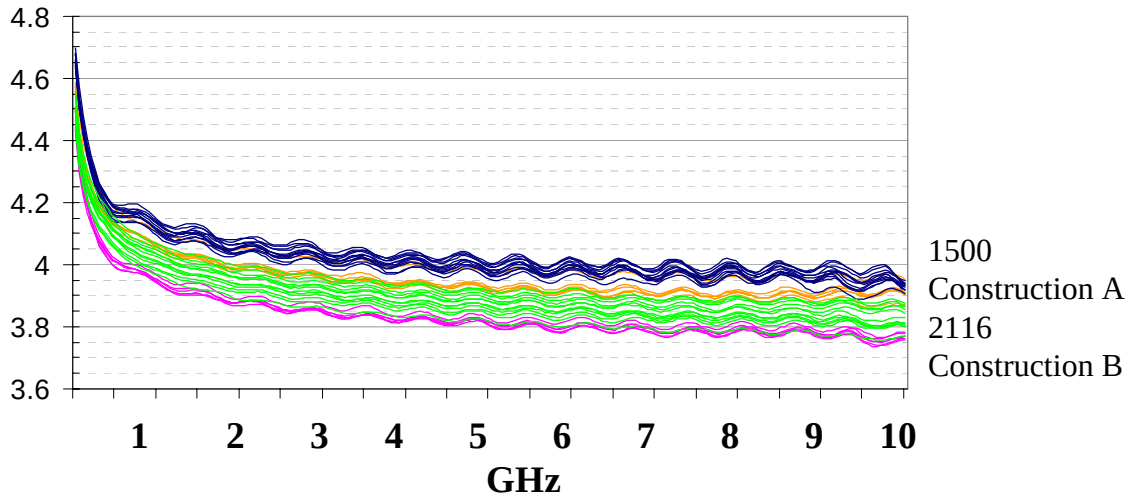
Bulk Dielectric Constant Manufacture Variations of B-Stage



Oven

Dielectric Constant vs Frequency

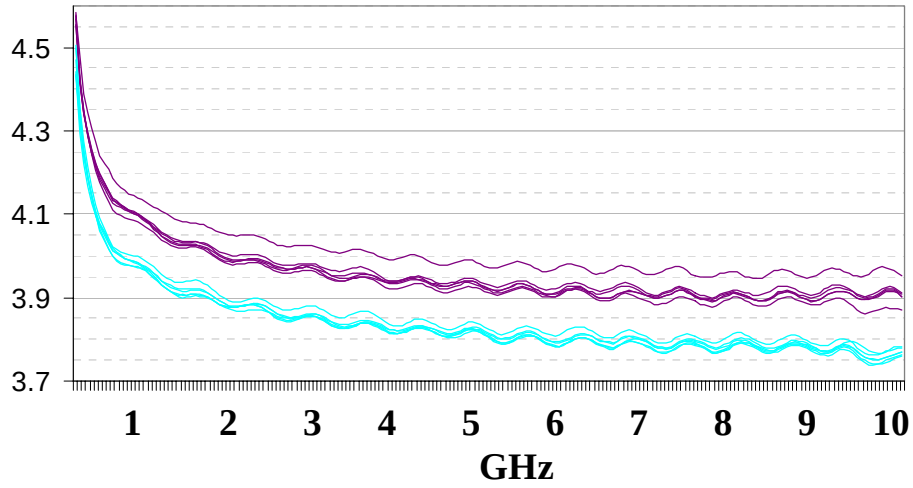
FR4 Material: Intel Test Data vs Reinforcement Style



- Dk follows resin ratio
- Dk as a function of frequency is consistent regardless of resin ratio
- Dk fairly flat above 2GHz

Dielectric Constant

Multi-ply Core Impact

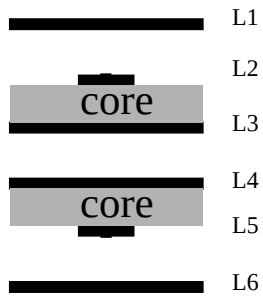


L5 data Trace closest to 2113 ply within the 5core

L2 data Trace closest to 1080 ply within the 5core

In the case of multiple prepregs or plys, dk is dependent on relative placement to the trace

Construction



1080/1080

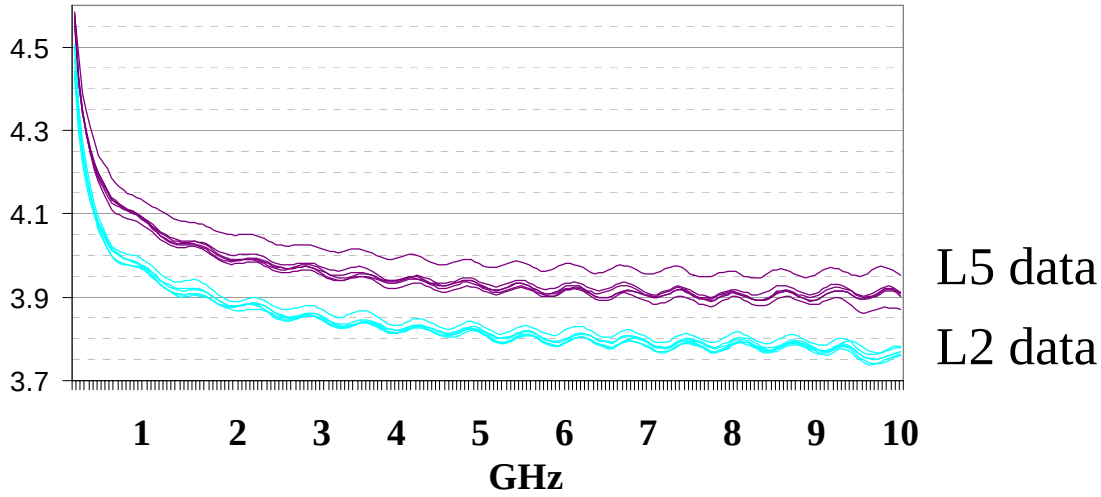
1080/2113

1080/2113

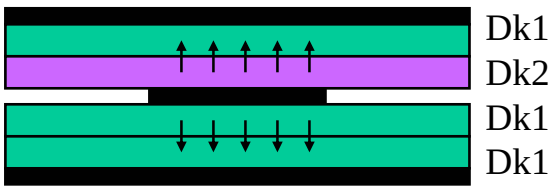
1080/1080

Dielectric Constant

Multi-ply Core Impact

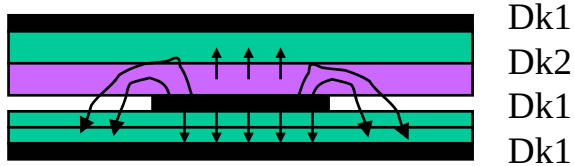


Not perfectly centered stripline so fringe effects will shift effective dk



E-fields such that dk should not be dependent on location of dk2

VS



E-fields such that dk should be dependent on location of dk2

PCB Materials

Copper

Surface Finishes

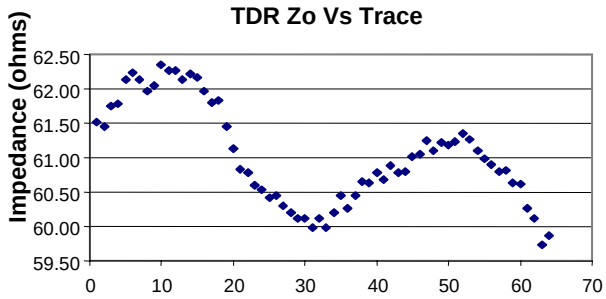
Dielectric Materials

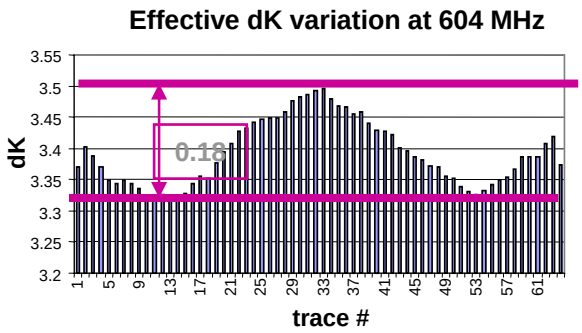
Spatial Properties

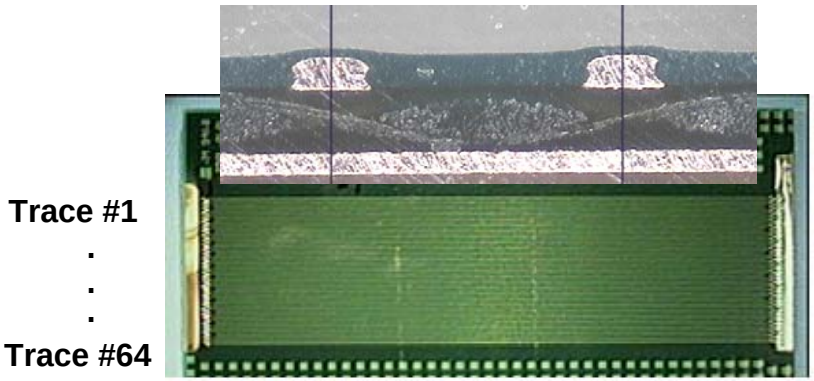
Spatial Dielectric Constant

Glass Reinforcement Impact

- Trace location relative to glass bundle determines effective dk of trace
- Largest impact on time of flight
  - All signals need to arrive at same time
  - Hard to dynamically de-skew
  - Limits bus length
- Zo impact



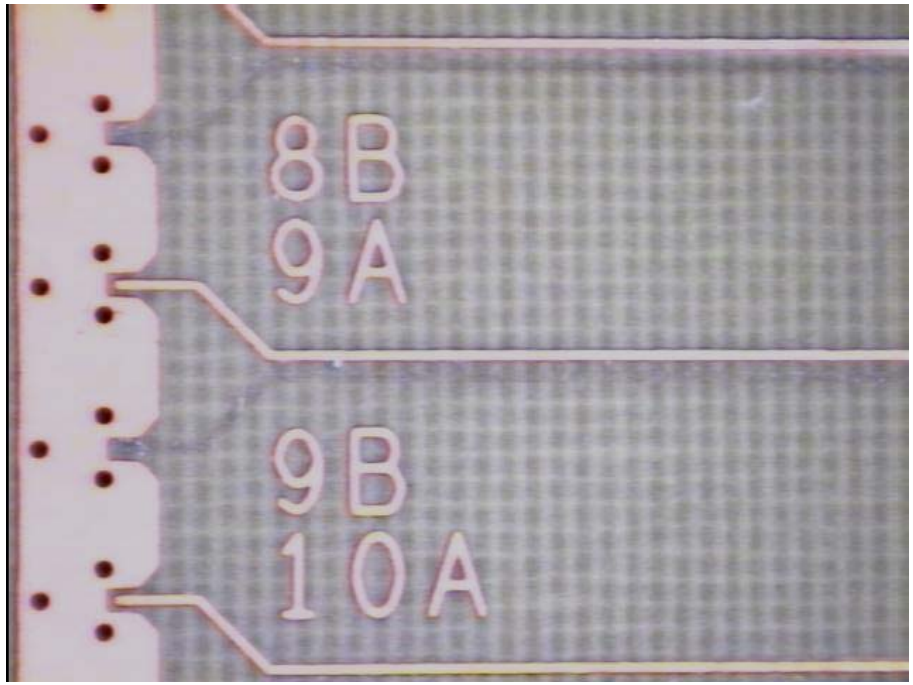




Dk vs spatial placement significant limiter to PCB performance

Spatial Dielectric Constant

Feature Placement vs Reinforcement Material



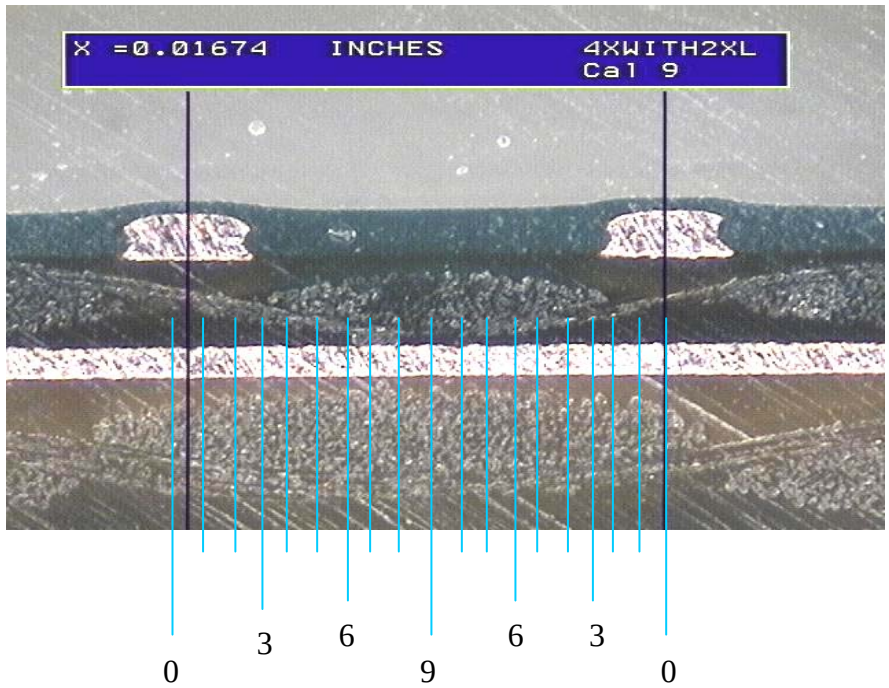
- Trace features can easily align with weave/bundle reinforcement pattern
- Alignment can extend over multiple inches
- Relative alignment to weave knuckle/trough random
- Relative alignment changes with bends/turns in trace features

Spatial Dielectric Constant

Glass Reinforcement Impact

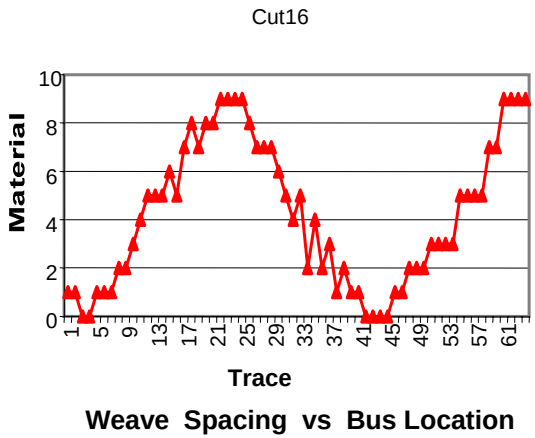
Zo sensitive to relative placement to glass weave bundles.

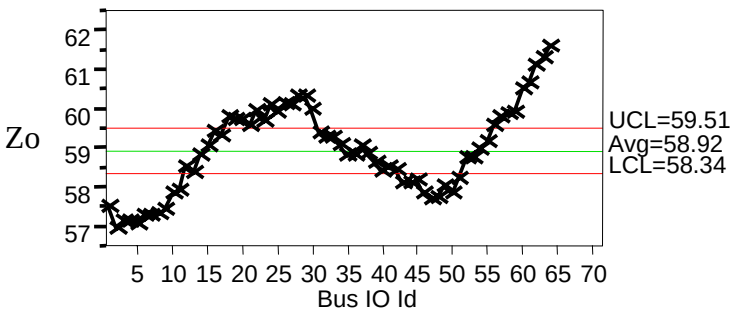
Common glass fabrics used in PCBs have center to center spacing of glass bundles between 16-22mils apart



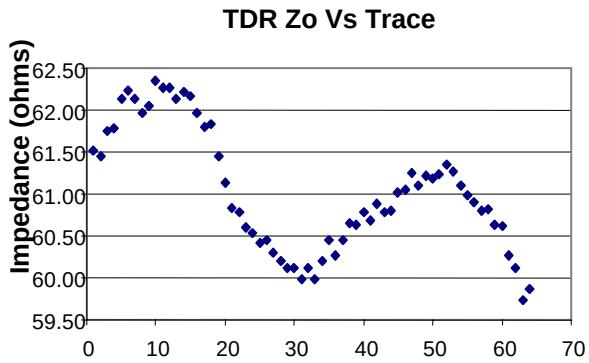
Spatial Dielectric Constant

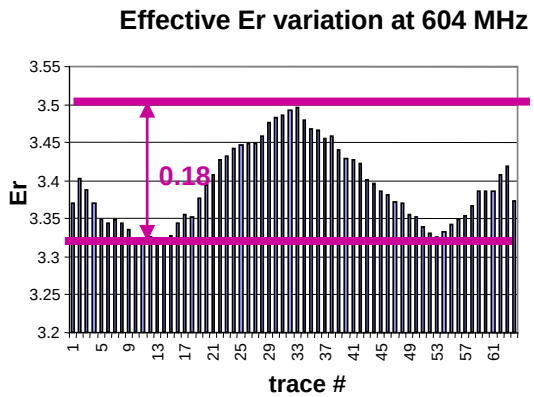
Glass Reinforcement Impact





Trace relative to Weave impacts Zo



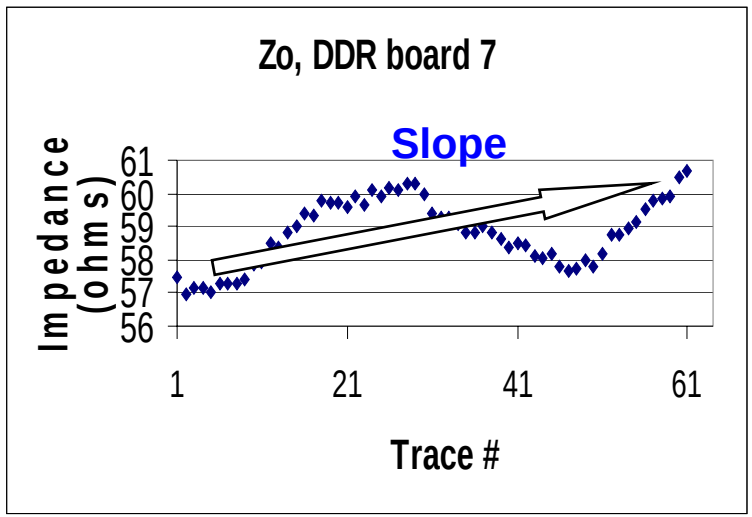


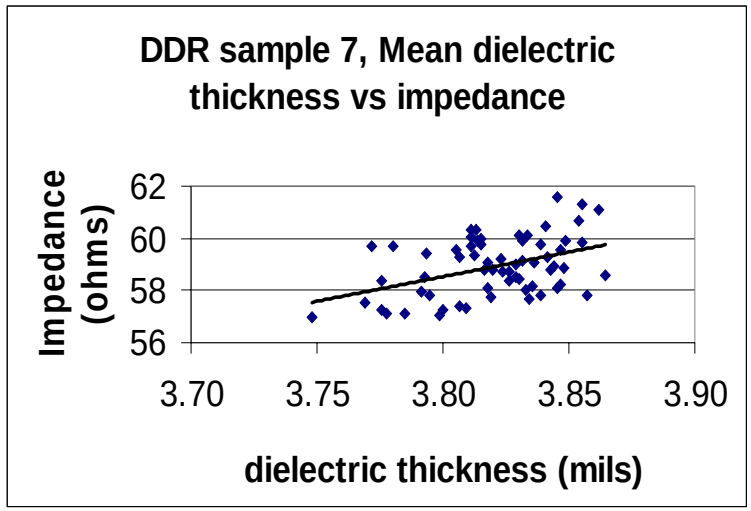
Correlation of Zo to effective Er changes with trace placement relative to glass bundles

Spatial Dielectric Constant

Glass Reinforcement Impact

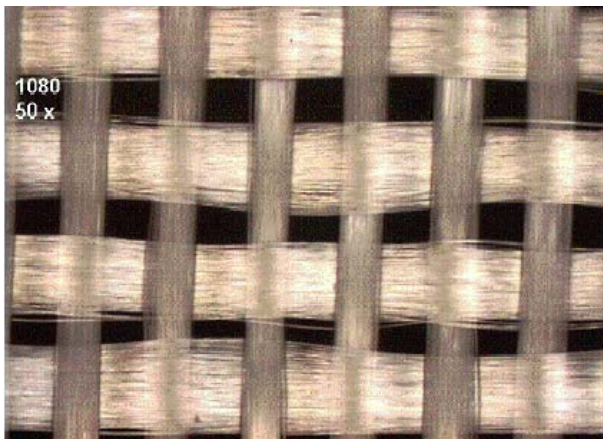
- Glass weave explains periodicity of Zo
- Glass weave does not explain + or – Zo slope across bus
  - Cross section dimensions indicate dielectric thickness is the dominant contributor to slope.



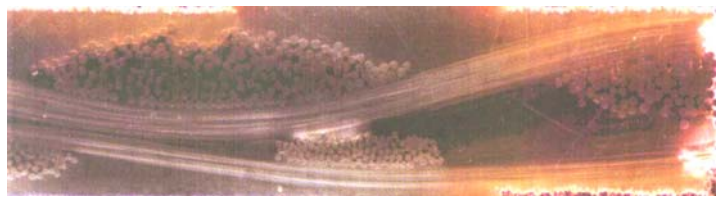


Spatial Dielectric Constant
Source of Variation

- Glass fabric is defined by
  - Weave style
  - Size of glass filaments used in bundles
  - Number of glass filaments per bundle
  - Number of bundles/inch in warp/fill direction
  - Continuous vs stabled filaments



Courtesy of Isola Laminates



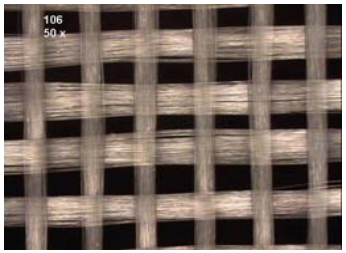
Spatial Dielectric Constant

Glass Weave Table

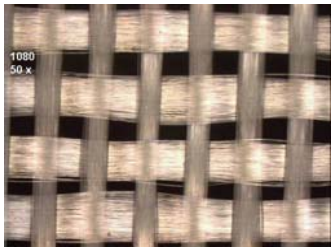
Style	Bundles pitch (mils)	Warp Yarn Filament dia (uin) / #filaments	Fill Yarn Filament dia (uin)/ #filaments	Glass Thickness (mils)
106	17.9x17.9	230 / 102	230 / 102	1.5
1080	16.7x21.3	230 / 204	203 / 204	2.5
2113	16.7x17.9	290 / 204	230 / 204	2.9
2116	16.7x17.2	290 / 204	290 / 204	3.8
1652	19.2x19.2	250 / 408	250 / 408	4.5
1500	20.4x23.8	290 / 100	290 / 100	5.2
7628	22.7x31.3	360 / 408	360 / 408	6.8
7629	22.7x29.4	360 / 408	360 / 408	7.0

Spatial Dielectric Constant

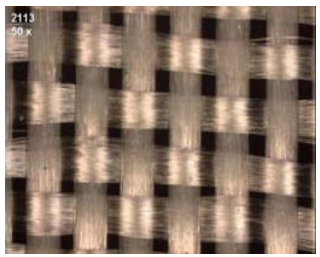
Glass Cloth Samples



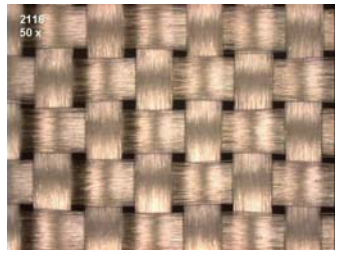
Glass Style: 106
Plain Weave
Count: 56x56 (ends/in)
Thickness: 0.0015 (in)



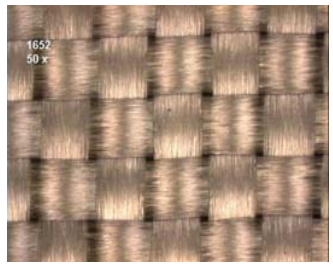
Glass Style: 1080
Plain Weave
Count: 60x47 (ends/in)
Thickness: 0.0025 (in)



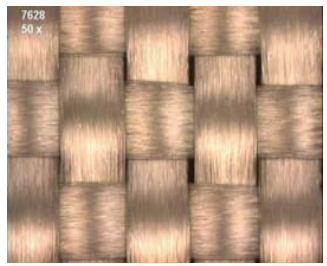
Glass Style: 2113
Plain Weave
Count: 60x56 (ends/in)
Thickness: 0.0029 (in)



Glass Style: 2116
Plain Weave
Count: 60x58 (ends/in)
Thickness: 0.0038 (in)



Glass Style: 1652
Plain Weave
Count: 52x52 (ends/in)
Thickness: 0.0045 (in)



Glass Style: 7628
Plain Weave
Count: 44x32 (ends/in)
Thickness: 0.0068 (in)

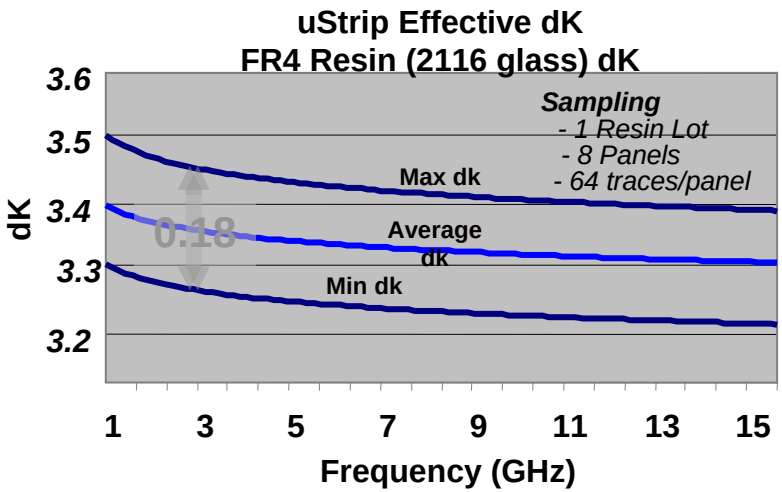
Courtesy of Isola Laminates

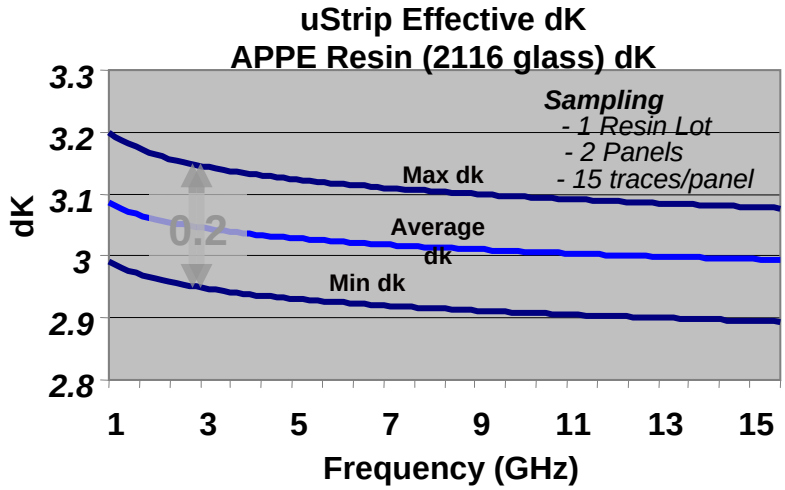
NOTE: The plain weave yarn consists of yarns interlaced in an alternating fashion one over and one under every yarn.

Spatial Dielectric Constant

Glass Reinforcement Impact vs Resin System

- Resin system changes nominal / bulk dielectric constant.
- Dielectric constant variation
  - Dependent on spatial glass/resin ratios
  - Function of dielectric constant delta between glass and resin



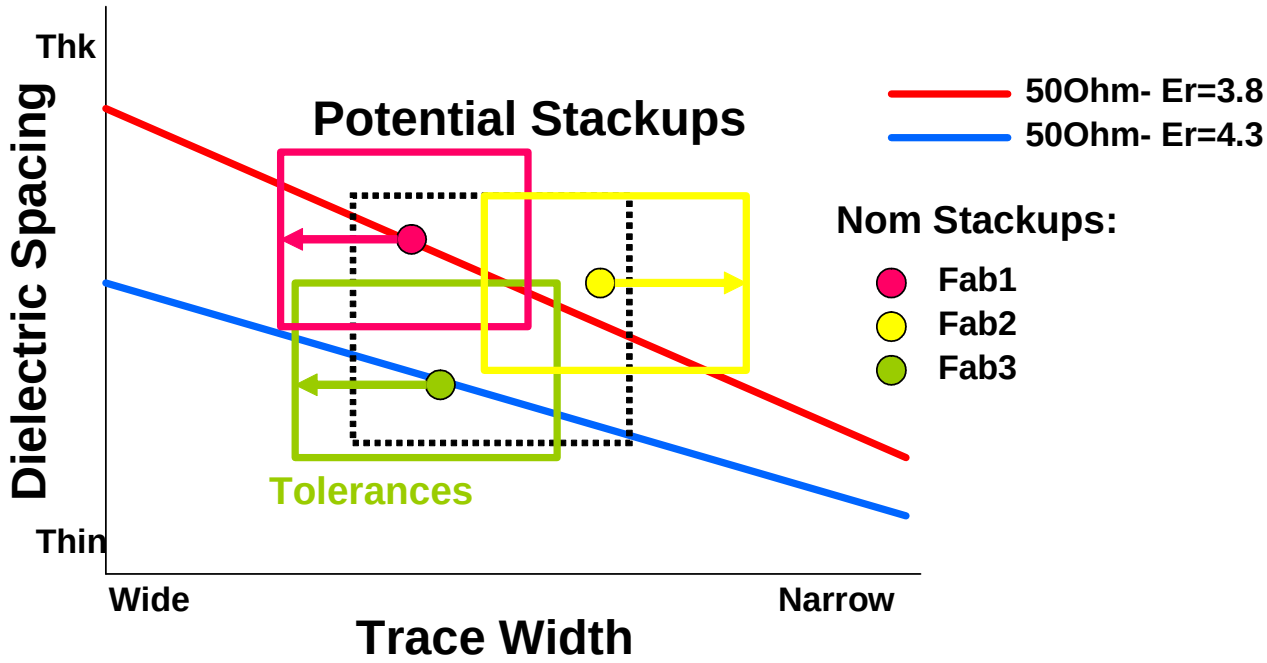


Within panel dK variation similar across Resin Systems

PCB Modeling

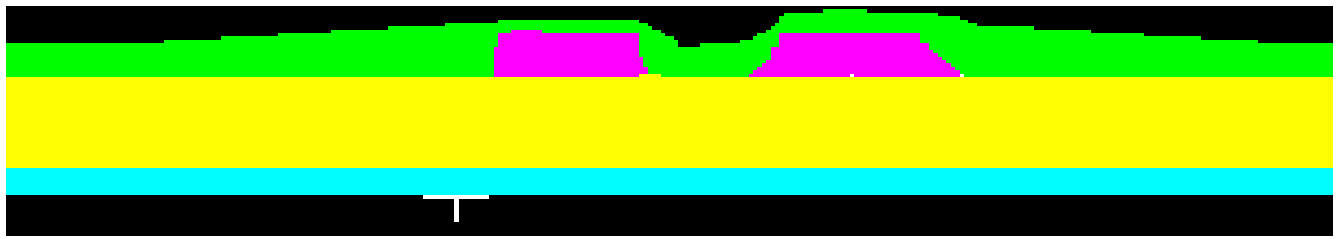
Statistical Tolerance Modeling

- Use Supplier to Supplier Nominals to Determine corners of all features for modeling
  - Use statistical variations to determine worst cases and within supplier or within board variations



Spatial Impacts and Modeling

- Determine corners of all features for modeling
  - Use statistical variations to determine worst cases
  - Remember process implications for worst case corners
    - Forgetting process implications will result in higher modeled Zo stdev
    - Examples
      - Narrow traces modeled as more rectangular due to over etching
      - Wider traces modeled as more trapezoidal due to under etching
      - Modeling materials at –3sigma most likely higher dk due to low resin content



2D models with arbitrary geometries

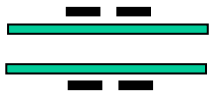
Designer Note: Modeling +/-3sigma corners using measured material and feature tolerance required to yield measured Impedance Capability

PCB Modeling: Conductor Widths

Measured Data (3Sigma Tolerancing)

Outerlayer +/- (0.6-1.0)mils

(1oz Foil+Plating)



Supplier Mean	Ave	**Gerber +/-0.5-0.75mils (Note1)** Max
Within Supplier variation	+/- 0.65 mil	+/- 1.0 mil
Within Lot variation	+/- 0.61 mil	+/- 1.0 mil
Within Board	+/- 0.66 mil	+/- 1.0 mil

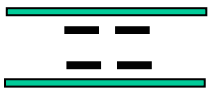
InnerLayer +/-(0.7-1.25)mils

(1oz foil)

Supplier Mean	Ave	**Gerber +/-0.5-0.75mils** Max
Within Supplier variation	+/- 0.8 mil	+/- 1.2 mil
Within Lot variation	+/- 0.7 mil	+/- 1.0 mil
Within Board	+/- 0.6 mil	+/- 1.0 mil

InnerLayer +/- (0.5-1.0)mils

(0.5oz foil)



Supplier Mean	Ave	**Gerber +/-0.5-0.75mils** Max
Within Supplier variation	+/- 0.75 mil	+/- 1.0 mil
Within Lot variation	+/- 0.5 mil	+/- 0.9 mil
Within Board	+/- 0.35 mil	+/- 0.9 mil

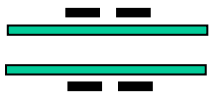
Note1: Suppliers allowed to modify artwork to achieve a nominal target. Per IPC specification, nominal value can vary from Gerber design by +/-1mil

PCB Modeling: Conductor Thickness

Measured Data

Outerlayer — +/- 0.6-1.0mils

(1oz Foil+Plating)

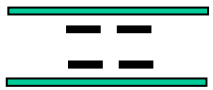


Supplier Mean **1.5-2.7 mils**

	Ave	Max
Within Supplier variation	+/- 0.65 mil	+/- 1.00 mil
Within Lot variation	+/- 0.61 mil	+/- 0.75 mil
Within Board	+/- 0.45 mil	+/- 0.80 mil

InnerLayer — +/-0.13-0.25mils

(1oz foil)

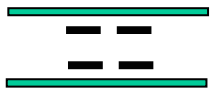


Supplier Mean **1.1-1.3 mils**

	Ave	Max
Within Supplier variation	+/- 0.14 mil	+/- 0.25 mil
Within Lot variation	+/- 0.13 mil	+/- 0.21 mil
Within Board	+/- 0.08 mil	+/- 0.20 mil

InnerLayer — +/- 0.05-0.10mils

(0.5oz foil)



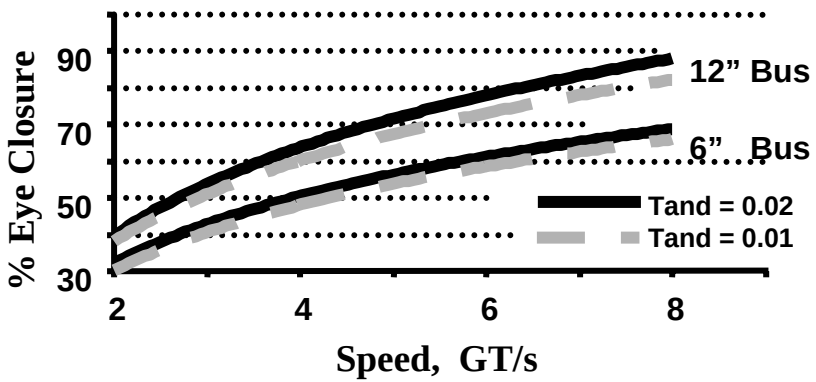
Supplier Mean **0.58-0.63 mils**

	Ave	Max
Within Supplier variation	+/- 0.058 mil	+/- 0.10 mil
Within Lot variation	+/- 0.055 mil	+/- 0.10 mil
Within Board	+/- 0.035 mil	+/- 0.08 mil

Lot variations based on +/-3sigma

PCB Modeling: Dielectric Loss

- Loss vs Dk variations
  - Loss reduces impact of high frequency Dk variations
  - Loss issues mitigated with differential signaling
- Low loss materials
  - Only modest gain in speed for differential signaling
  - Low loss does not dampen Zo reflections
  - Most effective on long busses



Simulation Conditions

- uStrip 5/5/5mil Diff pair
- 15mil pair separation
- Pkg+Pcb+Pkg
- Zo mismatches
- Crosstalk : 2 aggressor nets

PCB Modeling:
Frequency Dependent Loss Tangent

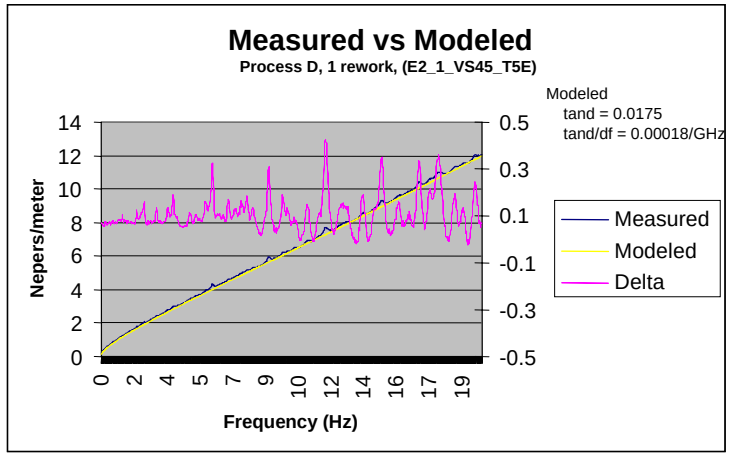
Required to obtain fit above 9-10GHz

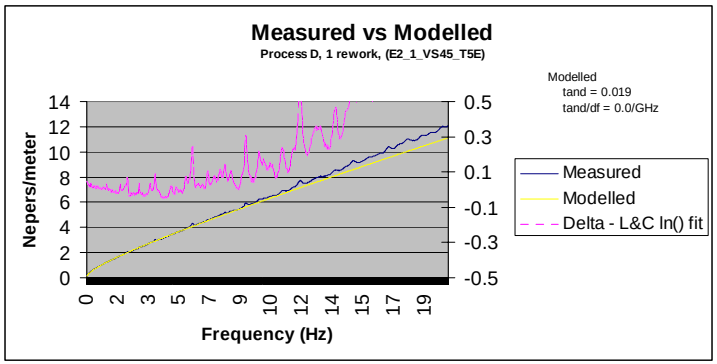
Used frequency dependent loss tangent.

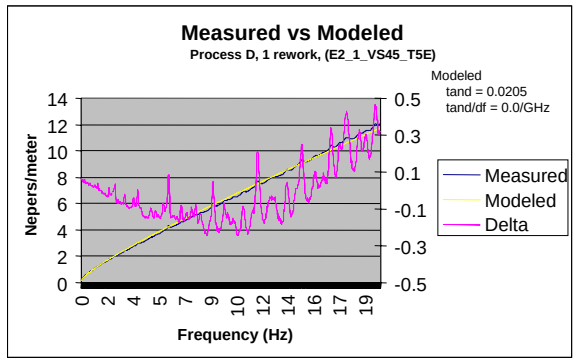
- Approximated by linear fit from data from NIST, material literature
- Good data source – split post resonators.

When using a tand/df component: tand from literature (0.0175) provided good fit.

When not using a tand/df component: Error term not consistent across frequency range and required a larger value then reported

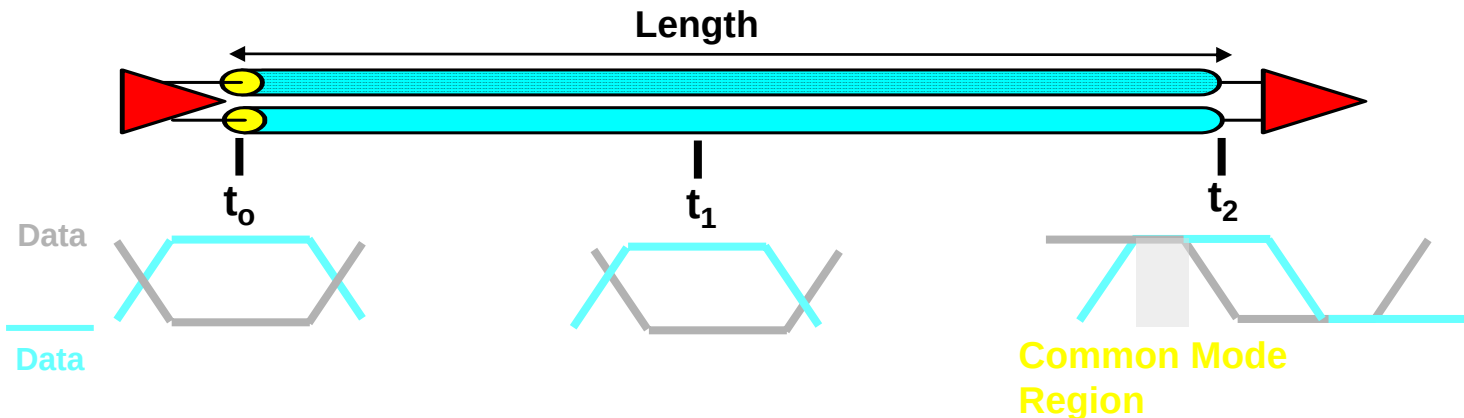






PCB Modeling:
Differential Signaling and Dielectric Constant Variations

- Differential to common mode conversion:
  - Weave location causes Δ propagation delay
  - Differential signals approach in phase across length
  - Common Mode (In Phase) increases noise with increase dk variations



dK Variation == common mode noise

PCB Modeling:
Transmission Loss vs dK variation

- Mode conversion increases signal loss
  - Differential signal loss increases with larger ΔEr.
  - Loss at high frequencies will be dominated by weave

$$V_1 = \frac{+1}{2} e^{-\gamma x} \cos\left[w(t + \frac{x}{v_1}) \right]$$

$$V_2 = \frac{-1}{2} e^{-\gamma x} \cos\left[w(t + \frac{x}{v_2}) \right] \qquad ;\ w = 2\pi f$$

Where:

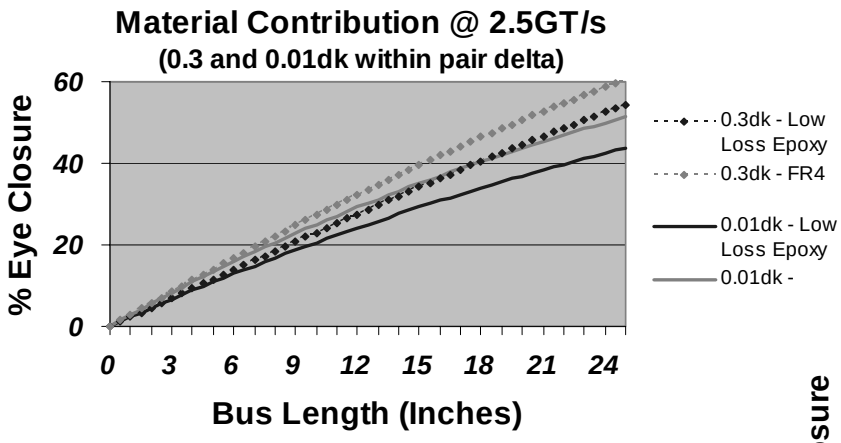
f	Is the frequency of the signal,
x	Is the distance of receiver from transmitter,
γ	Is the attenuation constant of the signal,
v_1, v_2	Is the propagation velocity of V_1 and V_2 respectively.

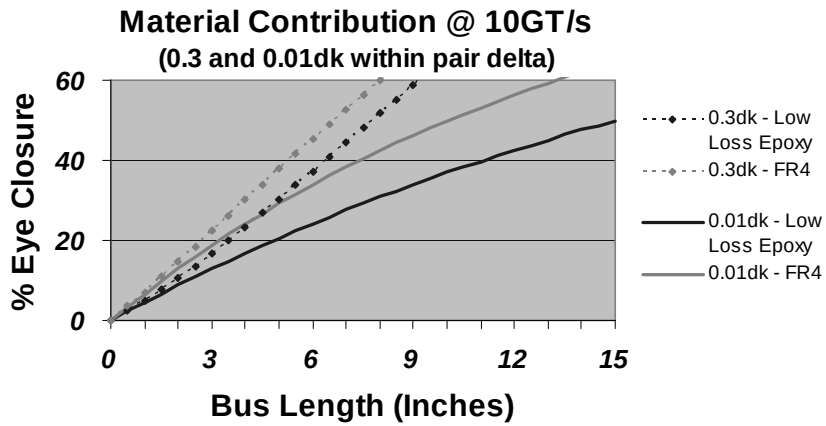
Magnitude of $V_1 - V_2$ is $\left| e^{-\gamma L} \cos\left(2\pi f L \frac{\sqrt{\varepsilon_1} - \sqrt{\varepsilon_2}}{2c} \right) \right|$

PCB Modeling:
Transmission Loss vs dK variation

- Mode conversion increases signal loss

$$\text{Eye Closure} = 100\left[1-\cos\left(\frac{\pi}{6}\right)e^{-\gamma L}\left|\cos\left(2\pi f L\frac{\sqrt{\varepsilon_1}-\sqrt{\varepsilon_2}}{2c}\right)\right|\right]$$



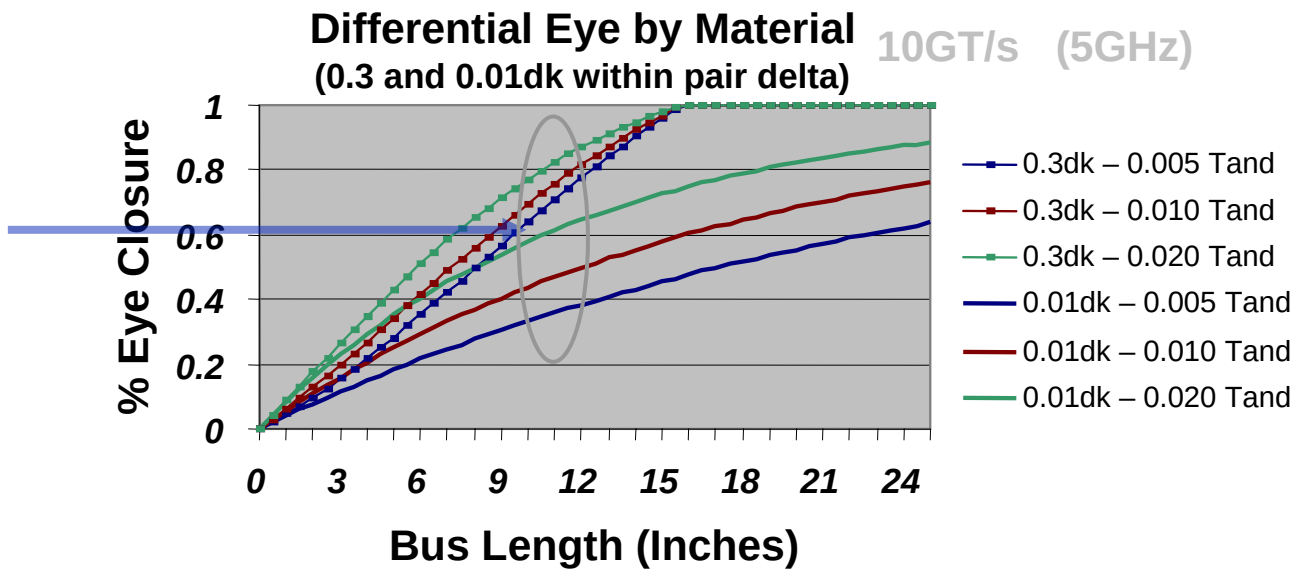


PCB Modeling:

Transmission Loss vs dK variation

- Within Pair dk Delta
  - Forces an absolute max length for 100% Common Mode
  - dK delta reduction has larger impact than changing to low loss resin system

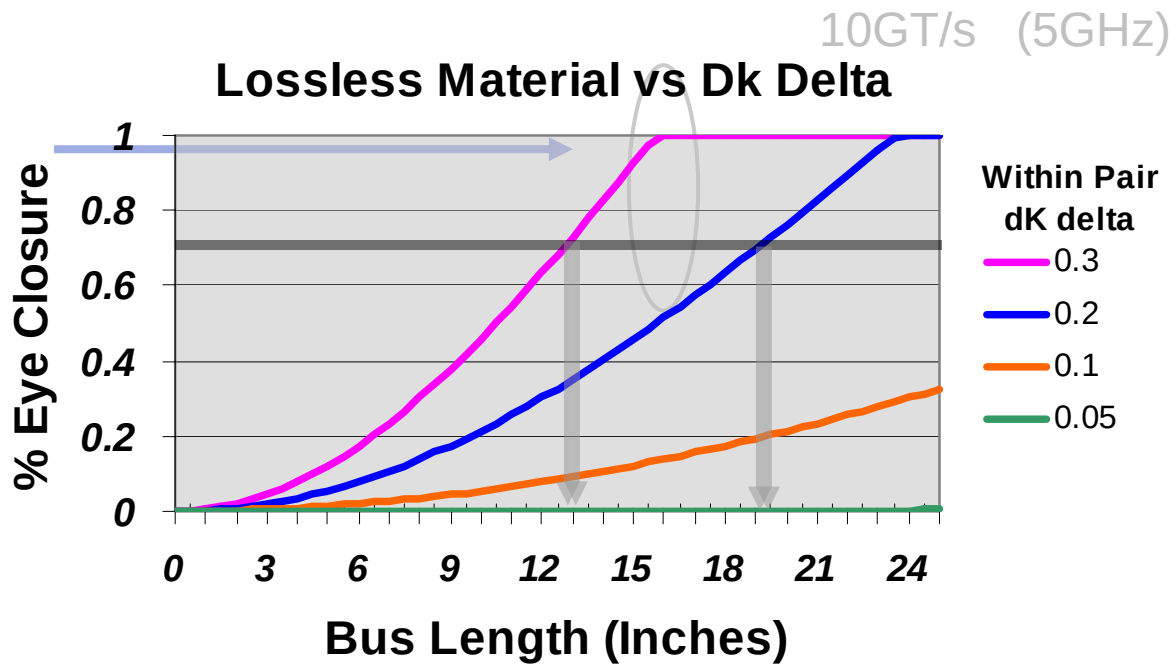
Low dK delta ~2x gain achieved with Low Loss
(10GT/s 11inch bus)



dK Variations Primary Limiter at Higher Frequencies

PCB Modeling:

- dK variation will limit even Lossless materials



Max Bus Length for 70% Eye Closure Specification

Summary

- New Generation I/O Signaling requires accurate characterization and modeling through 15-20GHz.
- Material characterization and modeling as critical as material selection to I/O performance.
- Statistical modeling required to validate and understand within board variation

Summary

- Statistical PCB Fabrication tolerances
  - Larger than typically reported
  - Varies by fabricator and process.
- Copper losses can not be ignored at high frequencies.
- Spatial patterns in dielectric materials require special design considerations.