Physics Division -- *Fast* Electronics Group

Description and Instructions
For a
Beam Raster Monitor Module
For the
Experimental End Stations
At
Jefferson Lab

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1.0 Introduction

A Raster System at Jefferson Lab consists of two pairs of magnet coils for each Raster magnet. The combination of horizontal and vertical magnetic fields will cause deflection of the electron beam at the fixed Raster frequencies. The electron beam at Jefferson Lab is rastered to prevent the beam from overheating targets or vacuum exit windows.[1]

2.0 Purpose of Module

The Beam Raster Monitor is designed to detect fault conditions of the Raster Magnet current(s) that will cause damage to targets or vacuum windows. The module is also designed to monitor the current to each Raster magnet pair and digitize the value of the magnet current amplitude. If a fault condition is detected, the BRM will send a signal to the Fast ShutDown system of CEBAF.[1]

The BRM also provides signal conditioning to two (2) Pearson™ current transducers. The analog current waveform from the Pearson™ transducer is terminated to 50Ω and the module provides a buffered monitor output for viewing on an oscilloscope.

3.0 Brief Functional Description

The BRM is comprised of the following four (4) sections:

1 VME Interface and Power Supply Distribution
2 Analog input
3 RMS-DC converter and Analog to Digital Conversion
4 Fault detection, DAC thresholds, and FSD interface

3.1 VME Interface Registers and Power Distribution

The BRM conforms to IEEE-STD1014 for signal levels and interface definitions of the VME standard backplane. The module uses both P1 and P2 connectors to mate with the VME backplane. The P2 connection uses the pins defined for ground and power only.

The VME address lines, data lines, and bus control lines are connected to an Altera® complex Programmable Logic Device[PLD]. The PLD decodes each address listed in the following tables as a valid address and initiates the proper read or write command to the BRM registers. The proper VME acknowledge signal is returned to the VME controller to verify that a VME cycle was executed properly.

The VME base address of the BRM is configurable by using the on board DIP switches, A15-A5. The following table list the memory locations and the values associated with each read or write register.

Table 1: BRM Address Map

Address	**Read/Write [* 8-Bit *]**	**Register Description**	**Notes**
Base + x00	Read	ADC Channel 0	X Magnet Current
Base + x02	Read	ADC Channel 1	Y Magnet Current
Base + x04	Read	ADC Channel 2	X_Low Threshold DAC
Base + x06	Read	ADC Channel 3	X_High Threshold DAC
Base + x08	Read	ADC Channel 4	Y_Low Threshold DAC
Base + x0A	Read	ADC Channel 5	Y_High Threshold DAC
Base + x00	Write	DAC Channel 0	X_Low Threshold
Base + x02	Write	DAC Channel 1	X_High Threshold
Base + x04	Write	DAC Channel 2	Y_Low Threshold
Base + x06	Write	DAC Channel 3	Y_High Threshold

Address	Read/Write	D7	D6	D5	D4	D3	D2	D1	D0	Note
Base + x10	Read	NC	NC	NC	NC	Y_High Trip	X_High Trip	Y_Low Trip	Y_High Trip	FSD Status Register
Base + x12	Write	Clear FSD	User	User	User	User	User	User	User	FSD Control
Base + x12	Read	FSD	User	User	User	User	User	User	User	FSD Control

[1] CEBAF Report 94-001; 7 July 1994

3.1 VME Interface Registers and Power Distribution [Continued]

The BRM uses three VME backplane supplied voltages. Each voltage passes through an EMI filter and each voltage is fused to 1Amps with on board fuses. An on board regulator provides –5Vdc to several circuits. Table 2 lists the required voltages and measured current requirements.

Backplane Voltage	Required Current	Fuse[Reference Designator]	Filter Reference Designator
+ 5 VDC	0.46 Amps	1Amp [F1]	FILT1
+12 VDC	0.14 Amps	1Amp [F2]	FILT2
-12 VDC	0.11 Amps	1Amp [F3]	FILT3
-5 VDC [Regulated from –12 VDC]		{-12 VDC fused}	No EMI filter

3.2 Analog Input

The X and Y current transducers are connected to the BRM on two (2) female BNC connectors. The BRM transducers are Pearson™ type current probes and are connected to the BRM using 50Ω RG-58 coaxial cable. Each input is terminated into 50Ω.

The input signal from the Pearson™ transducer is amplified by a factor of 2 and the amplifier stage drives a buffer amplifier. The buffer amplifier output is routed to the monitor output connector on the front panel. The monitor output will drive long cable lengths and provide enough current to drive a 50Ω load. The output voltage transfer function is 0.1V per Amp.

The BRM input stage is designed to handle the specifications of the Pearson™ current monitor. The specifications for the Pearson™ current monitor are given in the parts list appendix.

The input signal is also routed to an adjustable gain amplifier, which is used to optimize the input to the RMS-DC circuit. By using this adjustment the BRM full-scale range can be set and the conversion factors calibrated.

3.3 RMS-DC and Analog to Digital Conversion

Each input, X and Y, has a RMS-DC converter circuit. The RMS-DC converter is a precision integrated circuit manufactured by Analog Devices. The input to the RMS-DC converter is amplified as explained in the previous section in order to set the dynamic range of the BRM. The transfer function for the RMS-DC converter is 0.707 for sine wave input. The RMS-DC transfer function for amplitude modulated inputs will need to be calibrated for the given magnet current waveform. The RMS-DC function is of course very linear and the DC output voltage from the converter is connected to the eight-channel analog to digital converter.

The analog to digital converter is manufactured by Maxim and is an eight channel, eight bit, data acquisition system packaged into one twenty-eight pin integrated circuit. The eight channel ADC furnishes a very simple means of converting eight voltage levels to digital values that are presented to the VME data bus on command. The ADC has on board sample and hold circuitry as well as latched registers, which can be read out while new values are stored. The ADC requires an external voltage reference and external clock signal. The full-scale voltage reference is +5 volts and the clock rate is set at approximately 100khz.

3.4 Fault Detection, DAC Thresholds and FSD interface

Each input, X and Y, is monitored for various fault conditions. Each input is connected to a current transducer for a given raster magnet. For a given beam energy and beam current, the raster magnet current must fall between a minimum and maximum setpoint. The input current waveforms are converted to positive DC levels and presented to voltage comparator circuits. The upper and lower threshold limits to the comparator are set by a Digital to Analog Converter. Each channel, X and Y, use an upper and lower threshold voltage from the DAC.

The DAC is an eight channel, eight-bit device manufactured by Analog Devices. The BRM uses only the first four DAC outputs for setting the upper and lower limits of the fault detection comparators. The unused DAC outputs are not connected. The DAC requires a precision voltage reference that is configured for a +5 volt maximum range.

The main function of the BRM is the Fast ShutDown interface. The BRM measures the magnet current amplitude and

compares the measured value with programmed limits. If the measured magnet current falls outside the upper and lower threshold window the FSD circuit will trigger. The FSD output is a straight through fiber optic connector on the front panel of the BRM that is connected to the Accelerator FSD System. The FSD input “nodes” requires a 5Mhz clock, which represents a “No_Fault” state. Absence of a 5Mhz signal for even a short duration will shutdown beam.

The FSD circuit is a programmable logic device[PLD] that monitors the four (4) comparator outputs and latches the state of the comparators when a FSD condition is detected. The state of the four (4) comparators can be readout from VME at any time. After a fault is detected, the FSD circuit[PLD] will remain in the latched state until the user send a “FSD clear” command. The FSD clear command is simply a single bit, which must be toggled by the user. Once the FSD clear bit is toggled the 5Mhz signal is passed to the fiber optic transmitter if no faults are detected.

4.0 BRM Specifications

Single Wide VME IEEE-STD1014 module

INDICATORS: [Front Panel]
+5V DC OK: Green LED
+12V DC OK: Green LED
-12V DC OK: Green LED
MODSELECT: Green LED Flashes for all valid module address commands

INPUT: [Front Panel]
Two (2) inputs, X and Y, on female BNC connectors. 50Ω termination
Typical input is connected to Pearson™ current transducer.
Maximum input is 10Vp-p.
Maximum input frequency is 5Mhz.
Minimum input frequency is 20hz.

ANALOG-TO-DIGITAL CONVERSION:

8 Bit resolution. +5 volt full scale. 0.196 volts per Least Significant Bit.[LSB]
Input to ADC is driven from RMS-DC converter. Positive DC levels only.
100khz sample clock.

8 bit data is straight binary format. 0V = x00; +5V = xFF
Data is stored automatically on-chip dual ported RAM and can be read from any channel of the ADC via VME at any time.

OUTPUT: [Front Panel]
Two (2) outputs on female BNC connectors.
Outputs will drive 50Ω load to 10Vp-p.[+/- 200ma buffer output]
Output driver protected from short circuit.

FSD OUTPUT: [Front Panel]
ST style fiber optic connector. Five (5) megahertz signal is present if no fault conditions are detected.

5.0 BRM Instructions

5.1 Setting the base address

The BRM base address is set by switches labeled A15 through A5. The switches are located near the P1 DIN connector. Setting the switch to the ON position sets the address bit to zero(0). An example is given below in Table 2.

Table 2. Switch setting for Base Address [A16 Space]

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4-A1
Off	Off	Off	Off	Off	Off	Off	Off	Off	Off	On	Program
1	1	1	1	1	1	1	1	1	1	0	Space
F				**F**				**C**			

In this example the user has selected xFFC0 with address bits A4-A0 defining the usable programming space for this module.

5.2 Programming

Once the base address is set the user can access each register listed in Table 1. Keep in mind that the module supports single byte accesses commands for odd or even addresses. Typical VME access is A16:D16. Examples will assume that the user will use two byte access for reading and writing the registers. The BRM98 module only uses the lower eight (8) bits of the data word for read values and write values.

The BRM module provides a “module select” indicator which will flash for every valid BRM address access.

5.2.1 Programming—Read ADC Values

There are six Analog to Digital channels on the BRM module. Please reference Table 1. The magnet currents and threshold limits are measured and stored on the ADC registers. Due to the feature of the ADC, these registers can be accessed at any time. Below is pseudo code for reading the ADC registers. [Offset x00 – x0A]

```
Example 1:      Read X_Magnet Current register. [ Offset x00 ]
Base=xFFC0
Offset=x00                          //Magnet Current ADC register
Read_VME_Register(xFFC0)
AND readback Value with x00FF;      //Don’t use upper byte of data.
(Value) * (Coefficient)= Amps peak.;  //Display Amps on screen

Example 2:      Read Y_High_Threshold register. [ Offset 0Ah ]
Base=xFFC0
Offset=x0A                          //Y High Threshold readback register
Read_VME_Register(xFFCA)
AND readback Value with x00FF;      //Don’t use upper byte of data.
(Value) * (Coefficient)= Amps peak.;  //Display Threshold [Amps] on screen
```

5.2.2 Programming—Write Threshold DAC Values

There are four Digital to Analog channels on the BRM module. Please reference Table 1. These thresholds set the upper and lower limit of the fault detection comparators. The DACs are 8 bit devices. Below is a pseudo code example of writing to the threshold DACs. [Offset x00 – x06]

```
Example 3:      Write Y_High_Threshold DAC register. [ Offset x06 ]
Base=xFFC0
Offset=x06                          //Y_High Threshold DAC register
Calculate Current_Threshold_value;
(Current_Threshold_value) * (Coefficient)=Write_DAC_Value;
Write_VME_Register(xFFC6, Write_DAC_Value);
```

5.2.3 Programming—Read FSD Fault Bits

The FSD fault register reads the latched state of the FSD fault bits. This register can be read at any time and Table 1 lists the definition for the corresponding register bit. A bit value of one[True] means that the bit is NOT faulted. The example pseudo code below shows how to read the FSD fault register. [Offset x10]

```
Example 4:  Read FSD fault register bits. [Offset x10]
Base=xFFC0
Offset=x10h
Read_VME_Register(xFFD0)            //xFFC0 + x10 = xFFD0
Display bit values;                 //Bit=1 NOT Faulted
```

5.2.4 Programming—FSD Control Register

The FSD control register is used to clear the latched FSD fault bits. Another feature of this register is that it can be used as a “mailbox” to be used as an “alive” bit function. The most significant bit is used as the clear command to the FSD fault PLD. This bit must be toggled to clear the FSD fault PLD. The FSD control register is read/write and is an eight bit register. The following example pseudo code depicts how to use the FSD control register. [Offset x12]

```
Example 5:  Read and Write FSD control register [Offset x12]
Base=xFFC0
Offset=x12h
//Toggle FSD Clear Bit
Write_VME_Register(xFFD2, x80);     //xFFC0 + x12 = xFFD2
                                    //x80 Bit 8 set High
Write_VME_Register(xFFD2, x00);     //x00 Bit 8 set Low

//Write and Read “Alive Bit”. Runs forever
Read_VME_Register(xFFD2);           //Read control register
Write_VME_Register(xFDD2, x01);     //Alive bit is Least Significant Bit for instance
Read_VME_Register(xFFD2);           //Read control register
Write_VME_Register(xFFD2, x00);     //Bit=0
```

6.0 Basic Troubleshooting

After setting the base address and inserting the BRM98 VME module in a standard powered VME crate the user should verify that the power supply indicators are illuminated. All the indicators must be on[Green] in order for the module to function properly. If any of the indicators are not illuminated the user should check the replaceable fuses located near the P1 backplane connector. Be sure to replace the fuses with the equivalent rated fuse.

The module selection indicator is a useful when initially programming the module. The indicator will only flash for valid VME address access to the modules address space as given in Table 1. In case the module select indicator does not flash for attempted VME bus access, verify the base address. Write down the switch settings for A15-A5 and remember that a switch in the ON position means the address line is set to zero. The user should also verify software and be sure the proper VME address space is being requested.

Appendix A

SCHEMATIC DIAGRAMS

Schematic Sheets can be found at:
http://www.jlab.org/exp_prog/electronics/HallA_app.html

APPENDIX B

COMPONENT PLACEMENT DIAGRAM

Circuit Board Fabrication Drawing can be found at:
http://www.jlab.org/exp_prog/electronics/HallA_app.html

APPENDIX C

BILL OF MATERIALS

Bill of Materials can be found at:
http://www.jlab.org/exp_prog/electronics/HallA_app.html

APPENDIX D & E

PLD EQUATIONS