DIGITAL FIELD CONTROL: Architecture and Implementation of Feedforward and Feedback Techniques

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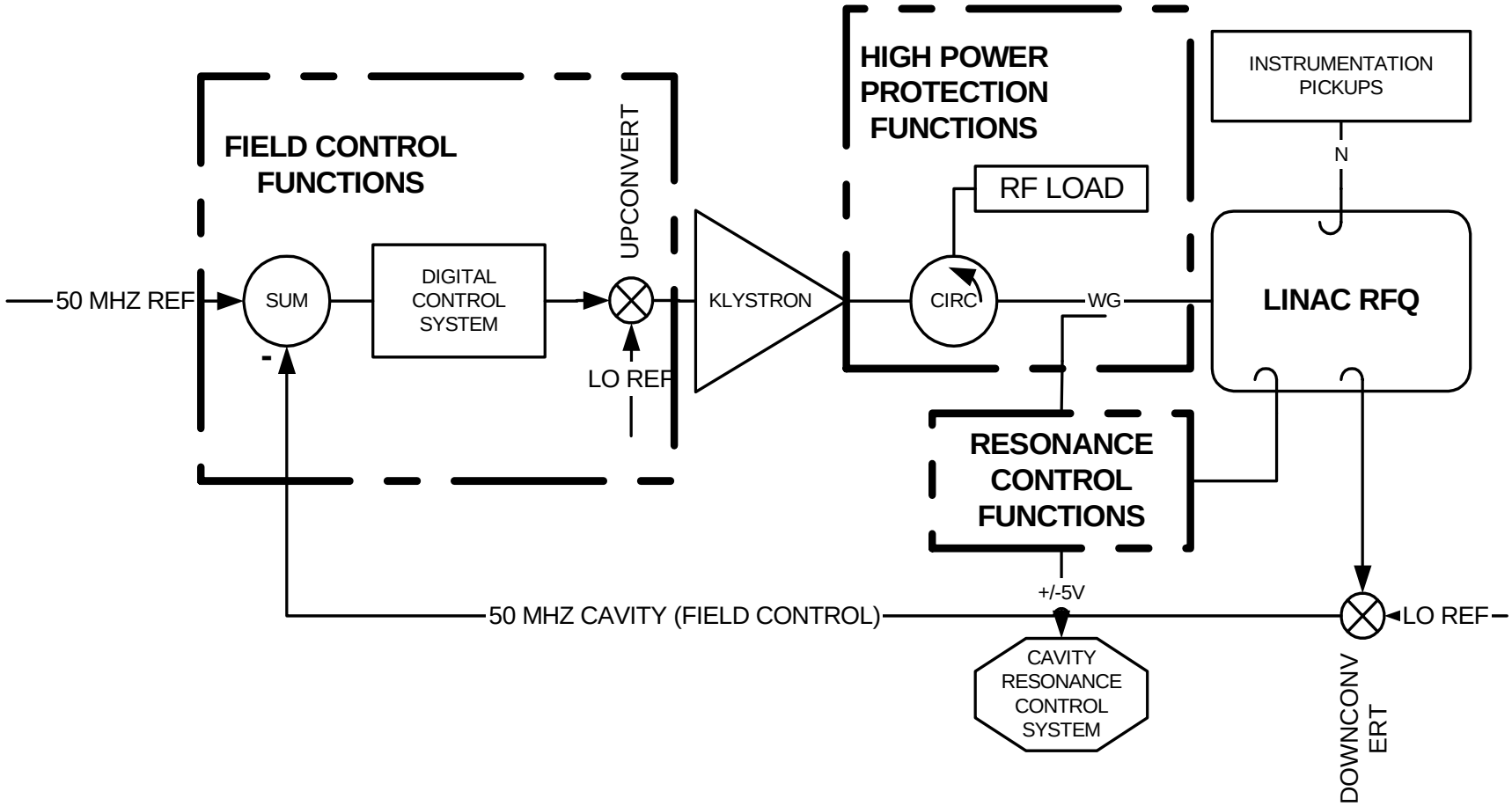
Outline

- Overall system configuration
- System Requirement and Specifications for FRC module
- Field Control Algorithm - PI Feedback & Adaptive Feed_forward
- Resonance Control Algorithm
- Field & Resonance Control Module Implementation
- Summary

RFCS Functional Block Diagram



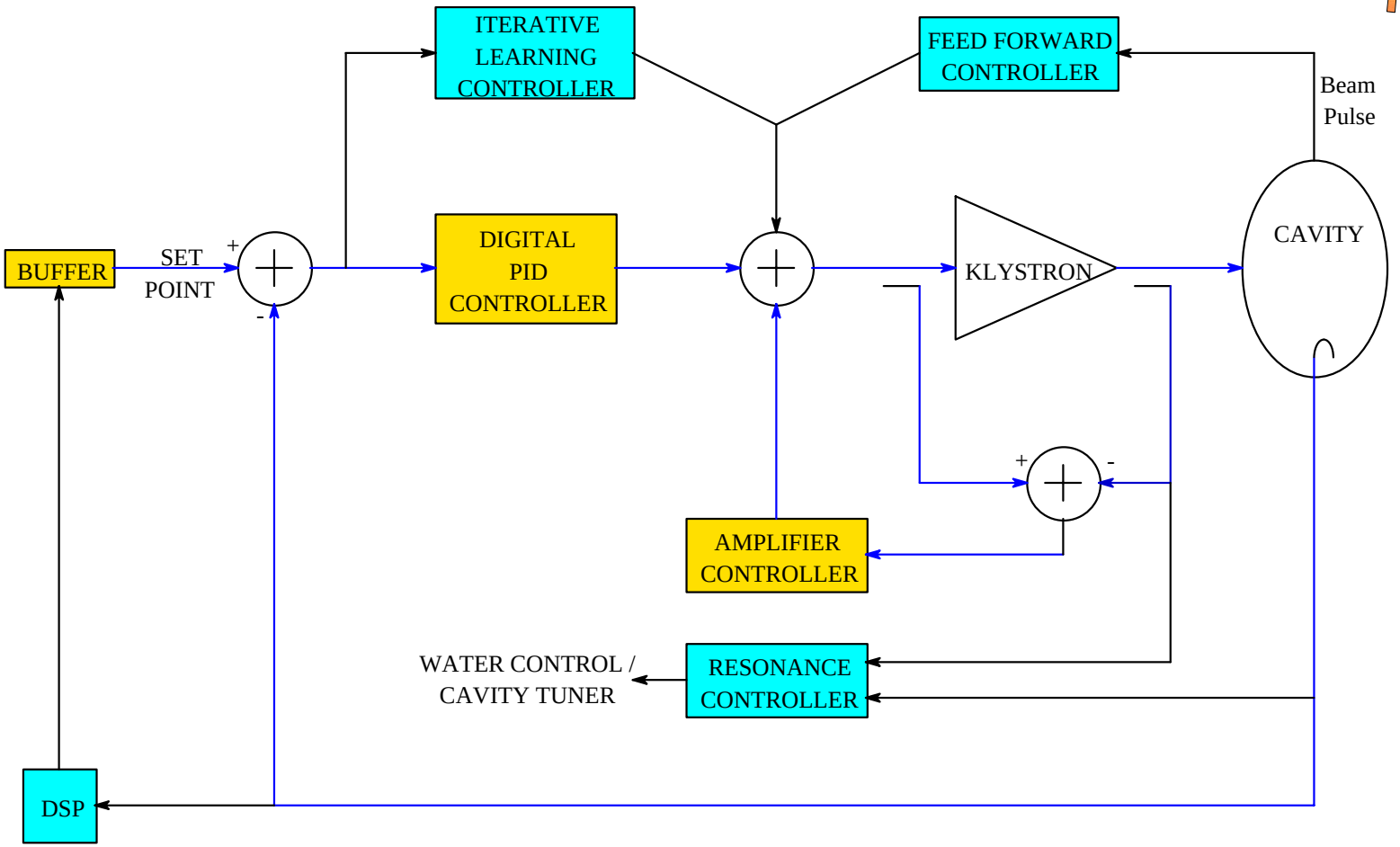
RF control system requirements drive design

- REQUIRED FUNCTIONS
- Cavity Field Control
- Cavity Resonance Control
- RF Reference generation and distribution
- HPRF protection

- ANTICIPATED NC SYSTEM CONFIGURATIONS
- Single 2.5 MW klystron driving single cavity (402.5 MHz)
- Single 5 MW klystron driving single cavity through a split (805 MHz)

- ANTICIPATED OPERATIONAL & CONDITIONING SCENARIOS
- Pulsed beam, Pulsed RF
- 60 Hz rep rate
- 68% chopping, 36 mA avg

Functional Block Diagram of the Digital Control System



Superconducting Cavity Model

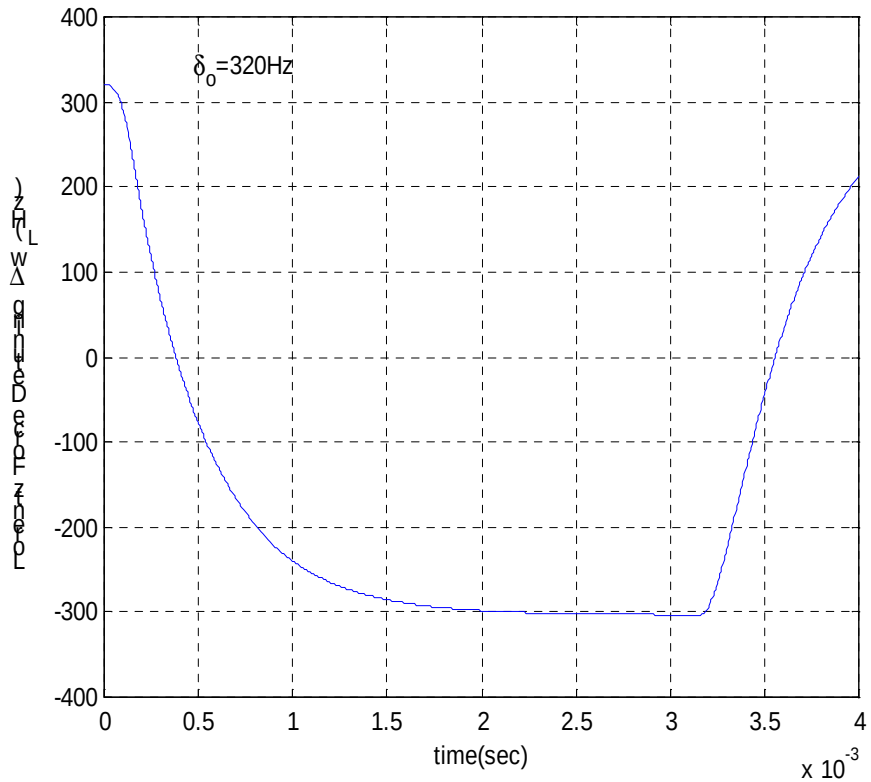
The state space equation of the superconducting model is given by

$$\dot{x} = A(\Delta\omega_L)x + Bu + B_I I$$
$$y = Cx \qquad (1)$$

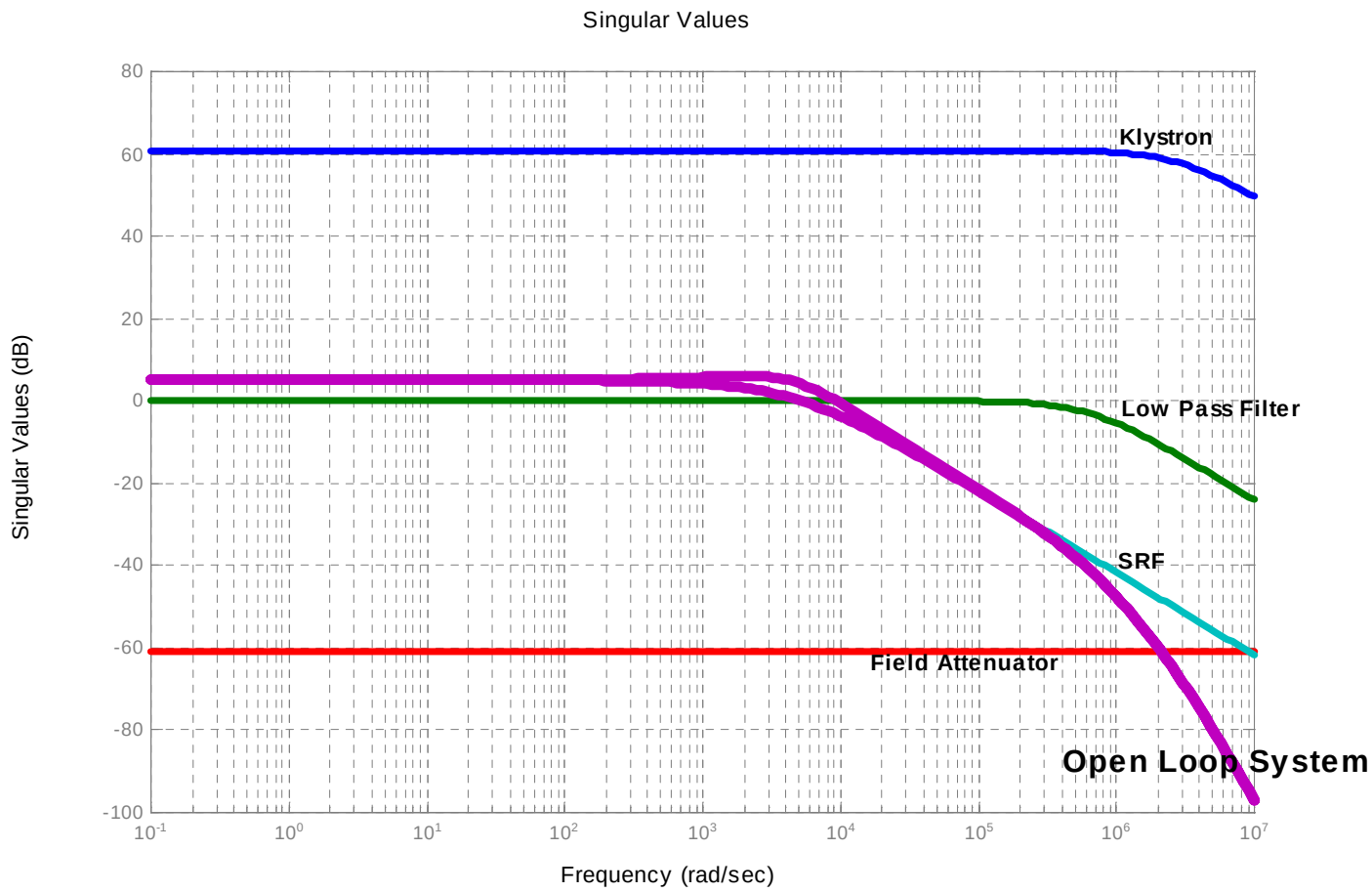
where,

$$A(\Delta\omega_L) = \begin{bmatrix} -\frac{1}{\tau_L} & -(\Delta\omega_m + \Delta\omega_L) \\ (\Delta\omega_m + \Delta\omega_L) & -\frac{1}{\tau_L} \end{bmatrix}$$

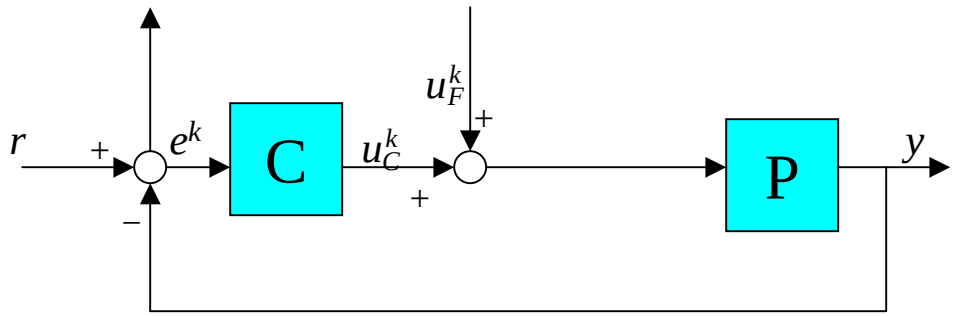
Lorentz Force Detuning of a Superconducting Cavity

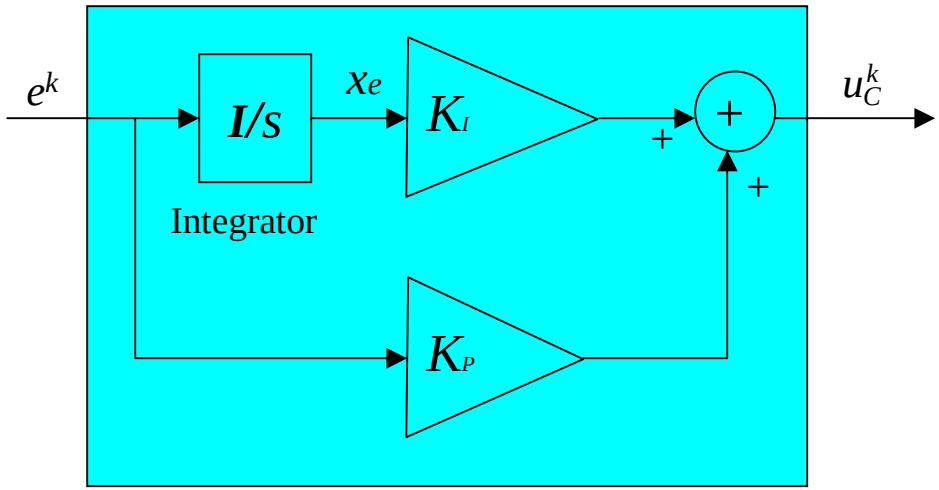


FREQUENCY RESPONSES OF THE OPEN LOOP SYSTEM COMPONENTS



GUI MODELING - PI Controller





GUI MODELING - PI Controller

- Outputs
  - PI Controller Gain Matrices K_P and K_I

Continuous time

$$\dot{x}_e = I_2 e$$
$$u = K_I x_e + K_P e$$

$\Longrightarrow$

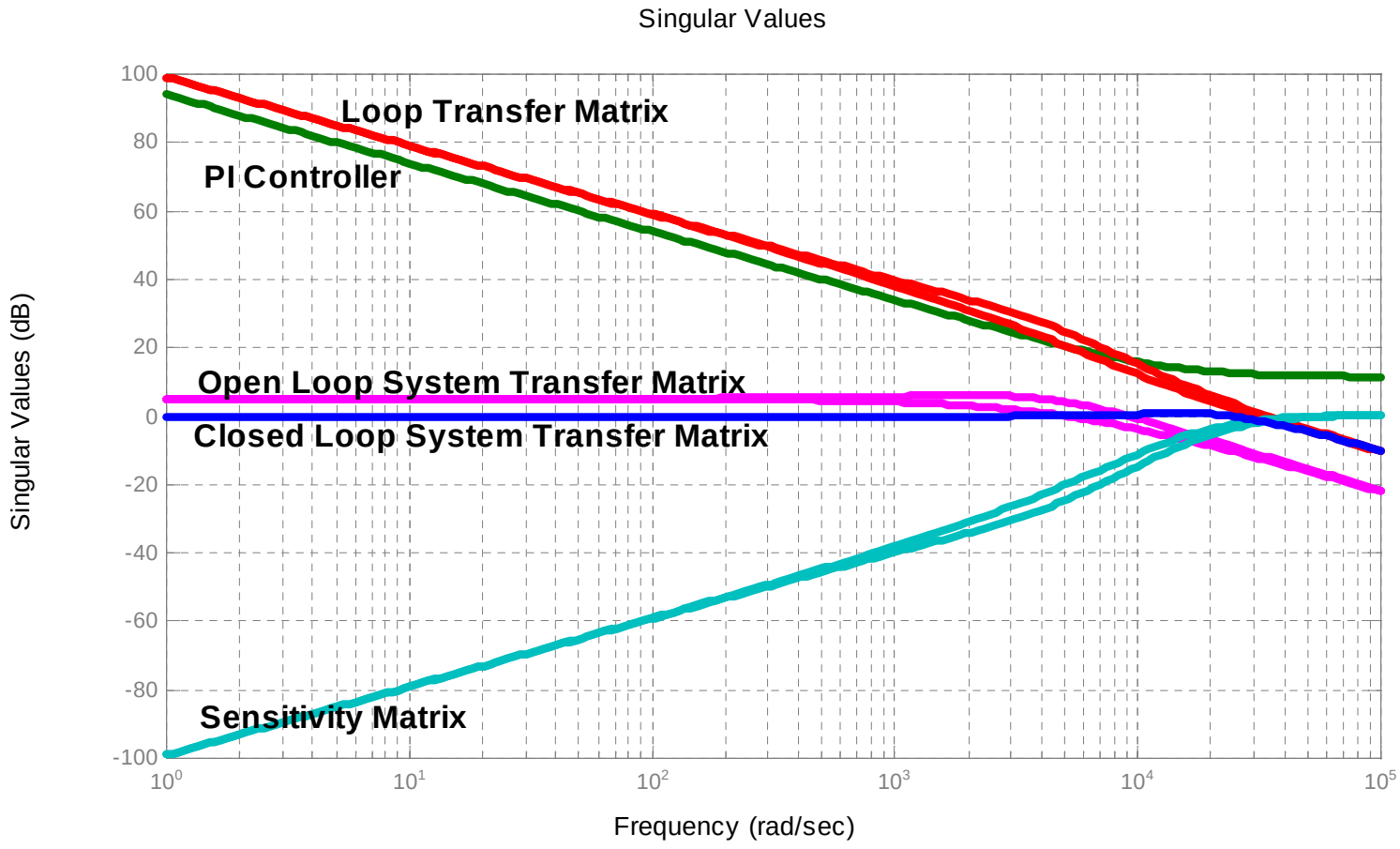
Discrete time

$$x_e(n+1) = x_e(n) + T \cdot e(n)$$
$$u(n) = K_I x_e(n) + K_P e(n)$$

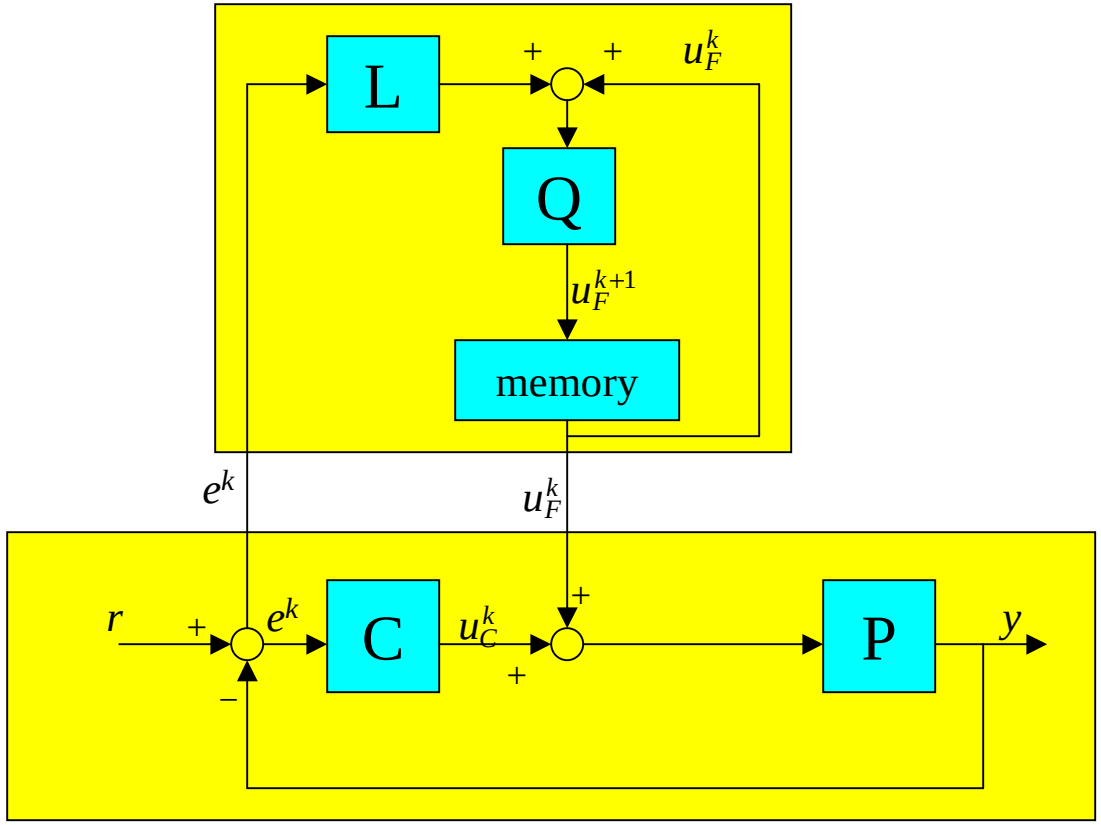
T: sampling time

$$K_I = \begin{bmatrix} k_{I1} & 0 \\ 0 & k_{I2} \end{bmatrix} \qquad K_P = \begin{bmatrix} k_{P1} & 0 \\ 0 & k_{P2} \end{bmatrix}$$

FREQUENCY RESPONSE OF THE PI FEEDBACK CONTROL SYSTEM



GUI MODELING - Iterative Learning Controller (ILC)



GUI MODELING - Iterative Learning Controller

- Iterative Learning Controller

$$U_F^{k+1} = Q\left(f \cdot U_F^k + \alpha \cdot LE^k\right)$$

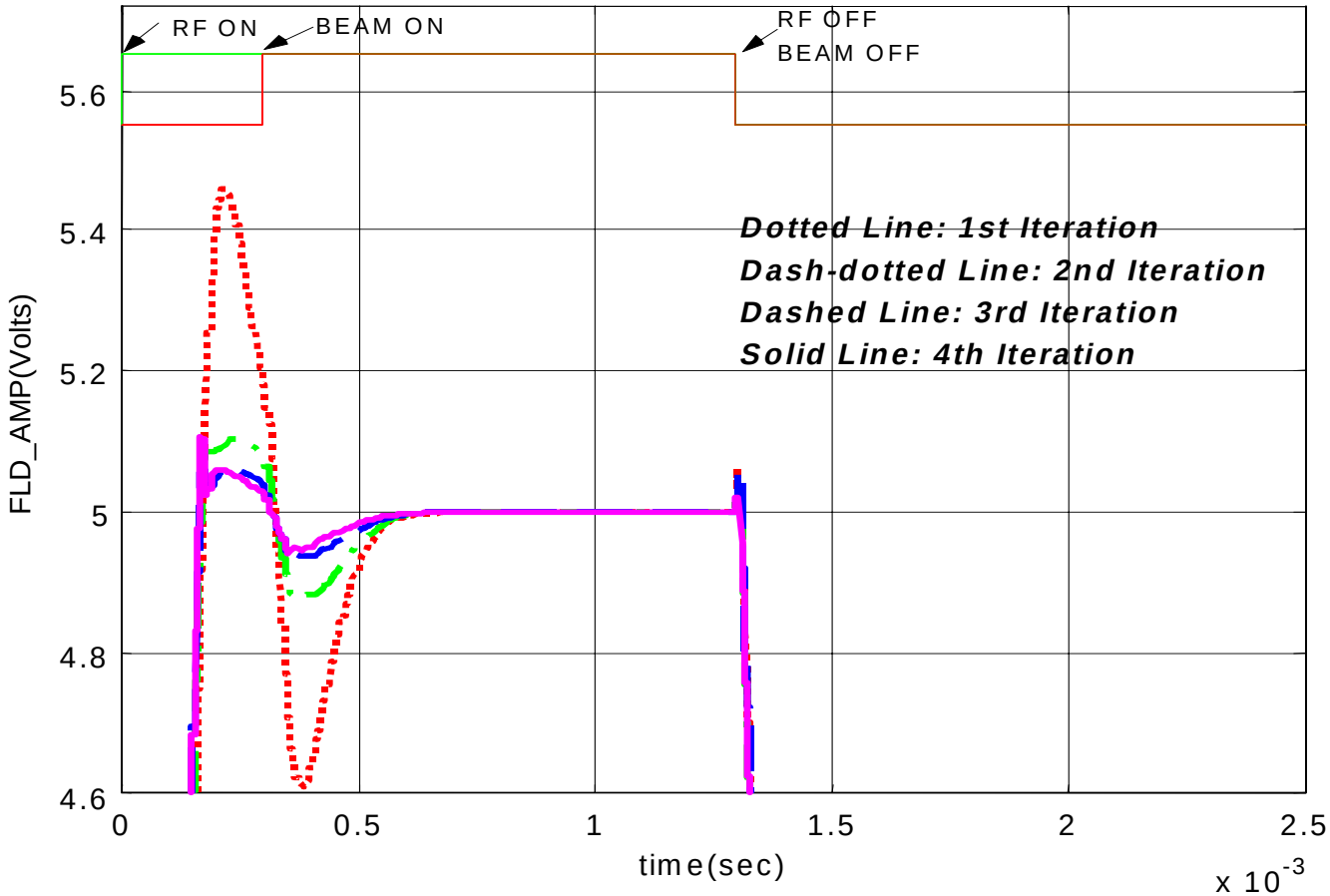
$$0 < f < 1, \qquad 0 < \alpha < 1$$

- Stability and Convergence

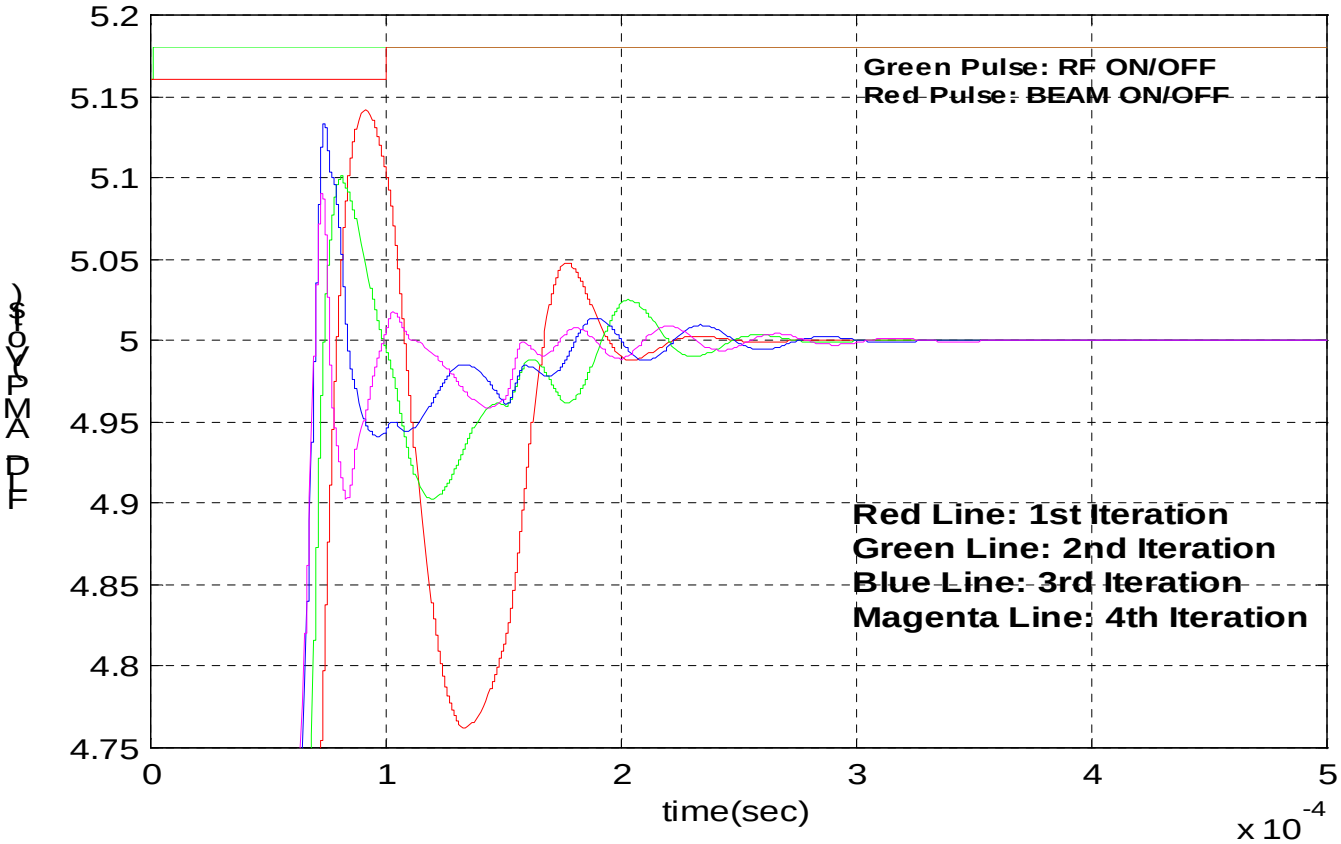
$$\left\| Q\left(f \cdot I - \alpha \cdot LP\,(I + CP)^{-1}\right) \right\|_\infty < 1$$

$$\lim_{k \to \infty} E^k = (I + CP)^{-1} R$$

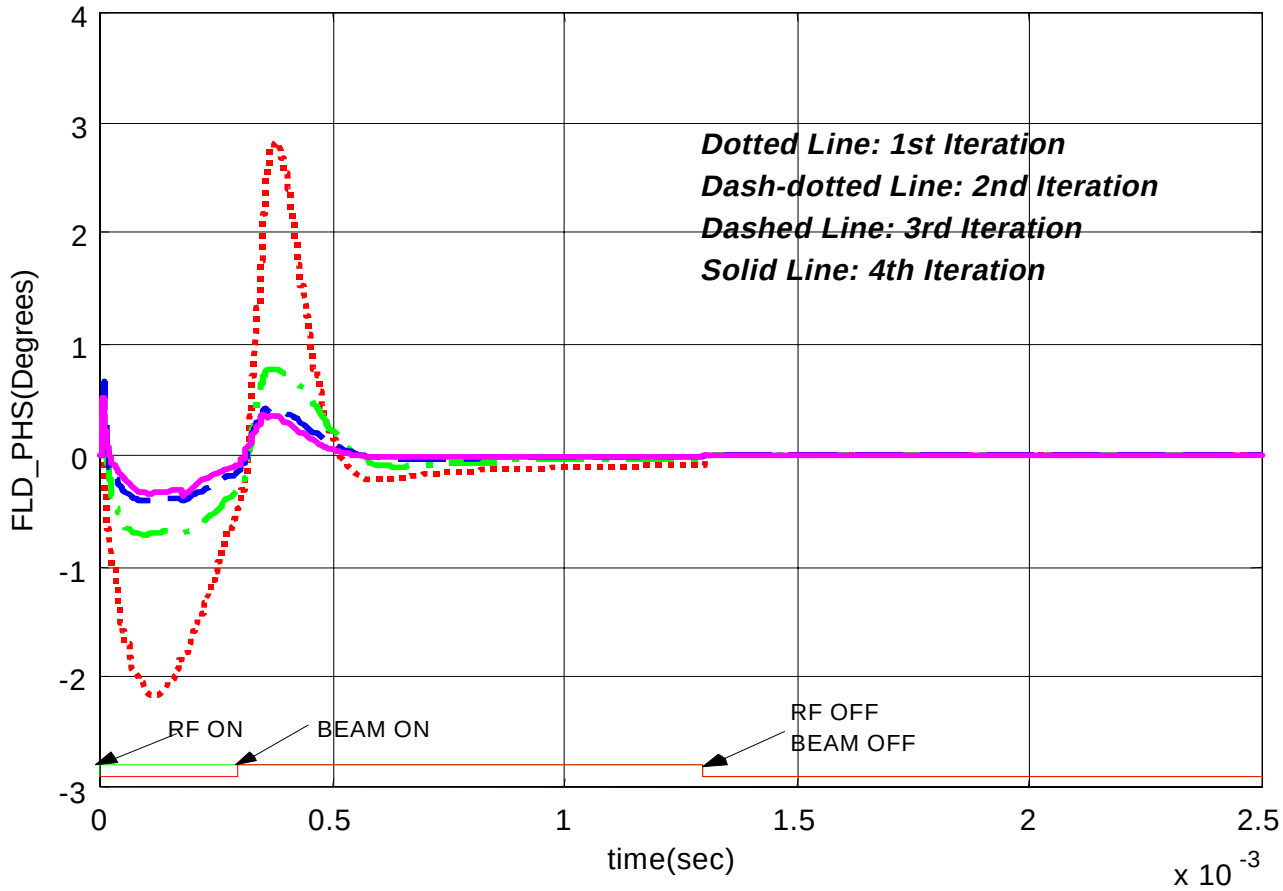
Field Amplitude



Zoom of Field Amplitude



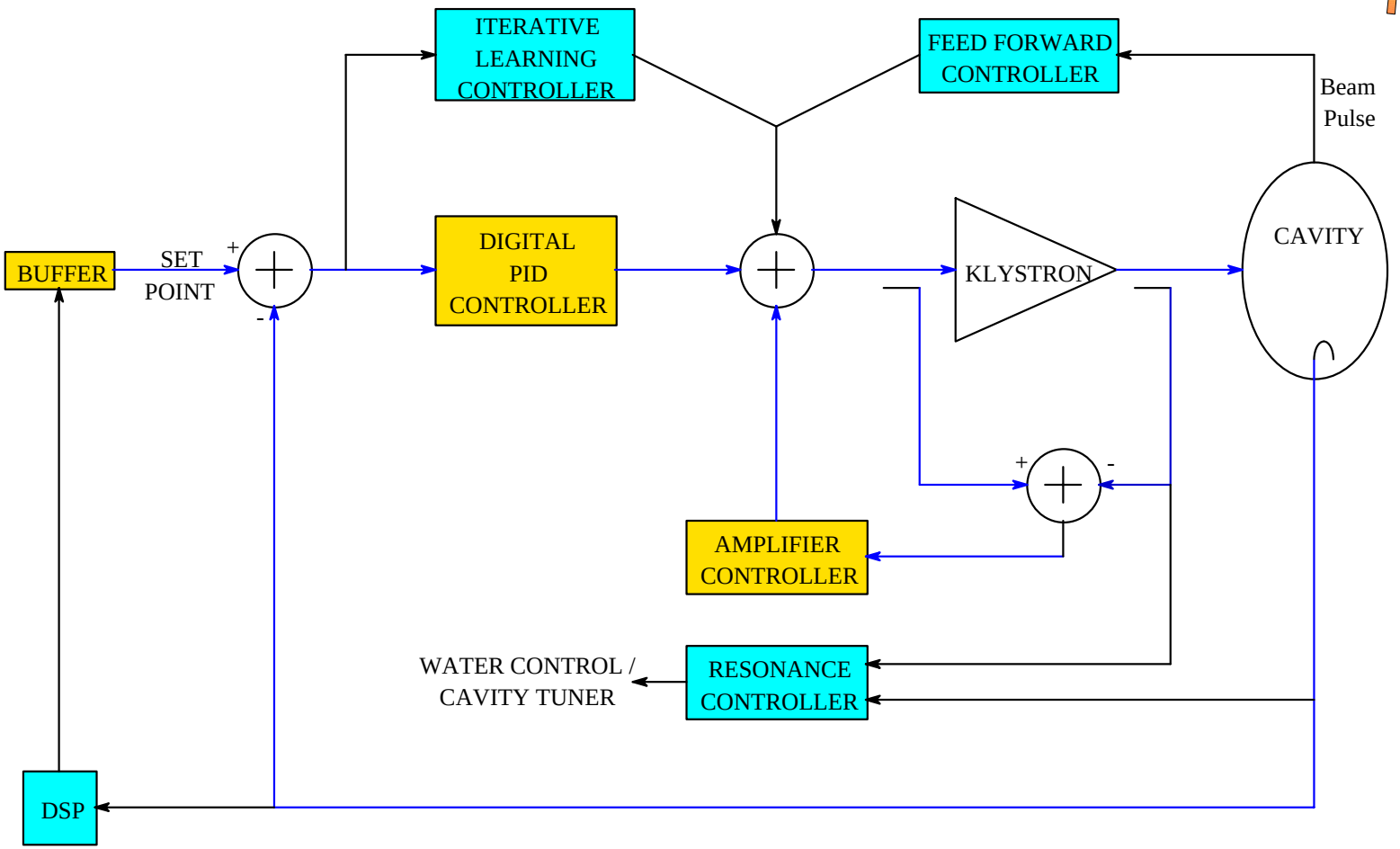
Field Phase


Dotted Line: 1st Iteration
Dash-dotted Line: 2nd Iteration
Dashed Line: 3rd Iteration
Solid Line: 4th Iteration
FLD_PHS(Degrees)
4
3
2
1
0
-1
-2
-3
0
0.5
1
1.5
2
2.5
time(sec)
x 10 -3
RF ON
BEAM ON
RF OFF
BEAM OFF

CONTROL SYSTEM REQUIREMENTS

• Controller Bandwidth:	>20 kHz
• Cavity Field Error:	< ±0.5 % (Amp) < ±0.5^{o} (Phase)
• Latency of the signal path:	1 μs
• Controllers:	PID, Feed-Forward and other modern controllers.
• Operation Mode:	Pulsed
• Calibration:	Real time auto calibration (beam off for a few pulses)

Functional Block Diagram of the Digital Control System



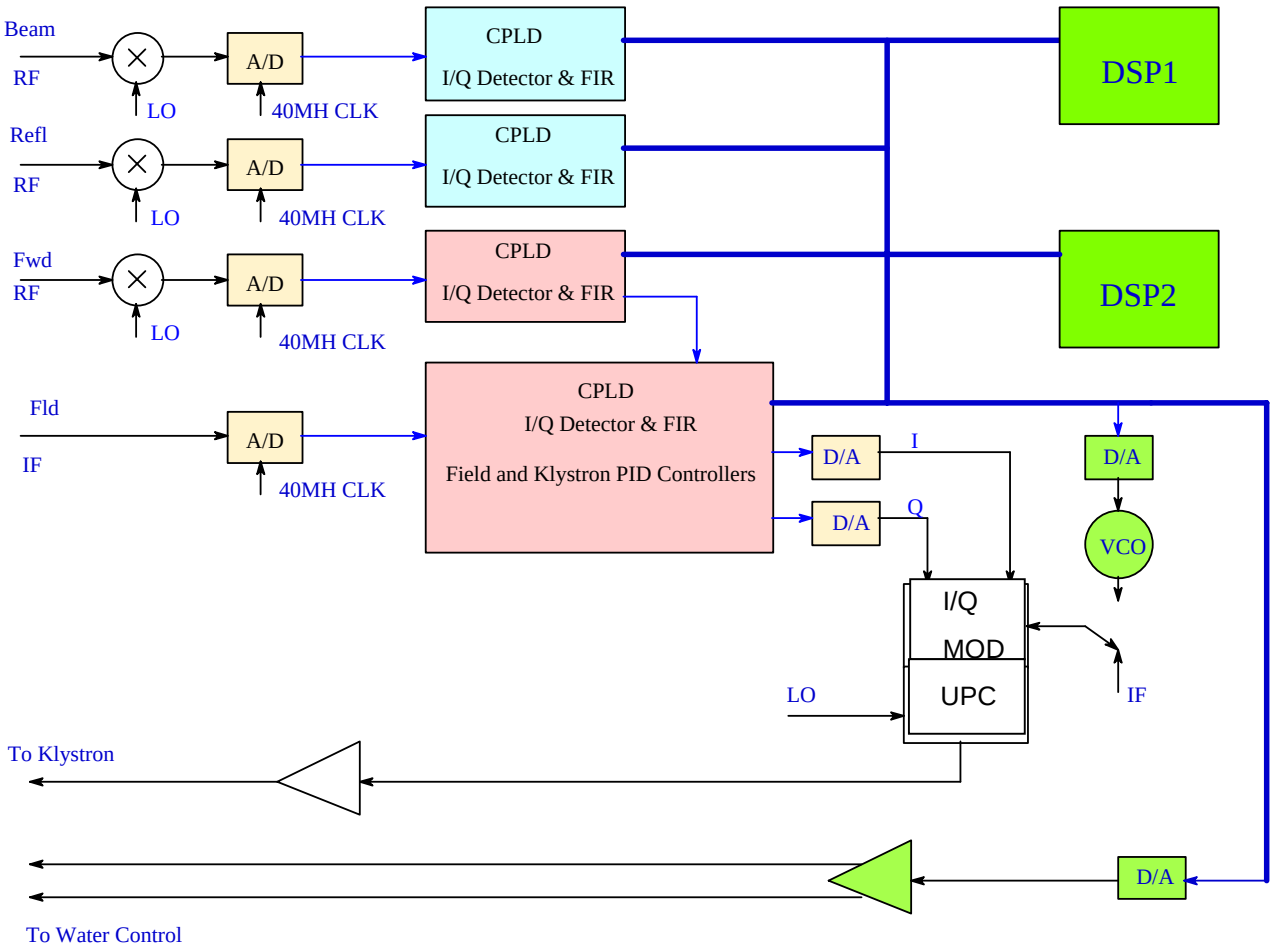
SYSTEM ARCHETECTURE OF FIELD AND RESONANT CONTROL MODULE FOR SNS LLRF

- A General Purpose MotherBoard Which provides VXI interface and Bus arbitration function for DSP and Front-Plug in board and could host two DSP plug-in boards and two Front-plug-in boards;
- Two DSPs: One DSP for Resonance Control and other for Field Control (adaptive feed forward and gain scheduling);
- One front-end-board for all RF I/O and Digital I/Q demodulation and fast digital control processing (Field control, resonant control and beam feed forward).
- Multi-rate digital processing in CPLD for optimized though-put in fast field control signal path.

Digital Control Board Functions and I/O

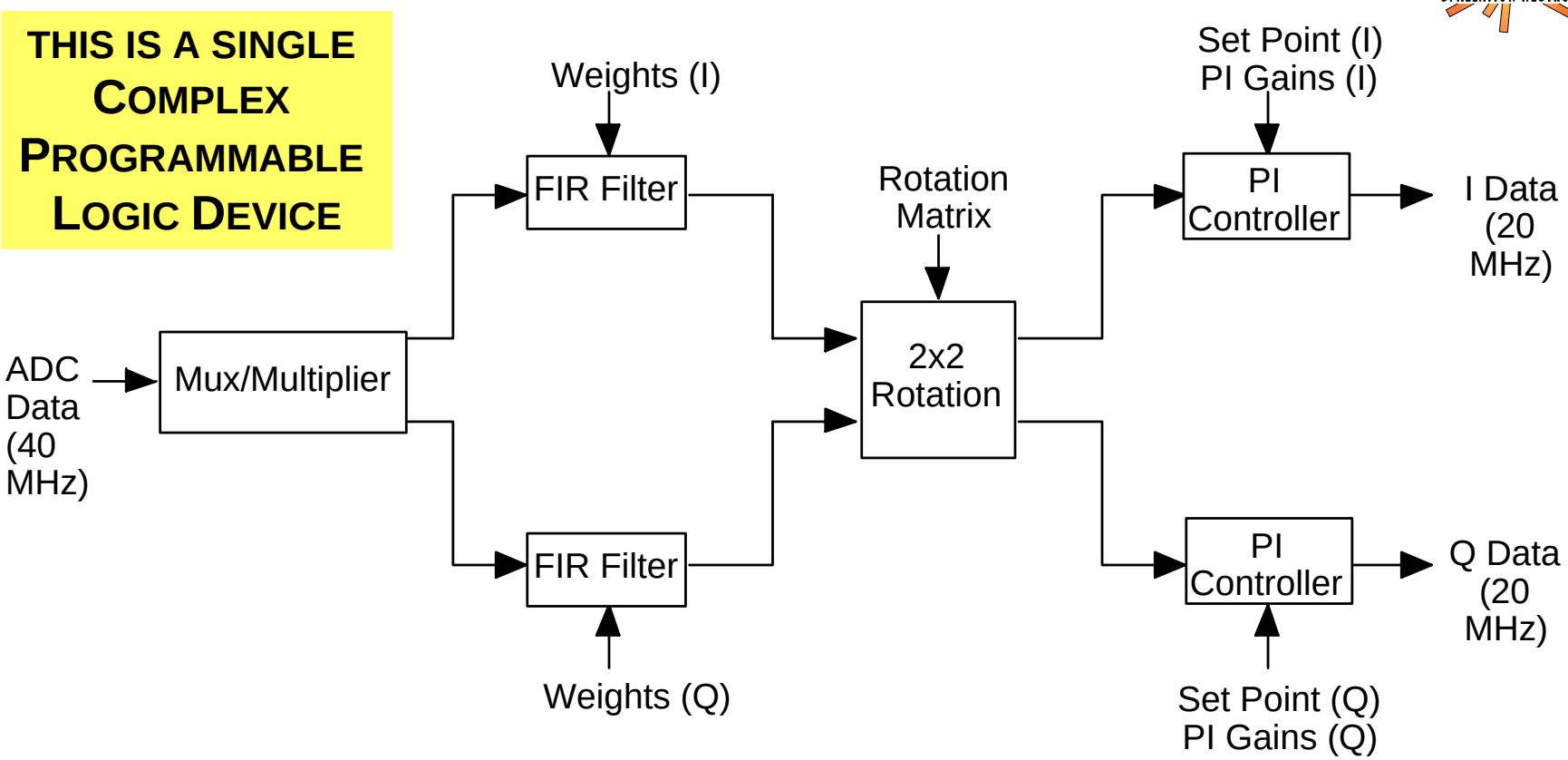
- Functions:
  - Field Control
  - Resonant Control
  - Beam Feed Forward
  - Klystron Control
- Input Signal:
  - Cavity field (IF 50MHz)
  - Forward field (RF)
  - Reflected field (RF)
  - LO and IF (50MHz)
  - Beam (RF)
- Output Signal:
  - RF to Klystron
  - Analog differential signal to water resonant control

Digital Control Module Block Diagram



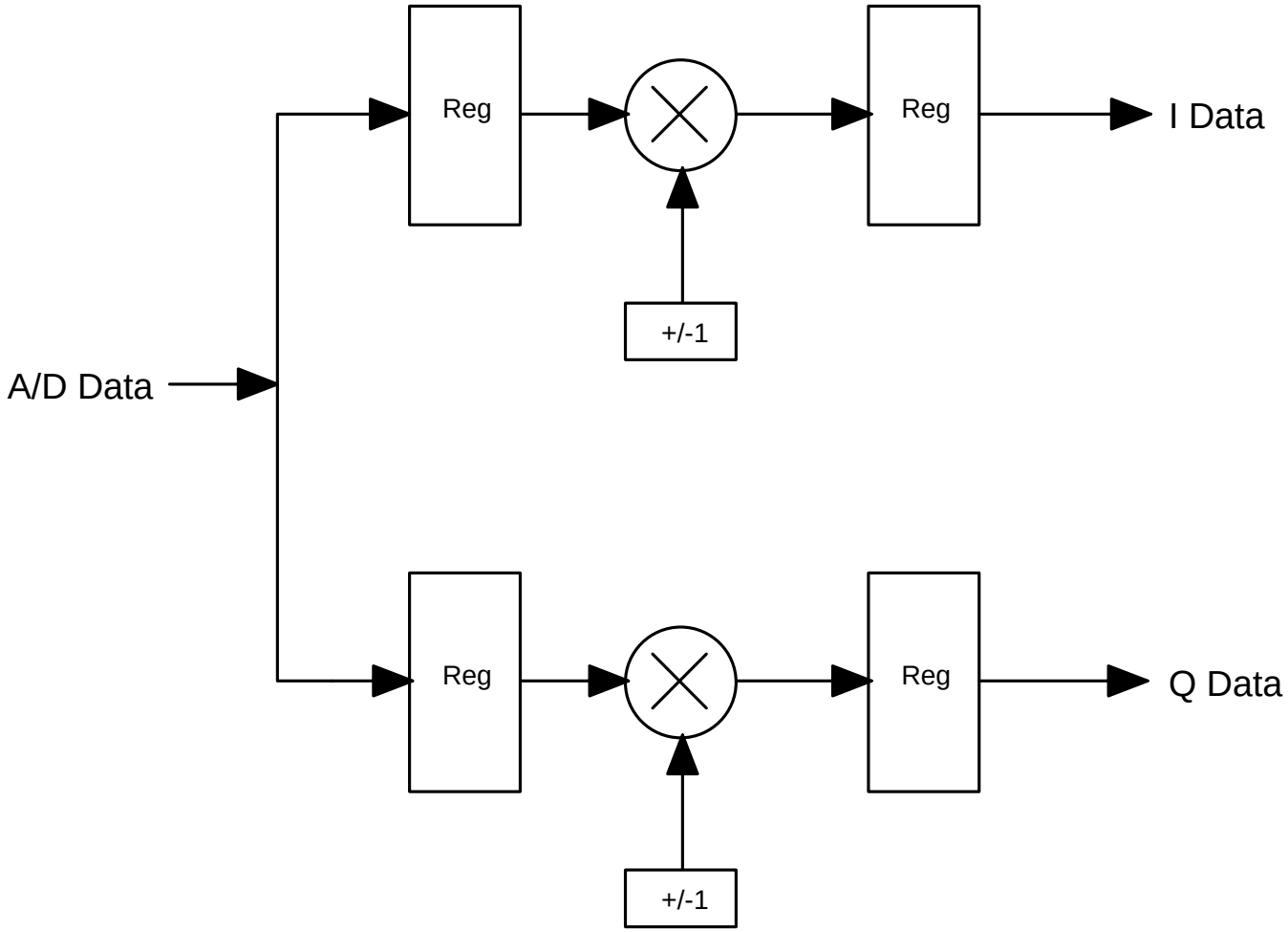
Fast Signal Processing (CPLD) Architecture

THIS IS A SINGLE COMPLEX PROGRAMMABLE LOGIC DEVICE

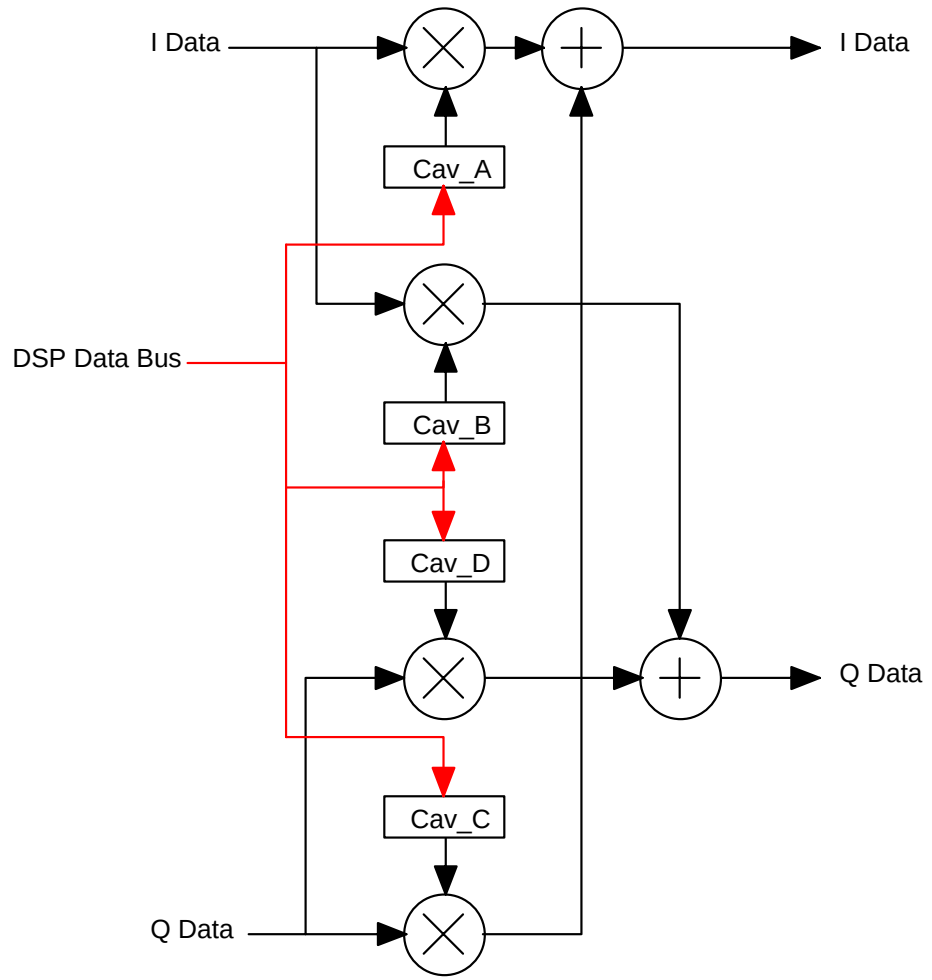


Delay	1	17	1	1	20 cycles
Latency	1.5	1	0	1	3.5 cycles

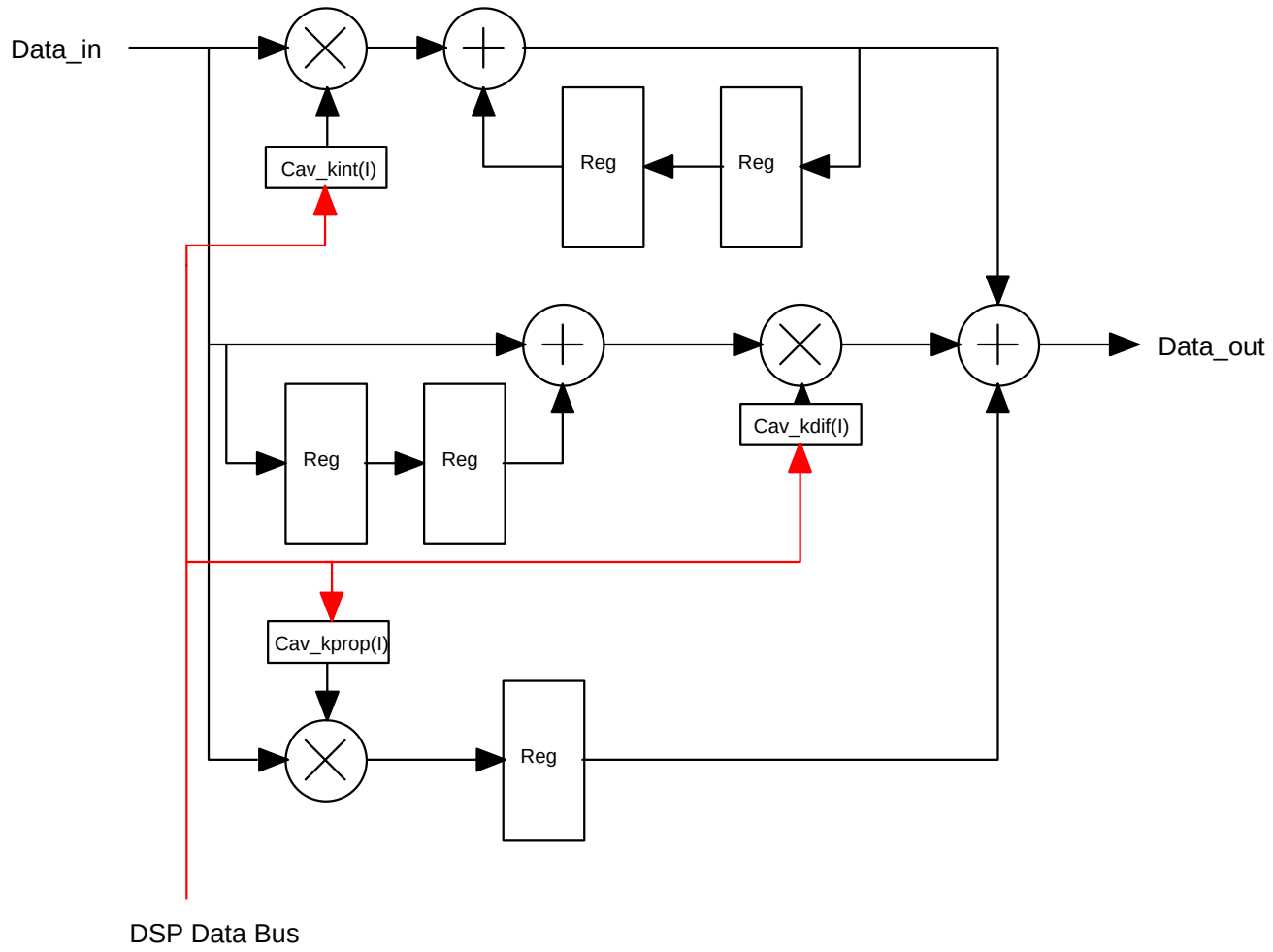
I/Q DEMODULATOR



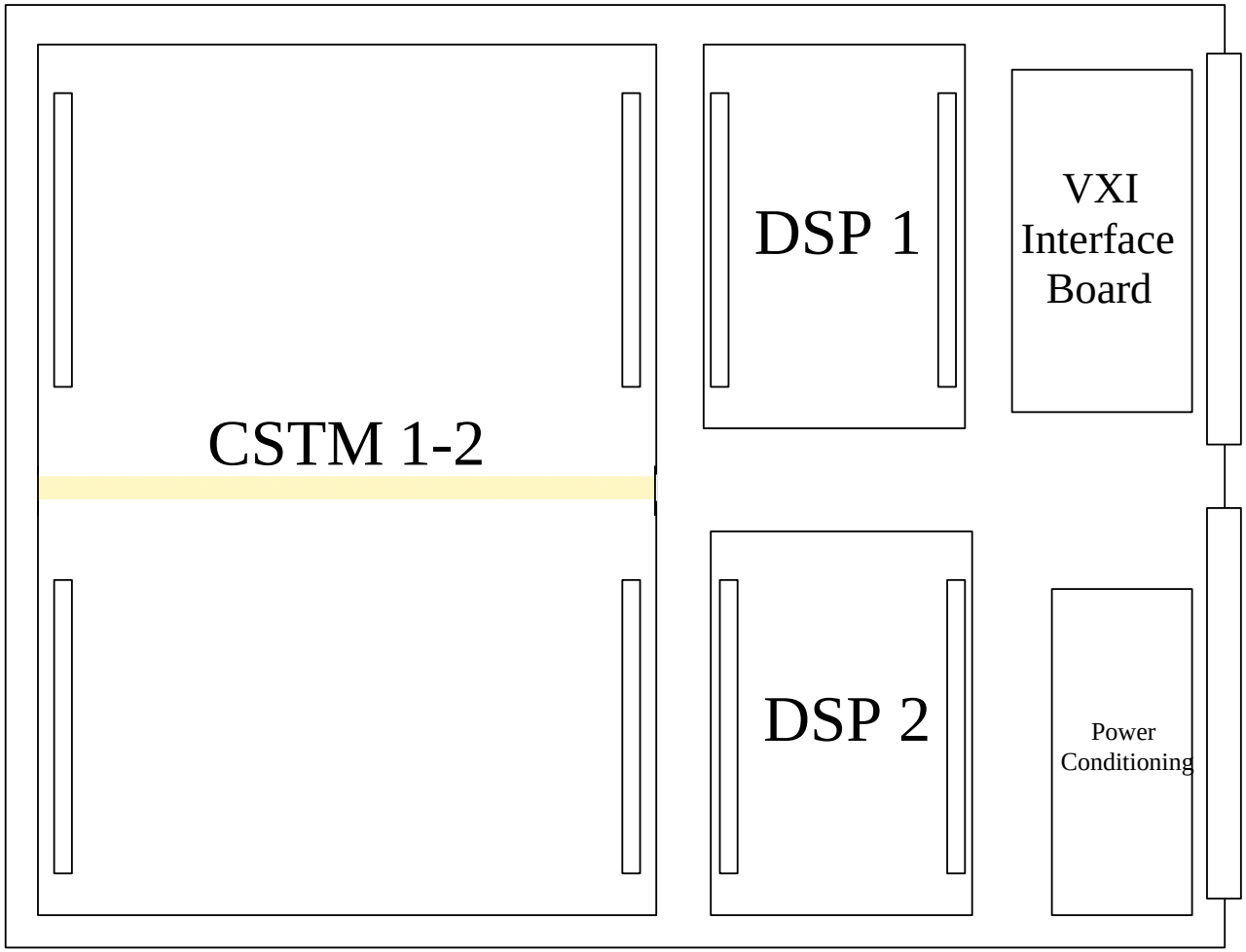
ROTATION MATRIX



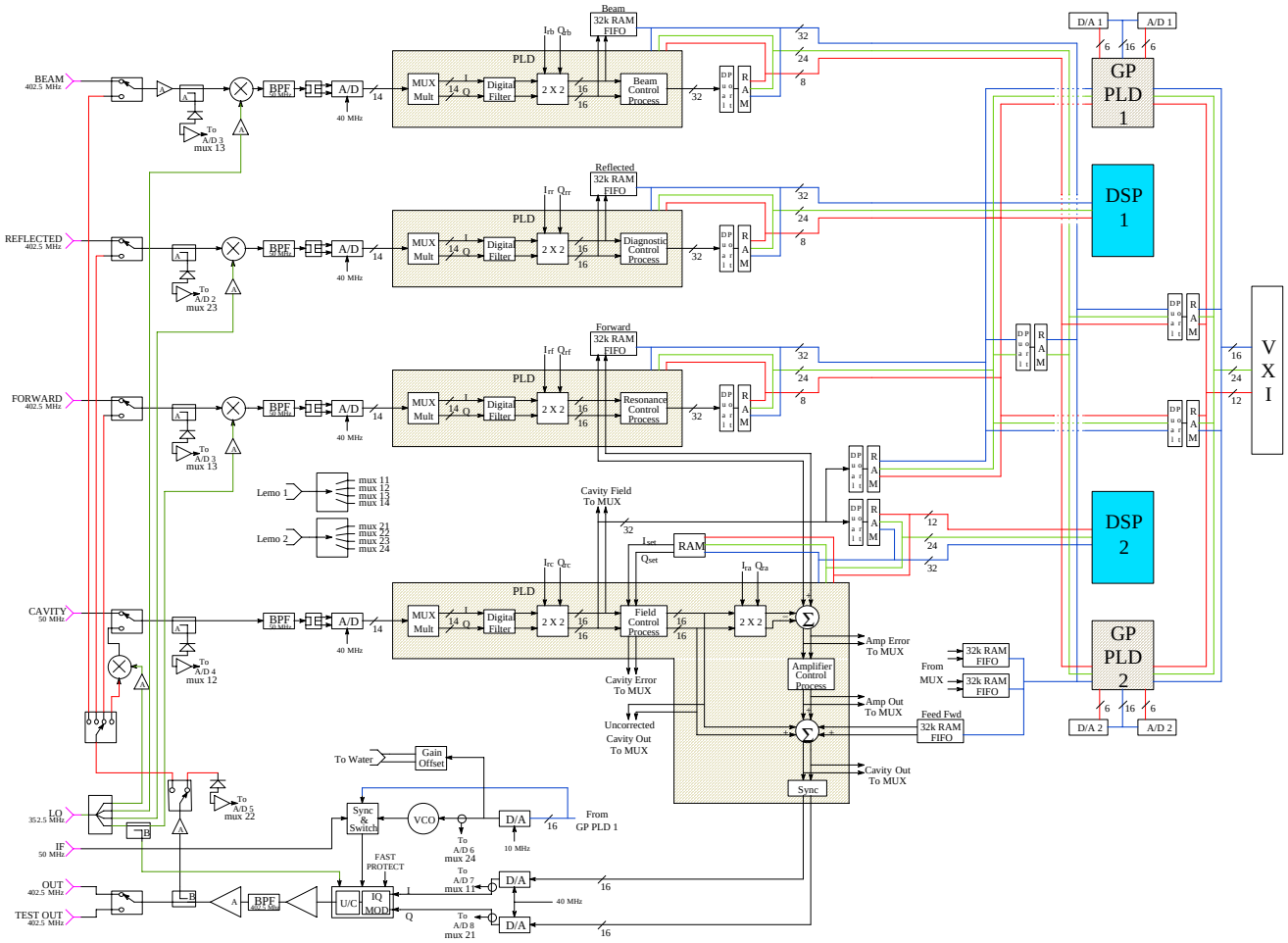
BLOCK DIAGRAM OF DIGITAL PID CONTROLLER



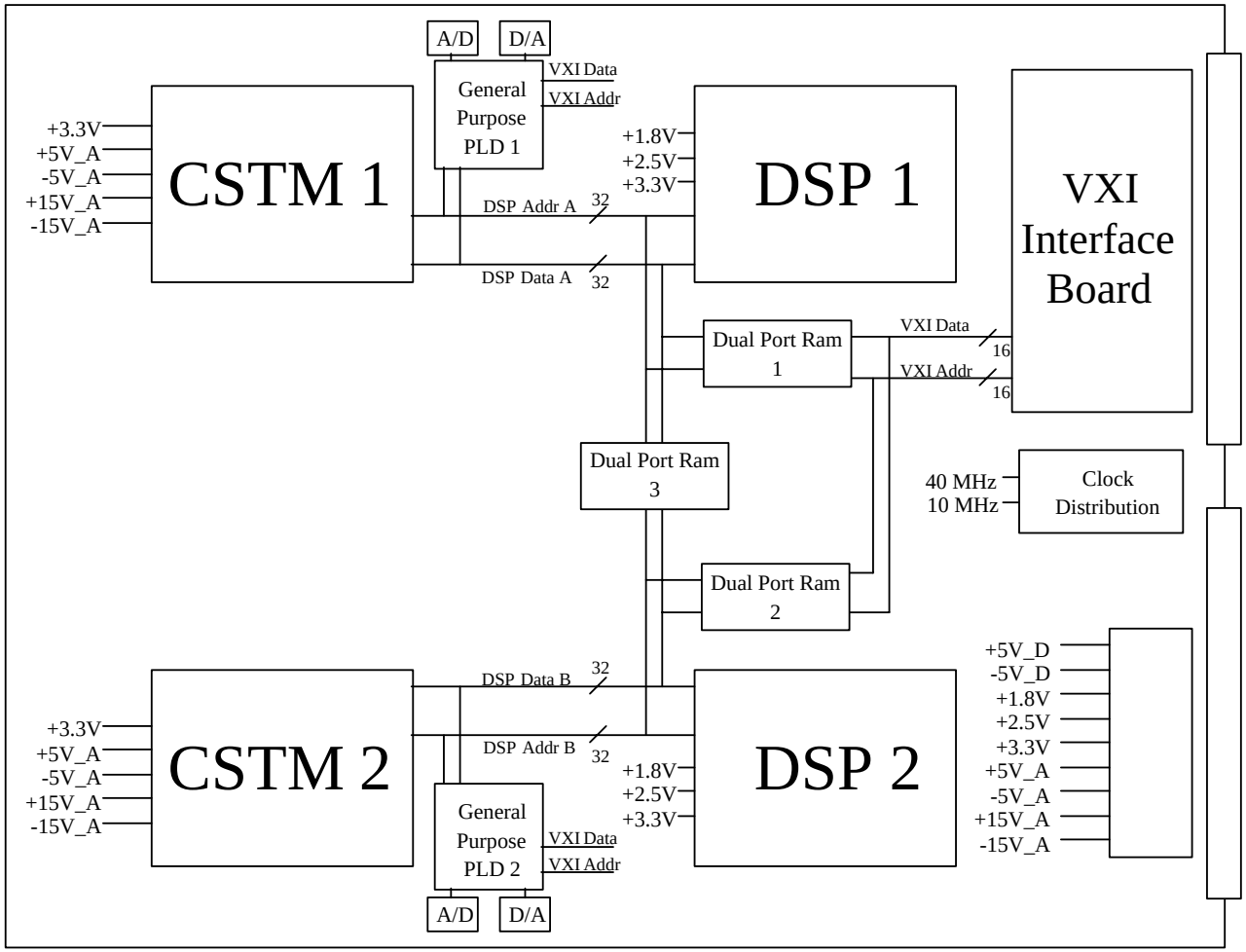
Mother Board Layout



Control Board Layout



Motherboard Block Diagram



Fast Signal Processing Timing

- Inherent Filter Delay = 20 cycles (50 ns) = 1000 ns
- Processing Latency = 3.5 cycles (50 ns) = 175 ns
- Total time = 23.5 cycles (50 ns) = 1175 ns

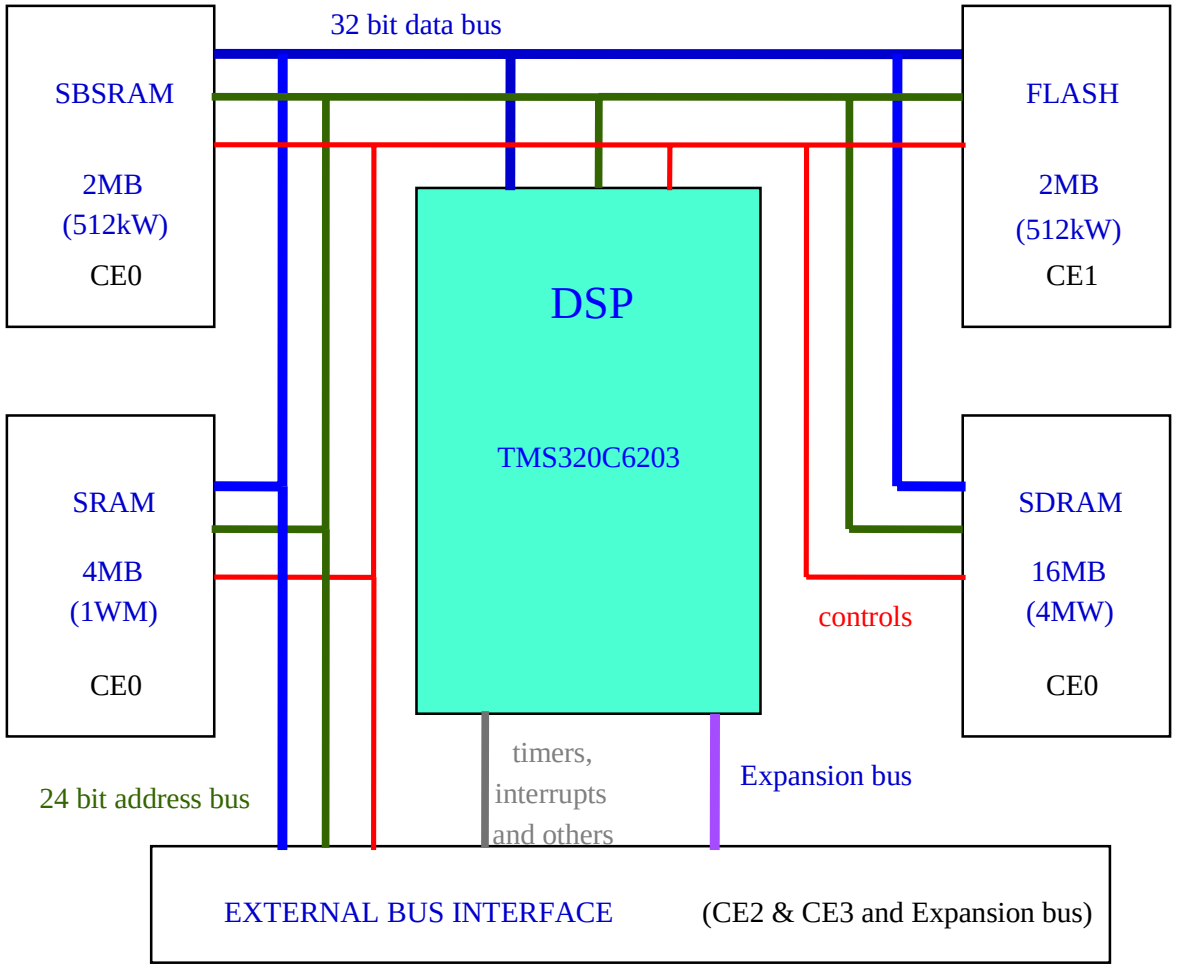
Fast Signal Processing

- Standard PLD Family
  - Altera 20KE Series
  - 672 FineLine BGA Package
  - 20K30E through 20K1500E devices available
  - Cost Estimate
    - EP20K300E - $360.00 ($322.00 – 230.00)
    - EP20K1000E - $1740.00 ($1218.00 – 870.00)

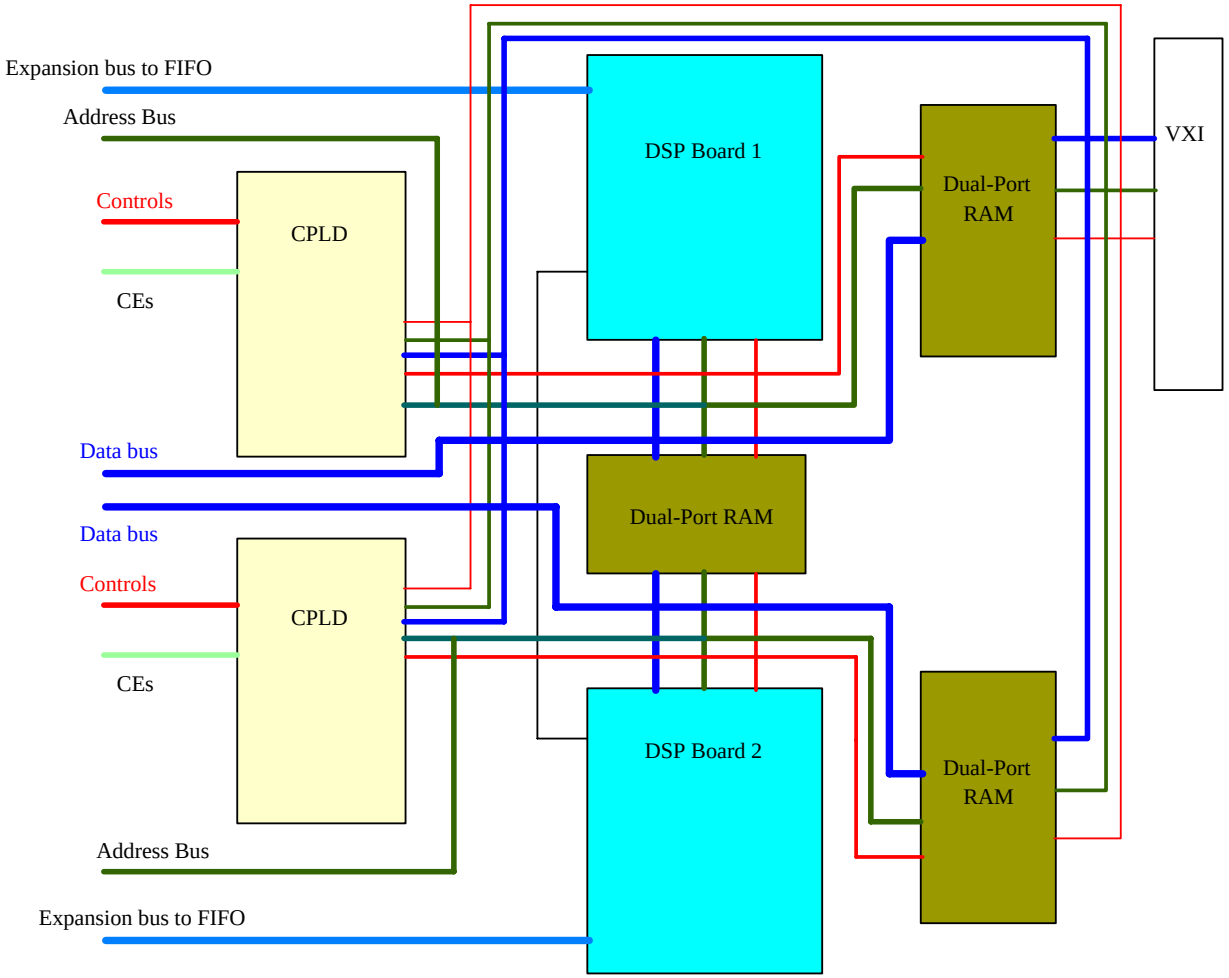
TMS320C6203 Specs

- Fixed point DSP with a clock rate over 200MHz
- VelociTI Advanced VLIW ’C62x CPU Core
  - 8 highly independent Functional Units: 6 ALU and 2 Multipliers
  - All instruction conditional
  - Byte addressable
- On-chip SRAM (7M-bit)
- 32-bit external memory interface (EMIF)
- DMA controller
- Flexible PLL clock generator
- 32-bit expansion bus
- Multichannel buffered serial ports

DSP Board Block Diagram



DSP Board Interfaces



SUMMARY

- Full digital implementation of the RF control system for both the normal conducting and superconducting system;
- Proposed an adaptive feed-forward algorithm to suppress the repetitive noise;
- Resonance control algorithm based on the full field measurement of both the forward and cavity fields;
- SIMULINK/MATLAB simulation is performed to verify the proposed algorithms and implementations;
- Hybrid CPLD/DSP implementation for both speed and computational power.