Outline

- Receiver Applications & Topology
- Conventional Analog Receiver
  - Digital Receiver
    - Digital Quadrature Sampler
    - Digital Processing
    - Digital LO Synthesis
- Applications
- Conclusion
Receiver Applications

- Wireless Voice Communication
  - Radio, Television
  - Cellular, PCS, Military Communication
  - Cordless Phones

- Wireless Data Communication
  - Bluetooth LANs

- GPS

- LLRF
  - RF Signal Measurement
  - Beam Signal Measurement
Digital Receiver Constellation

QAM Radio Reception using ZT400VXI
75 MHz IF, 500 MSPS, 12-Bit Digitizer
Receiver Topology

- Downconversion Mixer(s)
- Local Oscillator(s)
- Demodulator
  - I/Q, Amplitude/Phase, Amplitude
- Baseband Processor
  - Filtering, Synchronization, AGC, LLRF
Conventional Analog Receiver

Sources of Error

- **Conversion Loss Variation**
- **Amplitude Balance**
- **90° Phase Balance**
- **DC Noise and Offset Drift**
Digital Receiver

Sources of Error

- Reduced Conversion Loss Variation
- Perfect Amplitude Balance
- Perfect Phase Balance (at $f_c$)
- Zero DC Noise and Offset Drift
Digital Demodulator

Digital I/Q Demodulator

Direct I/Q Sampling
Direct I/Q Sampling Time Domain

ADC

1:2 DEMUX

 +/-1 MULTIPLIER

LO CLK

INPUT SIGNAL

SAMPLING: $f_s = 4 \times f_C$

DECIMATION BY 2

MULTIPLY BY +/- 1

DIGITAL FILTER
Direct I/Q Frequency Domain

(a) ADC
(b) DEMUX
(c) +/-1 MULTIPLIER
(d) +/-1 MULTIPLIER
(e) Q

INPUT SPECTRUM

(b) SAMPLING: \( f_s = 4 \times f_c \)

(c) DECIMATION BY 2

(d) MULTIPLY BY +/- 1

(e) DIGITAL FILTER
Under-Sampling Downconversion

(a) ADC

(b) SAMPLED IF

(c) LO CLK

IF

SAMPLED IF

LO CLOCK

IF INPUT

SAMPLED IF

$3f_s - f_c$ $f_c - 2f_s$ $4f_s - f_c$ $f_c - f_s$ $5f_s - f_c$ $f_c$
Direct I/Q Sampling Details

Sources of Error
- Quadrature Phase Errors Away From $f_C$
- Unaliased Data if $\Delta f < \pm f_S/8$
- Time Jitter $\rightarrow$ Phase Error Relative to IF

Under-Sampling Sample Rates
- $f_S = 4f_C/(2n+1)$ where $n$ is a positive integer

Analog-to-Digital Converters
- Analog Bandwidth $> f_C$
- Low Sampling Aperture Jitter
- Examples:
  - CLC5958, 52 MSPS, 14-Bit, 210 MHz
  - AD6644, 65 MSPS, 14-Bit, 250 MHz
  - AD9433, 125 MSPS, 12-Bit, 750 MHz
  - SPT7760, 1 GSPS, 8-Bit, 900 MHz
  - MAX108, 1.5 GSPS, 8-Bit, 2200 MHz
Digital Baseband Processing

Processing Functions
- Filtering – IIR, FIR, Matched Filters
- Decimation
- Carrier Recovery & Tracking
- Symbol Synchronization and Decoding
- Error Detection & Correction
- Automatic Gain Control
- Signal Measurement ($E_b$, Polar, FFT)
- Signal Modification (Control System)
Processing Device Comparison

![DEVICE COMPARISON](chart.png)

CPLD/FPGA
FIXED DSP
GENERAL DSP

- **SPEED**
- **FLEXIBILITY**
- **DENSITY**
- **LOW COST**
Digital Processing Devices

CPLD / FPGA
- Altera, Xilinx, Quick-Logic, Actel, etc.

Fixed-Purpose DSP
- HSP50210 – Digital Costas Loop
- HSP50110 – Digital Quadrature Tuner
- HSP43220 – CIC FIR Filter
- MAX2101 – Quadrature Digitizer
- AD6620 – Decimating Receiver
- CLC5902 – Digital Downconverter

General-Purpose DSP
- Texas Instruments, Analog Devices, etc.

Baseband Processors
- Philips, Intel, Motorola, Qualcomm, etc.
Digital LO Synthesis

LO Sinusoid for Downconversion Mixing
- Translates IF to Direct I/Q Sampling Frequency
- Must be Phase-Locked to Reference

LO Sampling Clock
- Direct I/Q Sampling Frequency
- Must be Phase-Locked to Reference

Reference Clock
- Must Be Integer Subharmonic of All LOs !!!
Synthesizer Topologies 1

**Numerically Controlled Oscillator (NCO)**

- **FREQ. REGISTER**
- **SINE ROM**
- **LO OUT**

**Direct Digital Synthesizer (DDS)**

- **FREQ. REGISTER**
- **SINE ROM**
- **DAC**
- **RECONSTRUCT FILTER**
- **LO OUT**
- **REF CLK**
Synthesizer Topologies 2

Phase Locked Loop (PLL)

DDS-Driven PLL
Synthesizer Topologies 3

DDS-Offset PLL

DDS Modulator
Synthesizer Devices

- ADF4113 – PLL, 4 GHz
- LMX2326 – PLL, 2.8 GHz
- MC12179 – PLL, 2.8 GHz
- SA8016 – PLL, 2.5 GHz
- MC145193 – PLL, 1.1 GHz
- TRF2050 – PLL, 1.1 GHz
- HSP45102 – NCO, 40 MHz
- AD9852 – DDS, 300 MHz
- ISL5314 – DDS, 125 MHz
- HSP45116 – NCO Modulator, 52 MHz
- AD9854 – DDS Modulator, 300 MHz
Digital Receiver Applications

Quadrature Demodulators
- SLAC 8-Channel I/Q Demodulator Module
  - Direct Quadrature Sampling
  - CIC-FIR Filter Fixed-Function DSP
- LANL Field Control Module
  - Direct Quadrature Sampling
  - CIC-FIR Filter Fixed-Function DSP
  - General Purpose TMS320C50 DSP

LO Synthesizer
- SLAC Clock Synthesizer Module
  - Triple PLL Synthesizer

Digital Radio
- SNL/LANL/Honeywell Telemetry Receivers
- LANL Underground Radio Transceiver
Conclusion

The Technology is Available Today for Implementing LLRF Systems using Digital Receivers, Processors, and Transmitters

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