DSG-RICH R&D Meeting Minutes

Date: February 5, 2021
Time: 11:00AM – 12:00PM

Attendees: Peter Bonneau, Aaron Brown, Pablo Campero, Brian Eng, Tyler Lemon, Marc McMullen, and Amrit Yegneswaran

1. Reviewed RICH-II planning meeting with INFN collaborators and Hall B

2. RICH-II interlock system
   - 2.1. SHT-35 alert and reset pins will not be used
     - 2.1.1. Alert pin is a built-in capability to send a 3.3 VDC signal to controller, which is unneeded because interlock program performs monitoring and interlocking of sensor
     - 2.1.2. Reset pin allows simple soft-reset of SHT-35; able to perform soft-reset through I^2C command, making reset pin unneeded

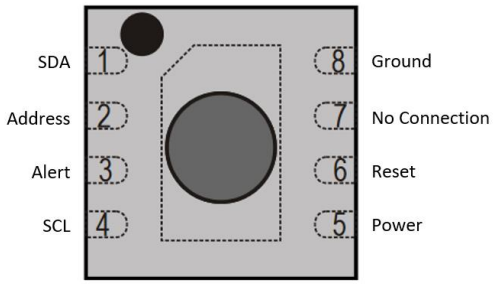

Fig. 1: SHT-35 pin out

   - 2.2. Each sensor used will have independent I^2C communication lines to prevent problems reading out other sensors on the same bus if a sensor fails
     - 2.2.1. One sbRIO can read 24 sensors; multiplexers will be investigated to allow more sensors to be read by one sbRIO

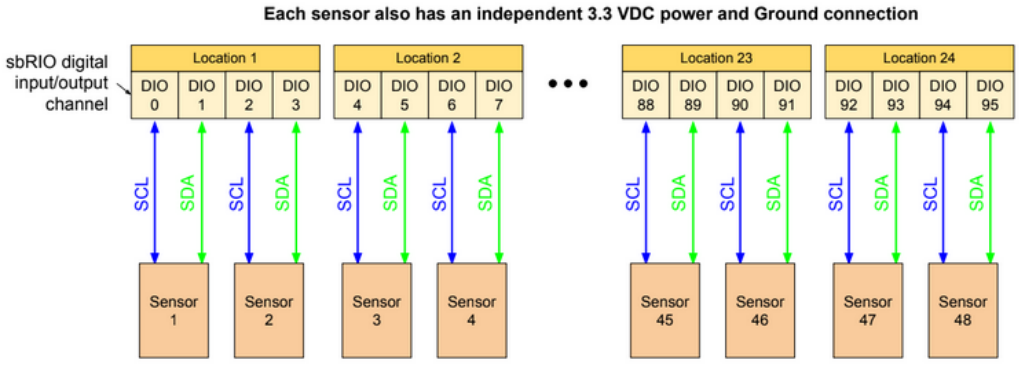

Fig. 2: Diagram showing each sensor with its own I^2C communication lines. Each sensors' independent 3.3 VDC power and ground not shown.