DSG-RICH R&D Meeting Minutes

Date: February 19, 2021
Time: 11:00AM – 12:00PM

Attendees: *Peter Bonneau, Aaron Brown, Pablo Campero, Brian Eng, George Jacobs, Tyler Lemon, Marc McMullen, and Amrit Yegneswaran*

1. RICH-II interlock system ordered items received; waiting for new JLab work-from-home policy to pick up items

2. Tyler Lemon will make a timeline for hardware interlock system development

3. Hardware interlock RIO mezzanine card (RMC)
    - 3.1. RMC will have a buffer driver for each sensor, a connector to attach RMC to sbRIO, relays for enabling/disabling CAEN power supply, and connections to backplane PCB of interlock chassis
        - 3.1.1. Backplane PCB has 3.3 V power distribution and RJ-45 connectors for each sensor location
    - 3.2. Researching whether circuit would need barrier diodes
        - 3.2.1. Tyler Lemon will simulate circuit to see how it behaves with and without diodes

4. SHT35 sensor board
    - 4.1. Created sketch of PCB needed for SHT35 sensor board
    - 4.2. Investigating whether pull-up resistors are needed for clock and data lines on input side of buffer driver
    - 4.3. Tyler Lemon will model heat generated by components in Ansys to ensure heat dissipated by buffer drivers will not affect sensor readout