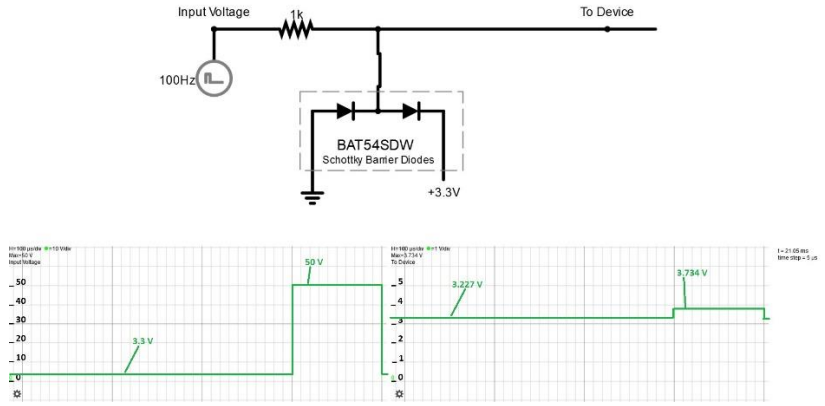
DSG-RICH R&D Meeting Minutes

Date: February 26, 2021
Time: 11:00AM – 12:00PM

Attendees: Peter Bonneau, Aaron Brown, Pablo Campero, Brian Eng, George Jacobs, Tyler Lemon, Marc McMullen, and Amrit Yegneswaran

1. Reviewed timeline of RICH-II hardware interlock system development
    1.1. Timeline in talk posted on DSG Website

2. Hardware interlock RIO mezzanine card (RMC)
    2.1. Peter Bonneau and Tyler Lemon are determining what circuits and connections are needed
    2.2. Interlock relay power and control components
        2.2.1. Relays will trip CAEN HV/LV mainframe on an interlock condition
        2.2.2. Reviewing specifications of sbRIO analog outputs and digital output to see which should drive relay
    2.3. Schottky barrier diodes will protect circuit components from over- and under-voltage conditions
        2.3.1. Placement of barrier diodes to be determined
        2.3.2. Circuit simulator shows that for both positive and negative voltage spikes, barrier diodes in series and connected to 3.3 V and ground will keep voltage to device between ~0 V and ~3.3 V.



Circuit simulator schematic and voltage plot results for an over-voltage example with Schottky barrier diodes. Input voltage to circuit modeled to behave as a 50 V spike on a 3.3 V signal. During spike, voltage to device only increases from 3.227 V to 3.734 V.

3. SHT35 sensor board
    3.1. Marc McMullen started schematic lay-out of PCB in Altium; goal is to make as small as possible
    3.2. Cable connection point to PCB being investigated
        3.2.1. Molex's Pico-Clasp connector a possibility, but is ~5 times taller than any other PCB component
        3.2.2. Searching for smaller profile connector, or will solder cable leads directly to PCB