DSG-RICH R&D Meeting Minutes

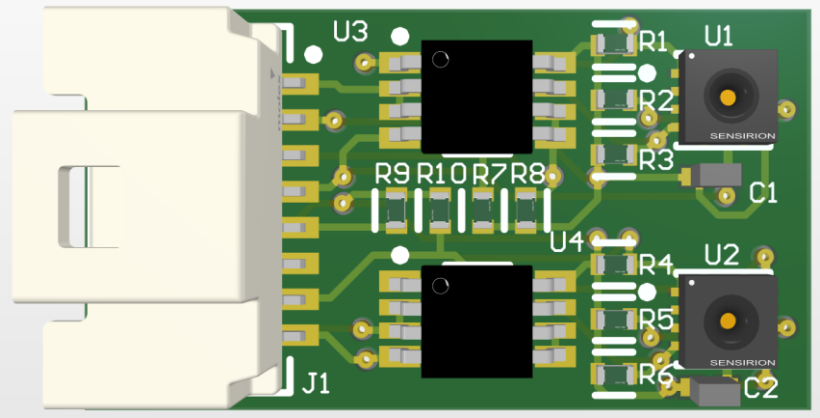
Date: March 12, 2021
Time: 11:00AM – 12:00PM

Attendees: Peter Bonneau, Aaron Brown, Pablo Campero, Brian Eng, George Jacobs, Tyler Lemon, Marc McMullen, and Amrit Yegneswaran

1. **Discussed previous RICH-II meeting with INFN and Hall B collaborators**
   DSG
   - Detector shell shipment in hands of courier; expected delivery of late April 2021
   - New dry cabinet has shipped from factory; expected delivery of March 27, 2021

2. **Upgrade of mirror reflectivity test station**
   DSG
   - DSG will compile parts list for upgraded test station, including two compact spectrometers, fiber-optic reflectivity probe, stabilized light source, and mechanical structure to align and hold components securely at mirror

3. **Reviewed second iteration of SHT35 sensor board design**
   Peter Bonneau, Aaron Brown, Pablo Campero, Brian Eng, Tyler Lemon, and Marc McMullen
   - Ground and power planes added and sensors moved further away from buffer driver

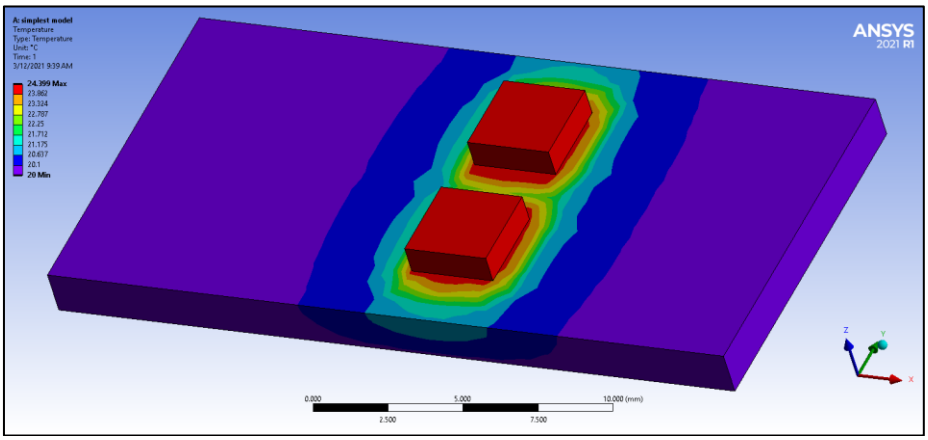


Altium 3D rendering of second board iteration.

4. ANSYS temperature analysis of SHT35 sensor board

Tyler Lemon

- Analysis modified to use internally-generated heat for each buffer driver and to apply convection to stagnant air for all items in model
  - Previous analysis used heat flow through faces of buffer driver models and did not have convection
  - With convection applied, distance between SHT35 sensors' placement decreased from 0.22" to 0.21"



ANSYS simulation result when internal heat generation of ~22 mW applied to buffer drivers. Distance where temperature increase from ambient heat is at or less than 0.1° C is 0.21".

- Next steps in ANSYS analysis
  - Time-dependent heat generation by buffer drivers, more closely modeling real-world behavior
    - During typical operation, buffer drivers are only held low for ~1 ms per data acquisition
  - Analysis using Altium-generated 3D model
    - Model used would be exact layout of PCB
- Inquired if the lab's license includes access to SIwave and Icepak packages, specifically for thermal analysis of PCBs; waiting for reply
  - Packages allow entire PCB design (versus just a solid model) to be imported from Altium
  - After importing, voltage sources and current sinks can be applied to components and simulation ran to show power dissipation and thermal mapping on a layer-by-layer basis

5. RICH interlock system hardware block diagram completed

Mary Ann Antonioli and Tyler Lemon

- Block diagram shows hardware components of interlock system's chassis, and data paths for one SHT35 sensor and internal interlock chassis monitoring