

## DSG-RICH R&D Meeting Minutes

**Date: April 23, 2021**

**Time: 11:00AM – 12:00PM**

*Attendees: Mary Ann Antonioli, Peter Bonneau, Aaron Brown, Pablo Campero, Brian Eng, George Jacobs, Tyler Lemon, Marc McMullen, and Amrit Yegneswaran*

### **1. Prototyping of SHT35 readout circuit**

*Tyler Lemon and Marc McMullen*

- Determined capacitance of flat CAT7 cable procured for prototyping is ~30 pF/foot
  - Capacitance determined by using oscilloscope to measure RC time constant of circuit with cable (acting as capacitor) in series with a 1-k $\Omega$  resistor
- Pull-up resistors should be ~300  $\Omega$  on clock and data lines between buffer drivers
  - [Talk presented on subject](#)
- Generated Bill of Materials
- Will order fabrication of five PCBs of first design

### **2. sbRIO RMC and backplane PCB design sketches**

*Mary Ann Antonioli, Peter Bonneau, Brian Eng, Tyler Lemon, and Marc McMullen*

- Modified RMC Serial Data – Serial Clock Circuit diagram to have one ground connection for every data line on J2 (Fig. 1)
  - Originally, SCL was paired with 3.3 V, but since backplane PCB was changed to get 3.3 V power from external power supply, the 3.3 V at J2 is unneeded.
- Modified RMC Backplane PCB Circuit diagram (Fig. 2)
  - A. On J1, changed 3.3 V lines to ground connections
    - Corresponds to change made to RMC on Fig. 1
  - B. Added J30 for connecting external 3.3 V power supply
    - Originally, 3.3 V came from J1 connector, but since all of those 3.3 V connections were changed to ground connections, PCB needed a connection to external 3.3 V power supply.
  - C. Added R3 and R4 for RJ-45's LEDs
    - LEDs typically need current limiting resistors, so added them to PCB in case RJ-45 port does not have them built in.

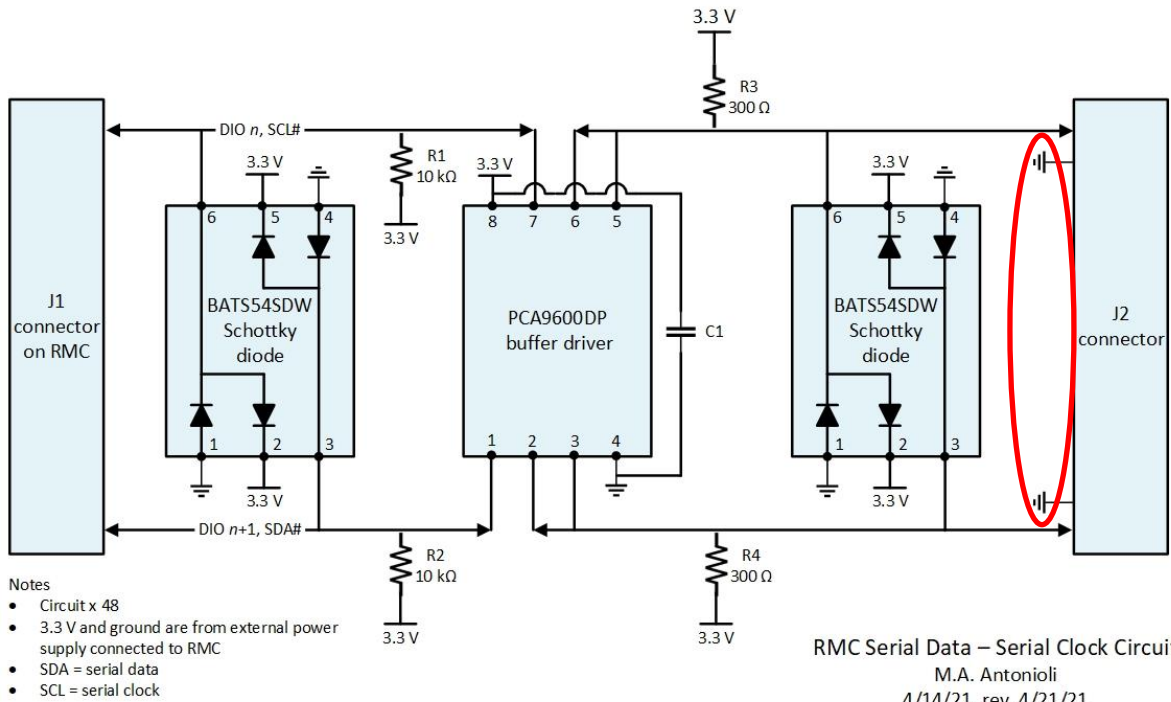
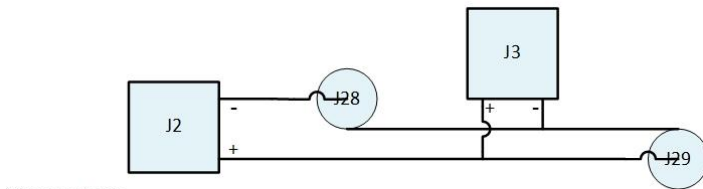
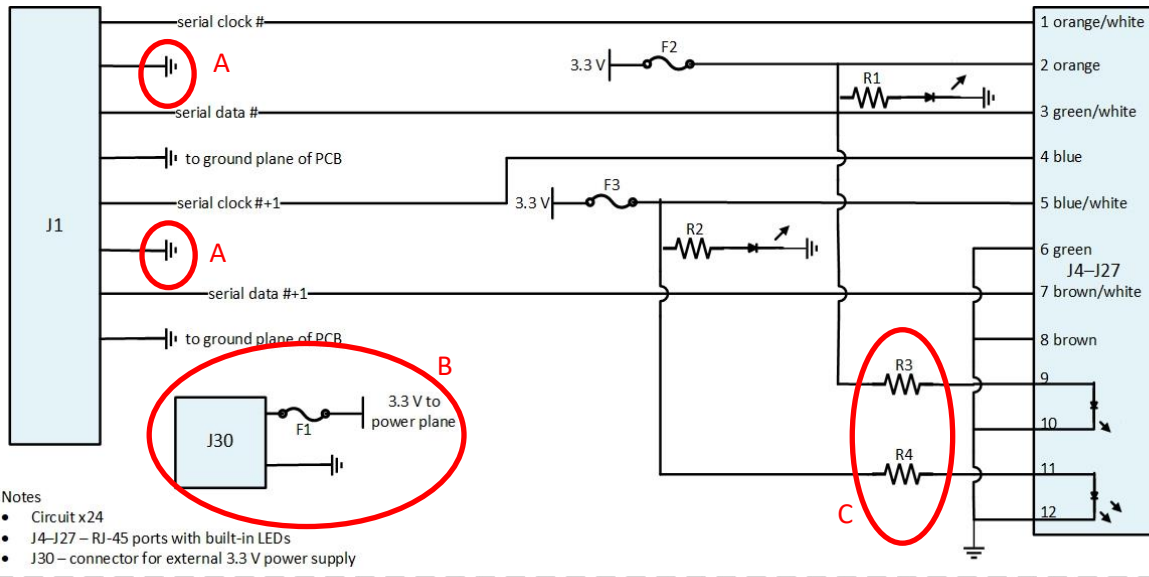


Fig. 1 RMC's I<sup>2</sup>C circuit for one sensor



- Connector Notes
- J2 – from RMC interlock out
  - J3 – from override switch
  - J28 – 00-sized feedthrough for daisy-chaining to external cRIO
  - J29 – 00-sized port feedthrough for connection to CAEN mainframe

RMC Backplane PCB Circuit  
M.A. Antonioli  
4/16/21 rev. 4/21/21

Fig. 2 Backplane PCB diagram