

DSG Moller

Date: 04/05/2023

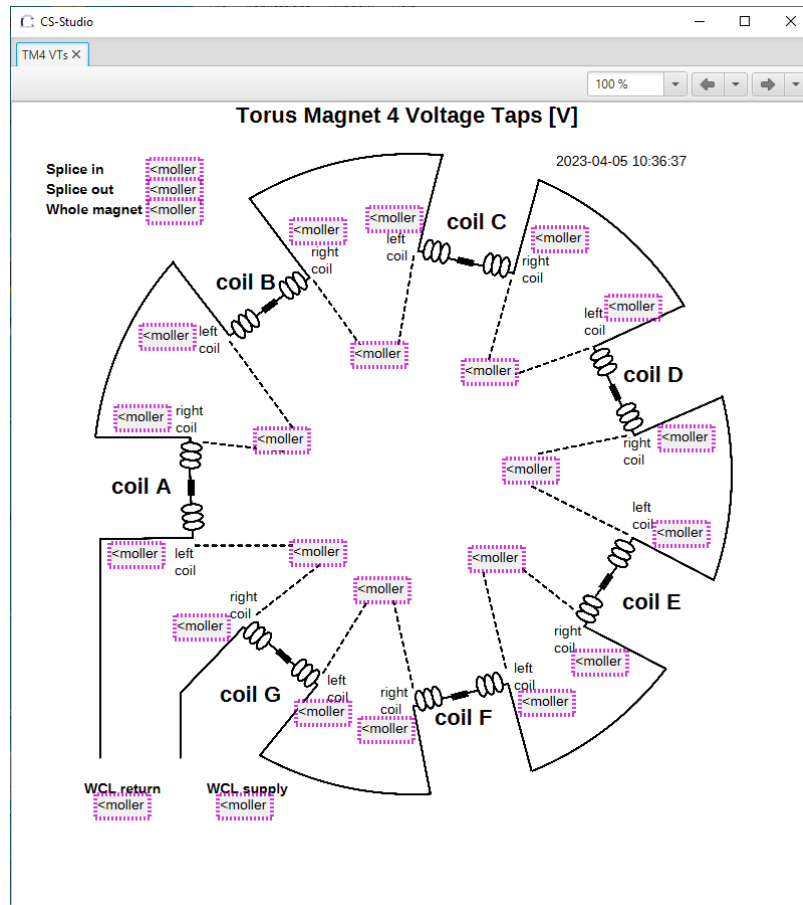
Time: 11:00 – 12:00

Attendees: Peter Bonneau, Aaron Brown, Pablo Campero, Brian Eng, Kaiyi Hall, Tyler Lemon, Marc McMullen

1. Phoebus Screens

Mary Ann Antonoli, Brian Eng

1. Completed temperature screens based on P&ID for magnets 1–4
2. Completed voltage taps screens based on P&ID for magnets 1–4; magnet 4 shown as example



3. Created overview voltage screen

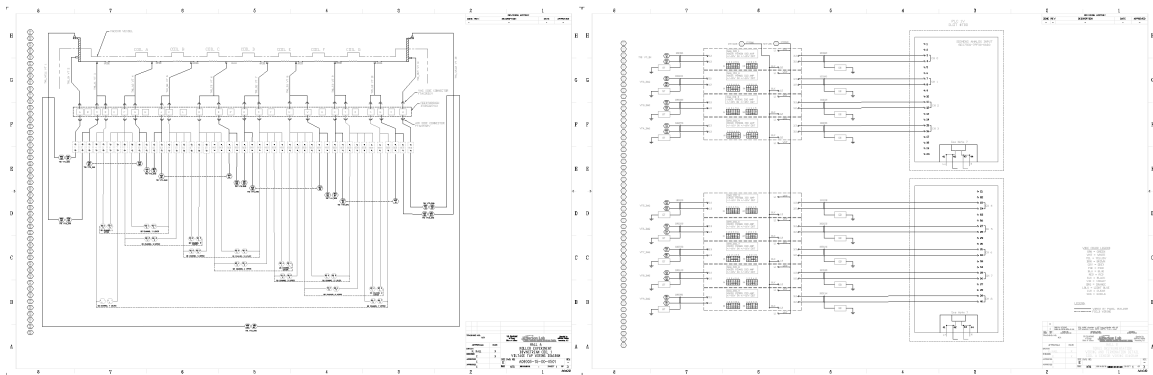
The screenshot shows a window titled "CS-Studio" with a sub-window "TM VTs list X" at 100% zoom. The main content is a table titled "Torus Magnets' Voltage Taps [V]" with a timestamp of "2023-04-05 10:35:43". The table lists various components on the left and four tap locations (TM 1, TM 2, TM 3, TM 4) on the top. Each cell in the table contains the text "<moller>".

	TM 1	TM 2	TM 3	TM 4
Splice in	<moller>	<moller>	<moller>	<moller>
Splice out	<moller>	<moller>	<moller>	<moller>
WCL supply	<moller>	<moller>	<moller>	<moller>
WCL return	<moller>	<moller>	<moller>	<moller>
Whole magnet	<moller>	<moller>	<moller>	<moller>
Coil A	<moller>	<moller>	<moller>	
Coil A left				<moller>
Coil A right				<moller>
Coil B	<moller>	<moller>	<moller>	
Coil B left				<moller>
Coil B right				<moller>
Coil C	<moller>	<moller>	<moller>	
Coil C left				<moller>
Coil C right				<moller>
Coil D	<moller>	<moller>	<moller>	
Coil D left				<moller>
Coil D right				<moller>
Coil E	<moller>	<moller>	<moller>	
Coil E left				<moller>
Coil E right				<moller>
Coil F	<moller>	<moller>	<moller>	
Coil F left				<moller>
Coil F right				<moller>
Coil G	<moller>	<moller>	<moller>	
Coil G left				<moller>
Coil G right				<moller>
Coil A-B				
Coil B-C	<moller>	<moller>	<moller>	<moller>
Coil C-D	<moller>	<moller>	<moller>	<moller>
Coil D-E	<moller>	<moller>	<moller>	<moller>
Coil E-F	<moller>	<moller>	<moller>	<moller>
Coil F-G	<moller>	<moller>	<moller>	<moller>
Coil G-A	<moller>	<moller>	<moller>	<moller>

2. VT Wiring Diagram

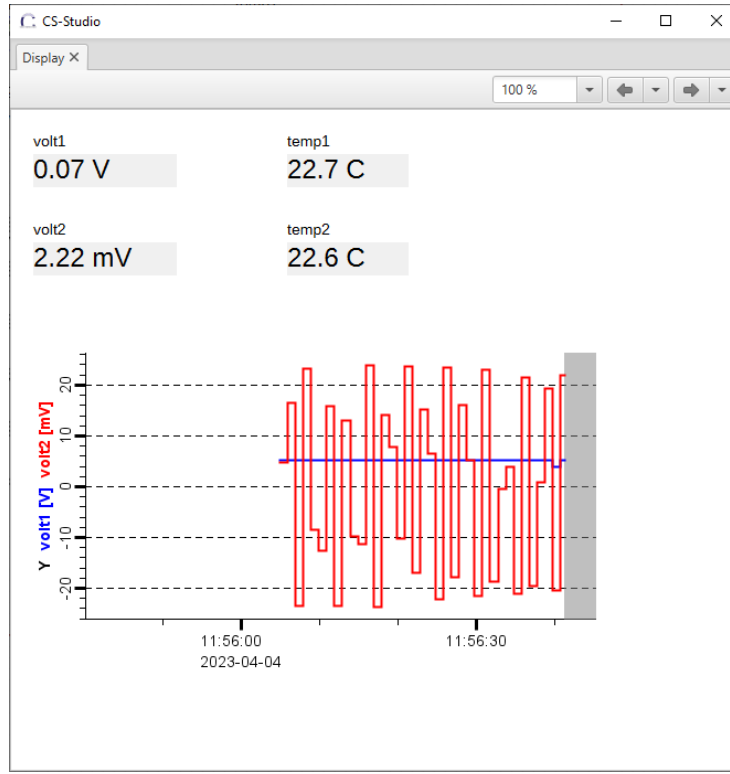
Kaiyi Hall, Brian Eng

1. Completed first draft of voltage tap wiring diagram



3. Siemens PLC *Brian Eng*

1. Created test IOC to communicate with Siemens PLC using s7nodave driver
 - Made test Phoebus screen to view the process variables (PVs)



- PV update rate not same as what is set in database, e.g. set to 100 ms, PV updates not at same rate

```
beng@DSG-WIN-EEL231: ~  
beng@DSG-WIN-EEL231:~$ /opt/epics/bin/linux-x86_64/camonitor ai_1_ch3  
ai_1_ch3      2023-04-05 10:53:55.297439 -1095  
ai_1_ch3      2023-04-05 10:53:55.484410 -10289  
ai_1_ch3      2023-04-05 10:53:55.669066 -12907  
ai_1_ch3      2023-04-05 10:53:55.853125 -7296  
ai_1_ch3      2023-04-05 10:53:56.132065 2990  
ai_1_ch3      2023-04-05 10:53:56.316744 11471  
ai_1_ch3      2023-04-05 10:53:56.500548 12788  
ai_1_ch3      2023-04-05 10:53:56.686328 6104  
ai_1_ch3      2023-04-05 10:53:56.963243 -4351  
ai_1_ch3      2023-04-05 10:53:57.148349 -11988  
ai_1_ch3      2023-04-05 10:53:57.332943 -11978  
ai_1_ch3      2023-04-05 10:53:57.610086 -4330  
ai_1_ch3      2023-04-05 10:53:57.795102 6126  
ai_1_ch3      2023-04-05 10:53:57.979635 12792  
ai_1_ch3      2023-04-05 10:53:58.258429 11458  
ai_1_ch3      2023-04-05 10:53:58.442143 2966  
ai_1_ch3      2023-04-05 10:53:58.628148 -7320  
ai_1_ch3      2023-04-05 10:53:58.812619 -12915  
ai_1_ch3      2023-04-05 10:53:59.090802 -10275  
ai_1_ch3      2023-04-05 10:53:59.275507 -1073  
ai_1_ch3      2023-04-05 10:53:59.459325 8878  
ai_1_ch3      2023-04-05 10:53:59.736826 13302  
ai_1_ch3      2023-04-05 10:53:59.921957 9406  
ai_1_ch3      2023-04-05 10:54:00.107469 -353  
ai_1_ch3      2023-04-05 10:54:00.384252 -9812  
ai_1_ch3      2023-04-05 10:54:00.569346 -13004  
ai_1_ch3      2023-04-05 10:54:00.754101 -7904  
^C  
beng@DSG-WIN-EEL231:~$
```

- Enabled a setting under protections in order for IOC to communicate with PLC; need to check with Siemens about possible security implications
 - The checkbox under Connection mechanisms was disabled by default
 - The access levels are unchanged from how controller was received

