Research and Development of a Basic Peer-to-Peer Streaming Application for PXI

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I researched and developed a basic peer-to-peer streaming application for DSG's PXI test station.

For this application, peer-to-peer streaming refers to reading and writing data between two FPGA modules installed into the PXI chassis without that data having to pass through the PXI's CPU or real-time OS. Potential uses for this format of peer-to-peer streaming are for applications where you need to both acquire and analyze data at very fast rates, but the PXI module's FPGA does not have the capability of performing both DAQ and analysis because of limited memory in the FPGA.

For the application, three separate programs were needed. The first program was developed to run on the FPGA of a PXIe-7971R module and acts as the writer to the stream. This program contains a while loop that indefinitely executes at a 40 MHz rate. In this loop, there is an integer counter that increments from 0 to 3, decrements back to zero, and then repeats. During every loop iteration, the counter's current value is also written to the peer-to-peer stream.

The second program was developed to run on the FPGA of a PXIe-7846R module and acts as the reader from the stream. This program reads data from the stream at a 40 MHz rate. If the value read is greater than or equal to 2, the program sets a digital input/output DIO channel of the module to True (or 3.3 V) and of the value is than 2, it sets the same DIO channel to False (or 0 V).

The third program developed configures, controls, and monitors the peer-to-peer stream and is deployed to the PXI's real-time CPU. Even though this program controls the peer-to-peer stream, it does not and cannot read or write any data to it.

- **PXIs have the capability to stream data between modules without that data**
- **Programs developed to write values of a counter to a peer-to-peer stream on one PXI module, read counter values from the stream on a second PXI module, and toggle a digital output of the second module based on the value of the counter**
- **End resulting behavior of programs and peer-to-peer stream were as expected**

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After development, compilation, and deployment of the three programs, the stream was enabled and the digital output status monitored using an oscilloscope. The behavior was as expected and a 6.67-MHz square wave was generated by the DIO channel.

Figure 1 is an ideal timing diagram of the expected values of the counter and digital output.

Figure 2 is a screenshot from the oscilloscope showing the square wave generated by the DIO channel that is toggled.

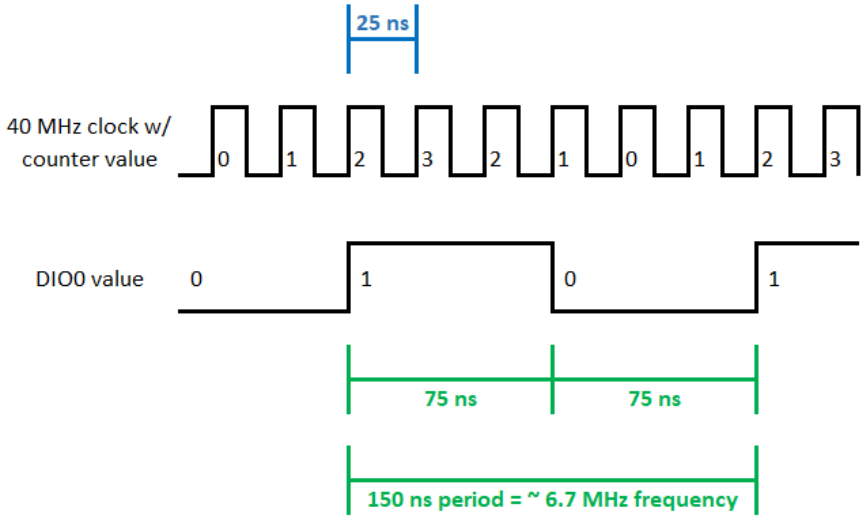

Fig. 1: Ideal timing diagram for counter value and DIO channel status. Both FPGA modules write to or read from the peer-to-peer stream at a rate of 40 MHz.

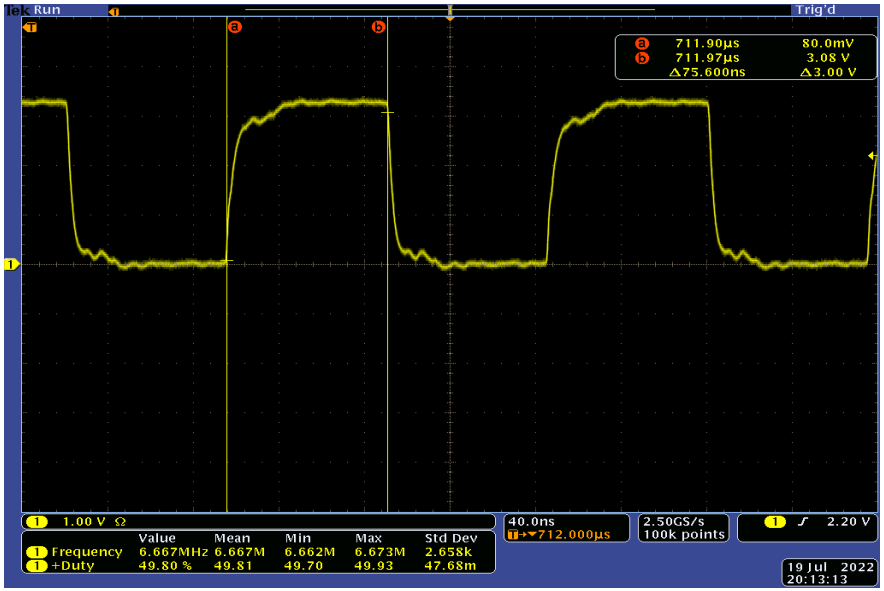

Fig. 2: Screenshot of oscilloscope capturing square wave generated by DIO channel on second FPGA module used to read counter value from the stream. Frequency and duty cycle of the waveform are measured by the oscilloscope and displayed in the lower left corner of the screenshot.