Sensiron SHT-35 Sensor Board Design for Hall B's RICH II Detector

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This note describes the design of the printed circuit board (PCB) that is the substrate for two Sensirion SHT-35 sensors. Twenty-four PCBs will be installed in the second Ring Imaging Cherenkov (RICH II) detector in Hall B to acquire humidity and temperature data from the nitrogen volume and the electronics panel [1, 2].

Figure 1 shows the nitrogen volume of the RICH II detector with the proposed installation locations of the SHT-35 sensor boards; Fig 2 the electronics panel.

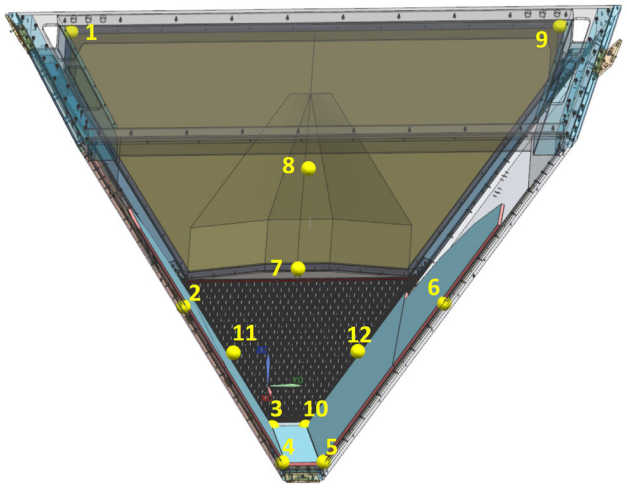

FIG. 1. RICH II detector's nitrogen volume showing the proposed installation locations of the SHT-35 sensor boards.

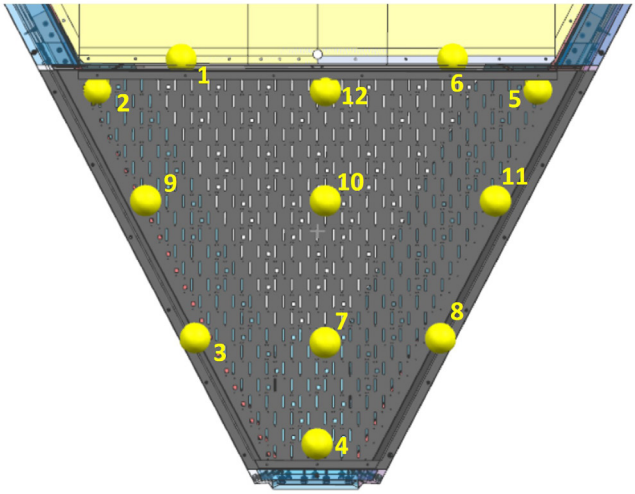

FIG. 2. RICH II detector's electronics panel showing the proposed installation locations of the SHT-35 sensor boards.

Figure 3, the rendering of the PCB, shows the PCB has two Sensirion SHT-35 sensors, two NXP PCA9600 buffers, electronics components, and a Molex Pico Clasp 8 connector.

Figure 4 shows the PCB layer layout. Each layer of the four-layer board has an ounce of copper. The top and bottom layers are trace layers; the inner layers are the 3.3-V power plane and the ground plane. All traces are eight-mils wide; the smallest copper-to-copper clearance is eight mils. The power plane and the ground plane are split in half along the length of the board, with 16 mils of clearance between the planes' halves.

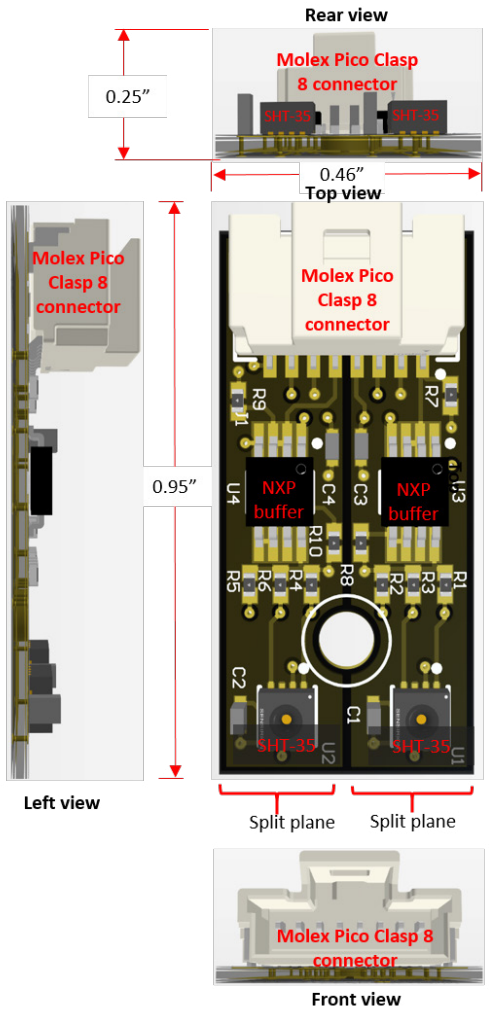

FIG. 3. Four views of the SHT-35 sensor board model. The bare board measures 0.95" by 0.46" by 0.062". With all components, the board profile is ~0.25", set by the height of the Molex Pico Clasp connector.

The Altium schematic, Fig. 5, shows that the sensors (U1 and U2) have their own NXP PCA9600 dual bidirectional bus buffers (U3 and U4) to isolate the bus capacitance. The

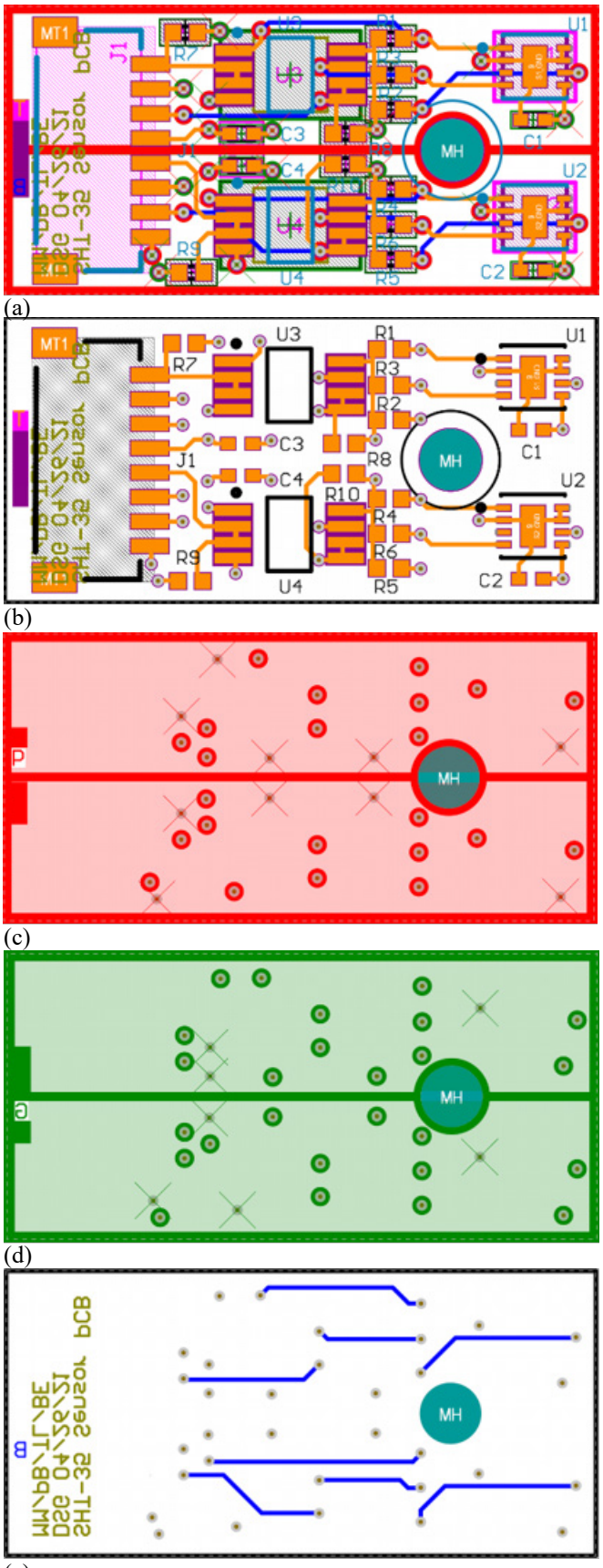

FIG. 4. SHT-35 sensor board four-layer design. (a) all layers, (b) top, (c) power plane, (d) ground plane, (e) bottom.

data, reset, and clock lines from the sensor to the buffer have a 10-KΩ pull-up resistors (R1-R6) to 3.3 V. The serial data and clock lines from the buffer to the connector have 300-Ω pull-up resistors (R7–R10) to 3.3 V [3]. To reduce noise, the sensors and the buffers have 10-µF, decoupling capacitors (C1–C4) located close to them.

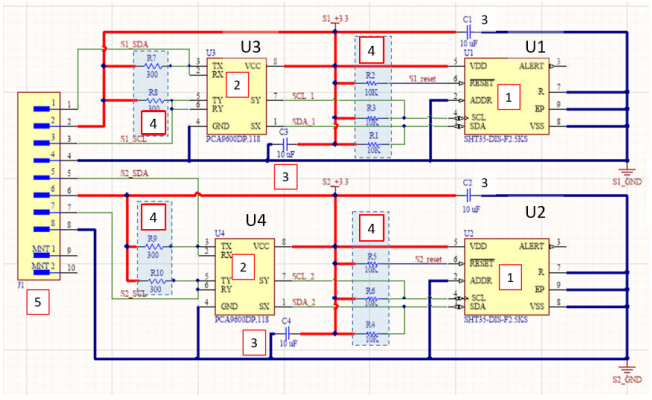

FIG. 5. Altium schematic of the SHT-35 sensor board. **1**. SHT-35 sensor. **2**. NXP PCA9600 buffer. **3**. Decoupling capacitor. **4**.Pull-up resistor. **5**. Molex Pico Clasp 8 connector.

Cable connection to the interlock chassis from the PCB is done using the Molex connector, which has eight pins with a pitch of 1 mm, four pins per sensor. Each set of four pins has a power pin and a ground pin, connected to their respective planes; the remaining two pins are for the I²C serial data and clock lines.

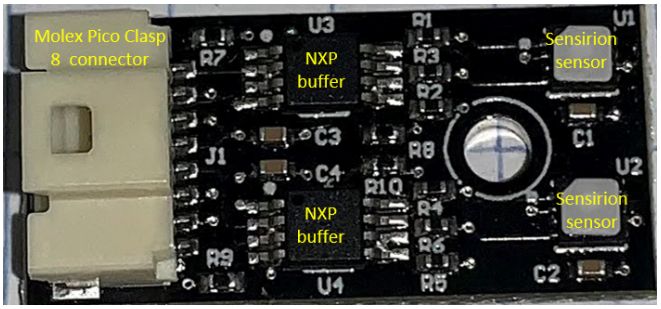

FIG. 6. A populated SHT-35 sensor board.

Ten PCBs were manufactured and populated, Fig 6. Upon receipt, the PCBs were bench tested.

In conclusion, SHT-35 PCBs for RICH II were researched, designed, developed, and tested. The first batch of ten boards is ready to be installed.

[1] P. Bonneau, et al., *Proposed Temperature and Humidity Digital Sensors for Interlock Systems of Detector Hardware*, DSG Note 2020-28, 2020.

[2] T. Lemon, et al., *RICH II LabVIEW Remote Interface*, DSG Talk 2021-17, 2021.

[3] T. Lemon, et al., *I²C Pull-Up Resistor Values for RICH Hardware Interlocks*, DSG Talk 2021-19, 2021.