Design of the Reconfigurable Input/Output Mezzanine Card for the Hardware Interlock System of Hall B's Second Ring Imaging Cherenkov Detector

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The second ring imaging Cherenkov (RICH) detector's reconfigurable input/output (RIO) mezzanine card is the interface between the sbRIO 9629 in the interlock chassis and the temperature and humidity sensors in the electronics and nitrogen volumes. The custom-designed RIO mezzanine card (RMC) supports I^2C communications over ~60 feet, keeps signal voltages in the range 0–3.3 V, and provides two relay circuits to interlock the RICH. This note presents the design of the RMC.

The detector's temperature and humidity is monitored by 24 SHT35 sensor boards, 12 each in the nitrogen and the electronics volumes [1]. Based on the values of the acquired signals, the sbRIO enables interlocking of the detector [2].

The sensors' signal cables connect to the interlock chassis by RJ-45 connectors on the Backplane PCB, where the signals are grouped in sets of four in the Backplane's insulation displacement contact (IDC) connectors and are from there routed to IDC connectors P1–P6 on the RMC, Fig. 1.

Figure 2 shows the RMC design. Signals are routed from the RMC IDC connectors P1–P6 to the Samtec SEAM-40, 240-pin connector J1, which mates with a connector on the sbRIO. Each IDC connector handles four SHT35 sensor boards, each of which has two humidity and temperature sensors, thus eight sensors per IDC connector.

On the RMC, each IDC connector has eight sets of buffering circuits, one for each sensor signal. Each buffering circuit has a dual Schottky diode chip at its input, an NXP



FIG. 1. Diagram illustrates signal interface from SHT-35 sensor boards via the RMC and sbRIO to the network.



FIG. 2. RICH II RMC Altium design. Each of the six routing layers is represented by a color $[top = orange, inner_1 = black, inner_2 = light blue, inner_3 = violet, inner 4 = pink, bottom = dark blue].$

PCA9600DP buffer, which regenerates the signal and outputs it to another dual Schottky diode chip. The dual Schottky diode chips from the Diodes Incorporated BAT54SDW series transmit signals voltages in the range 0–3.3 V. The input signal traces to the buffer and the output DIO traces have pull-up resistors of 10 K Ω and 300 Ω , respectively, connected to the 3.3 VDC power line [<u>1</u>, <u>3</u>]. Each buffer chip has a 10-µf decoupling capacitor placed as close as possible.

The dimensions of the RMC are 14 X 8 X 1.22 inches. The minimum trace width and clearance is eight mils. To ensure routing space for each DIO channel from the IDC connectors to the J1 connector, the RMC board stack-up uses 10 layers: six layers for routing signals [top, inner_1 to inner_4, and bottom] and four plane layers for power and ground [power, ground, power_1, and ground_1]. The layer stack-up is such that all trace routing layers have an adjacent uninterrupted plane layer for a return path of each signal. Each layer has an ounce of copper. Board components and traces are placed and routed to avoid traces crossing over openings in the planes caused by vias or pads. All signal traces are single-ended and have an impedance of 55 Ω , which meets the sbRIO requirement.

The board's Samtec 50-pin connector J3 (upper right corner in Fig. 2) monitors signals, such as the state of the override key switch, and controls the interlock relays. Additionally, the 5 V and 3.3 V power of the sbRIO is monitored by J3.

To conclude, the design of the RMC board has been completed. Initial breadboard prototyping indicates that the design works.

- [1] M. McMullen, et al., Sensirion SHT35 Sensor Board Design for Hall B's RICH II Detector, DSG Note 2021-14, 2021.
- [2] P. Bonneau, et al., Proposed Temperature and Humidity Digital Sensors for Interlock Systems of Detector Hardware, DSG Note 2020-28, 2020.
- [3] T. Lemon, et al., *I²C Pull-Up Resistor Values for RICH Hardware Interlocks*, DSG Talk 2021-19, 2021.