Monitoring and Relay Controls of the Reconfigurable Input Output Mezzanine Card for the Second Ring Imaging Cherenkov Detector's Interlock System

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This note describes the monitoring and controls section of the reconfigurable input output (RIO) mezzanine card (RMC) board.

The RMC for the second Ring Imaging Cherenkov (RICH) detector is attached to the sbRIO by the Samtec SEAM-40, 240-pin connector J1, Fig. 1 top center, which mates with a connector on the sbRIO. Certain input/output (I/O) signals of the sbRIO are used for controls and monitoring, for example, the hardware interlock system's external override key switch. In addition to the monitoring feature, the RMC has two relay channels, one to interlock the CAEN high voltage system, the other a spare. [1]

The Samtec 50-pin connector J3 on the bottom side of the RMC board, upper right corner, Fig. 1, connects to its counterpart on the sbRIO with a 50-pin ribbon cable. Table I defines the controls and monitoring signals of the sbRIO on J3.

There are eight analog input channels on J3, AI0–AI7, that monitor signals. AI0 and AI1 monitor the signals that actuate relays K1 and K2 [2]. AI2 monitors the position of the external override key for the hardware interlock system via connector J6. AI3–AI5 monitor voltages from the sbRIO and the RMC via the J1 connector, and the external 3.3 V that powers the RMC. AI6 and AI7 are available analog input channels for monitoring, which can be accessed using J7 and J8.

J3 has four analog output channels, AO0–AO3, for the control signals. The controls signals are generated by the sbRIO software. AO0 and AO1 are dedicated to the control of the two solid-state relays K1 and K2. To activate the relay, a current is supplied to the base of one of the NPN transistors from either AO0 or AO1. Access to the relay contacts is provided by two-pin headers J4 and J5, respectively. AO2 and AO3 are connected to two-pin header connectors J9 and J10 and are available for use in other systems.

The last four channels of J3, DIO0–DIO3, are routed to the eight-pin header connector J11. The DIO channels can be defined as inputs or outputs and are reserved for future use.

In conclusion, the RICH II RMC uses the 50-pin connector J3 to route control and monitoring signals. The breadboard version of the design has been tested.

[1] Marc McMullen, et al., *Design of the Reconfigurable Input/Output Mezzanine Card for the Hardware Interlock System of Hall B's Second Ring Imaging Cherenkov Detector*, DSG Note 2021-22, 2021.
[2] Tyler Lemon, et al., *Selection of Parts for the Reconfigurable Input/Output Mezzanine Card of the Hardware Interlock System for Hall B's Second Ring Imaging Cherenkov Detector*, DSG Note 2021-24, 2021.

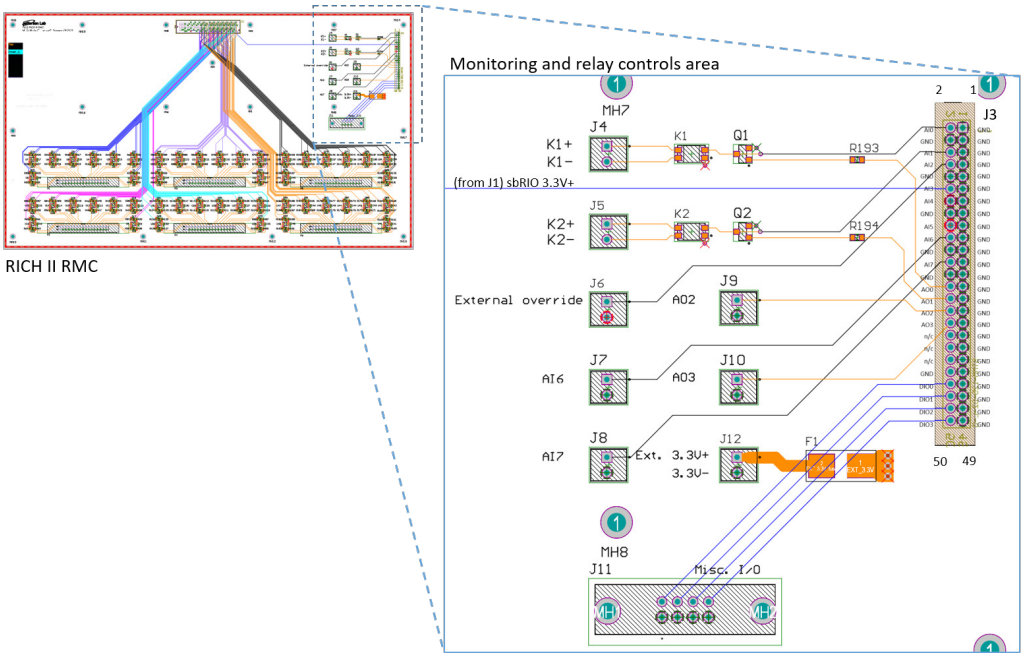

FIG. 1. The RICH II RMC PCB with a close-up of the monitoring and relay controls area.

sbRIO signal on J3	Monitored	RMC connection	Function
AI0	Q1 collector	Q1 pin 3	monitor relay K1 control signal
AI1	Q2 collector	Q2 pin 3	monitor relay K2 control signal
AI2	external override	J6	monitor external key position
AI3	sbRIO 3.3	J1 F39 & F40	monitor sbRIO 3.3 V
AI4	sbRIO 5	Power_2 (plane)	monitor sbRIO 5 V
AI5	external 3.3	Power (plane)	monitor input 3.3 V to RMC
AI6	J7 pin 1	J7	monitor undetermined input signal
AI7	J8 pin 1	J8	monitor undetermined input signal
J3 signal	Controlled	RMC connection	Function
AO0	K1 relay	J4 (contacts)	control relay K1
AO1	K2 relay	J5 (contacts)	control relay K2
AO2	J9 pin 1	J9	undetermined analog output control
AO3	J10 pin 1	J10	undetermined analog output control
J3 signal	Expansion I/O	RMC connection	Function
DIO0	J11_1	J11 pin 2	TBD I/O control or monitor
DIO1	J11_2	J11 pin 4	TBD I/O control or monitor
DIO2	J11_3	J11 pin 6	TBD I/O control or monitor
DIO3	J11_4	J11 pin 8	TBD I/O control or monitor

TABLE I. Controls and monitoring signals of the sbRIO on J3.