Upgrading the Hall B Magnet FastDAQ system with additional Voltage Taps

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February 21, 2023

This note describes the changes to the Hall B Solenoid Magnet FastDAQ system to monitor additional voltage taps that were added to monitor hardware changes internal to the magnet power supply (MPS).

With repairs and upgrades to the Hall B Solenoid (MPS), some components were replaced with similar components. One of these components is the flexible link between the bus bars inside the power supply connecting the MPS to the external leads. In the original MPS, these were laminated copper sheets, Fig 1; the new ones are braided copper cable, Fig. 2.

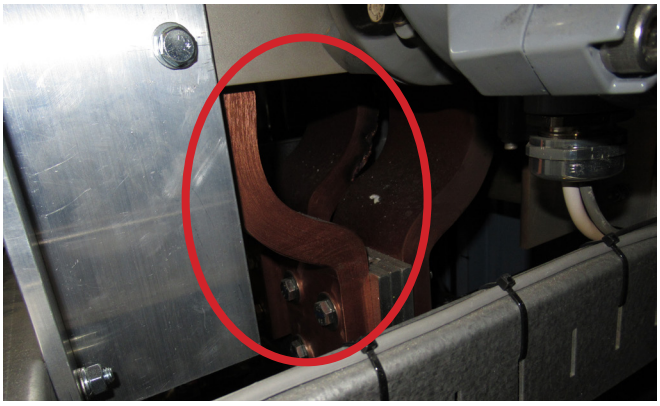


FIG. 1. Laminated links in the original MPS.

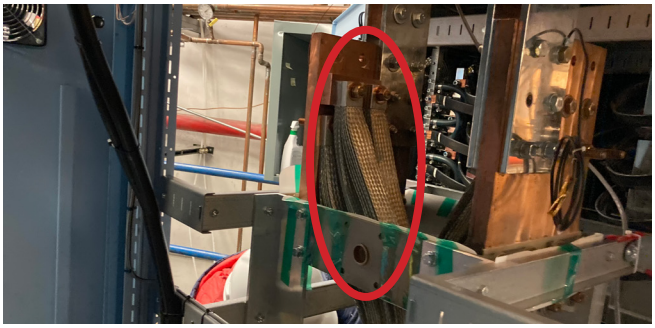


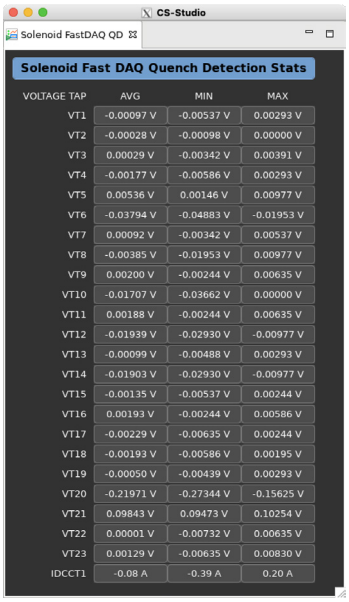
FIG. 2. Braided links in the repaired MPS.

To ensure that there are no changes in performance of the MPS due to these new components, two new voltage taps (VTs) were added across the flexible links to measure voltage drop.

Changes to both software and hardware were made to implement the additional VTs. Hardware changes required wiring of the VTs from the MPS to the instrumentation racks, the installation of additional isolation amplifiers (0–5 V input range, 0–10 V output range), and wiring to the ADC modules of the cRIO. Software changes were needed in the LabVIEW code, as well as in the EPICS softIOC to display the new values to end users.

The LabVIEW code on the cRIO has two sections—the FPGA code that acquires data from the ADC modules and the virtual instruments (VIs) that process this data and send it to EPICS and the PLC. The FPGA code was written so that all channels on all ADC modules are sampled. The VIs that process the data from the FPGA required modifications, namely removing the new channels from the block of code that removes unused channels from being processed, and adding the correct scale factor. The new VT signals (V, $V_{average}$, V_{min}, and V_{max}) were added to the EPICS IOC that runs on the cRIO, as well as the softIOC that passes the signals to the MYA archiver.

The PLC code shifts offsets (as the new VTs were added between existing used channels) and adds new tags for the new signals. Lastly the VTs were added to the EPICS CSS screen, Fig. 3.



VOLTAGE TAP	AVG	MIN	MAX
VT1	-0.00097 V	-0.00537 V	0.00293 V
VT2	-0.00028 V	-0.00098 V	0.00000 V
VT3	0.00029 V	-0.00342 V	0.00391 V
VT4	-0.00177 V	-0.00586 V	0.00293 V
VT5	0.00536 V	0.00146 V	0.00977 V
VT6	-0.03794 V	-0.04883 V	-0.01953 V
VT7	0.00092 V	-0.00342 V	0.00537 V
VT8	-0.00385 V	-0.01953 V	0.00977 V
VT9	0.00200 V	-0.00244 V	0.00635 V
VT10	-0.01707 V	-0.03662 V	0.00000 V
VT11	0.00188 V	-0.00244 V	0.00635 V
VT12	-0.01939 V	-0.02930 V	-0.00977 V
VT13	-0.00099 V	-0.00488 V	0.00293 V
VT14	-0.01903 V	-0.02930 V	-0.00977 V
VT15	-0.00135 V	-0.00537 V	0.00244 V
VT16	0.00193 V	-0.00244 V	0.00586 V
VT17	-0.00229 V	-0.00635 V	0.00244 V
VT18	-0.00193 V	-0.00586 V	0.00195 V
VT19	-0.00050 V	-0.00439 V	0.00293 V
VT20	-0.21971 V	-0.27344 V	-0.15625 V
VT21	0.09843 V	0.09473 V	0.10254 V
VT22	0.00001 V	-0.00732 V	0.00635 V
VT23	0.00129 V	-0.00635 V	0.00830 V
IDCCT1	-0.08 A	-0.39 A	0.20 A

FIG. 3. New VTs VT22 and VT23 added to screen.

During checkout of the MPS, it was found that the addition of current limiting resistors on the VTs caused an additional 25% voltage drop. This 25% offset was corrected by changing the scale factor from 0.5 (based on the iso-amp input range vs output range) to 0.625 in the cRIO VI code that configures the FPGA.

To conclude, with the voltage taps added to the FastDAQ system, any voltage differences due to the braided MPS links can be monitored and archived.