Detector Support Group
Weekly Report 2018-04-04

Summary

Hall B Magnets

- Solenoid and Torus recovered after multiple failures on 4/1/2018.
  - Failure 1: Torus fast dump caused by Ethernet/IP module failure.
    - Ethernet/IP module failure caused I/O Fault on PLC controller.
    - I/O Faults will cause PLC to stop its program, in turn causing a fast dump.
    - Torus PLCs recovered after power cycling remote and local PLC chassis.
  - Failure 2: Solenoid fast dump caused by induced voltage in Solenoid coil 5 from Torus's fast dump.
    - Induced voltage tripped QD1:Ch1-upper
    - SOE module gave no indication of trip sequence as module still displayed old trip data because of an issue with the module's reset.
  - Failure 3: Torus FastDAQ cRIO failed; cause unknown.
    - cRIO not able to be connected over network or run program, but cRIO could boot in safe-mode (fourth time magnet cRIOs have had this failure).
    - cRIO replaced with spare 9067 model cRIO.
    - PR submitted for replacement 9045 model cRIO.
  - Failure 4: Solenoid FastDAQ cRIO died; cause unknown.
    - cRIO not able to be connected over network or run program, but cRIO could boot in safe-mode (fourth time magnet cRIOs have had this failure).
    - cRIO replaced with DSG's spare 9035 model cRIO.
    - PR will be submitted for new 9045 model cRIO.
- Differential probes and oscilloscopes connected to Solenoid Quench Detector (QD) #2 Channel 8 to monitor voltages at QD board.
  - Oscilloscope #1 monitors output to QD unit for QD #2 Channel 8.
  - Oscilloscope #2 monitors signal input to QD board for QD#2 Channel 8.
  - Webcam and oscilloscope network connections set up for remote monitoring.
    - Webcam hostname hallbcam09.jlab.org.
    - Oscilloscope assigned hostname hb-oscope with IP address 129.57.96.41

SVT

- Replacement cRIO model 9035 received for SVT Hardware Interlock System.
- Code to handle negative HFCB temperatures in the hardware interlock system tested and debugged using DSG test station.
  - Code will be deployed in interlock system during next shut-down period.
- Resolved error that was preventing archival of hardware interlock PVs in MYA database.
  - Error caused by a firewall issue with accelerator systems.
  - Logging of hardware interlock signals in MYA database started on 3/20/2018 at 13:00.
- HTSB redesigned to make board cheaper and easier to assemble.
  - Omega PT100 will be replaced by a surface mount RTDs.
  - Surface mount RTDs ordered to test their 4-wire applications before finalizing redesigned HTSB
- Connectors received for Patch Panel boards.

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HDice

- Data array processing subVIs for NMR test program developed.
  - SubVIs align current shunt and lock-in amplifier data after an NMR scan using sequence number from the CT-box binary data stream.
  - Error checking routine's interface to the alignment subVIs also developed.
- Calibration system assembled to check Oxford power supply set and read-back settings.
- Development RF Box tested.
  - Proper wiring based on control and power schematics verified.
  - LabVIEW program used to test RF Box switch, attenuators, and key readback.
    - All tests passed except for AFP attenuator readback since that attenuator always reads back -63 dB.
- Development RF Box's DCON 7053 digital input module debugged.
  - Module used to read AFP attenuator status.
  - Module's inputs float to ~4.5 V, causing module's status bits for inputs to all falsely read as True.

Gas System

- Design work completed on front and rear panels of MFC power chassis.
- LabVIEW VI developed to generate a report on gas system status.
  - VI collects data every 10 seconds when running and generates a report containing data taken for the past 24 hours.

Hall D Solenoid

- Magnetic field sensor fixed on 04/02/2018
  - The single-axis probe was not properly installed after initial debugging.
  - Probe was rotated to proper position and reinstalled.
  - Magnetometer now correctly reads ~1.4 T when Solenoid is at full field.

cRIO Test Station

- Voltage integral nonlinearity test's automatic and manual modes developed and successfully tested.
  - Updated test program to compare midpoints of test values, not at test value.
- "Missing Codes" test defined for ADCs, developed, and successfully tested.
  - Test computes the number of the bits in the digital output for voltage inputs.
  - Test then compares measured number of bits with the ideal number of bits in the digital output of the ADC.
  - Test determines the presence of "missing codes" for each channel in the ADC module if ideal value is greater than the measured.
  - Code for test developed and added to test station's manual mode.

Antonioli, Mary Ann

cRIO Test Station

- Wrote voltage integral nonlinearity test for auto mode.
  - Updated Excel template.
  - Tested OK.
- Updated, tested, and debugged voltage integral nonlinearity test to compare midpoints of test values, not at test value.
  - Updated test in both manual and automatic modes.
  - Both modes tested OK.
- Wrote, tested, and debugged test for missing code.
  - Added test to manual mode and made Excel template.
  - Tested OK.

Bonneau, Peter

HDice

- Programmed, tested, and debugged data array processing subVIs for NMR Development test program.
  - Developed subroutines align current shunt and lock-in amplifier data after an NMR scan using sequence number from the CT-box binary data stream.
  - Developed error checking routine's interface to the alignment subVIs.
- Assembled current calibration system to check Oxford power supply set and read-back settings.

SVT

- Received replacement National Instruments cRIO model 9035 for SVT Hardware Interlock System.
  - Loading of system software on processor in progress.
- Tested the debugged HFCB temperatures conversion code using DSG test station.
  - Conversions for HFCB temperature sensor readings below 0 °C completed.
  - Revised code will be implemented in interlock system during next extended maintenance period.
- Resolved issue with EPICS Hardware Interlock PVs to MYA database.
  - "IO error 2" was shown on console when archived interlock PVs were displayed.
  - Error caused by a firewall issue with accelerator systems.
  - Datalogging of hardware interlock signals started on 3-20-2018 @ 13:00.
  - A list of the 114 PV signals & dead-band settings was posted on the SVT slow controls userweb.

- Held daily meetings on Hall D status and EPICS controls monitoring.

Campero, Pablo

Magnets

- Set up two oscilloscopes to measure voltage at the Solenoid Quench Detector # 2.
  - Goal is to monitor the VT18_DAQ that causes the trip in the QD even when the set trip thresholds are not observed in FastDAQ data.

- Requested IP and hostname for the oscilloscope to be set up in the Hall B subnet.
  - Hostname hb-oscope and IP 129.57.96.41 assigned.
- Installed video camera to monitor two oscilloscopes connected to QD#2.
- Oscilloscopes set up to measure voltage at QD#2:ch8's input to QD board with a trigger level of 830 mV, and QD#2:ch8's output from QD board to QD unit with a trigger level of 740 mV.

HDice

- Debugged test RF box with Tyler and Amanda.
  - Verified proper wiring based on control and power schematics.
  - Used LabVIEW test program to verify proper responses of attenuator A and attenuator B.
    - Found issues with the read-back for attenuator B.
    - For any attenuation value set, the read-back value was always -63 dB.
  - Found Digital input module 04 (DCON 7053) was reading ~4.5 V when relay was open.
    - Module expects under 3.0 V to read input as zero or False.

Hall D

- Monitored CDC, FDC and Solenoid via EPICS and logbook entries daily.
  - Magnetic field sensor for the Solenoid fixed on 04/02/2018
    - The single-axis probe was rotated to proper position and reinstalled.
    - Magnetometer now correctly read ~1.4 T when Solenoid is at full field.

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- Defined "Missing Codes" test for ADCs in the **cRIO Test Station**.
  - Test must compute the number of the bits in the digital output for each voltage input.
    - Voltage inputs will be tested at 1 V steps.
  - Test then compares measured number of bits with the ideal number of bits in the digital output of the ADC
  - Test determines the presence of "missing codes" for each channel in the NI9207 ADC module if ideal value is greater than the measured.
- Set up new 72" screen in EEL 121 control room.

Eng. Brian

SVT

- Redesigned HTSB to make it cheaper and easier to assemble.

Hall B Magnets

- Analyzed voltage tap data for spikes in Solenoid and Torus.
- Recovered both Magnets and their control systems after multiple failures on 4/1/2018.
  - Failure 1: Torus fast dump caused by failure of Ethernet/IP module.
    - https://logbooks.jlab.org/entry/3552977
    - Ethernet/IP module failed, causing an I/O Fault on PLC controller.

        - I/O Fault causes PLC to stop running its program, in turn causing a fast dump.
        - Torus PLCs recovered after power cycling remote and local PLC chassis.
    - Failure 2: Solenoid fast dump caused by an induced voltage on coils from fast dump of Torus.
        - https://logbooks.jlab.org/entry/3553002 and https://logbooks.jlab.org/entry/3552938
        - QD1-upper tripped; status matched on both software indicators and hardware QD's local display.
        - SOE module gave no indication of trip sequence as module still displayed old trip data.
    - Failure 3: Torus FastDAQ cRIO died; cause unknown.
        - https://logbooks.jlab.org/entry/3553050
        - Torus FastDAQ cRIO failed in the same way it has failed three previous times: not able to connect to over network or run program, but cRIO can boot in safe-mode.
        - cRIO replaced with spare 9067 model cRIO.
        - PR submitted for replacement 9045 model cRIO as newer model cRIOs in use in Hall B have not had same failure as 9060 series models.
    - Failure 4: Solenoid FastDAQ cRIO died; cause unknown.
        - https://logbooks.jlab.org/entry/3553105
        - Solenoid FastDAQ cRIO failed in the same way it has failed three previous times: not able to connect to over network or run program, but cRIO can boot in safe-mode.
        - cRIO replaced with DSG's spare 9035 model cRIO.
        - PR will be submitted to replace cRIO with 9045 model cRIO as newer model cRIOs in use in Hall B have not had same failure as 9060 series models.
- Met to discuss VT and QD unit diagnostic testing
    - Since Hall B was in controlled access due to accelerator's RF studies, probes were attached to QD units on 4/3/2018.

Hoebel, Amanda

HDIce

- Debugged RF Box with Tyler and Pablo using Pete's test program.
    - Program works on known operational RF Box but on test RF Box, the AFP attenuator setting is always read back as -63 dB.
    - Problem found to be related to module 4.
        - Operational RF Box had a relay voltage of ~1.2 V whereas test RF Box had a relay voltage of ~5 V.
        - The ~5 V is most causing all digital inputs in module 4 read an input, causing -63 dB to be read by the program.

- Set up new TV in DSG control room for Hall D monitoring.
- Moved electronics rack to EEL room 125 with Tyler, Pablo, and Mary Ann.

Jacobs, George

LTCC

- Monitored daily the internal pressure and gas usage for LTCC S5 single sector test.
- Updated LTCC S5 single sector test status power point

- Completed SAF100 training

Leffel, Mindy

Absent

Lemon, Tyler

RICH

- Completed detector health report for DSG weekly meeting.
- Wrote DSG note discussing differential pressure transducers installed for RICH and analysis of archived pressure measurements.

HDice

- Debugged RF Box and DIO modules with Pablo and Amanda.
  - ✶ Ran program to test RF Box switch, attenuators, and key readback.
    - All tests but AFP attenuator readback passed.
    - AFP attenuator readback always reads -63 dB, regardless of what attenuator is set to.
  - ✶ Debugged input module used to read AFP attenuator status.
    - Noted when there should be zero voltage when attenuator's bit is off, DI module was getting ~5 V.
    - Voltage coming from module itself; measured voltage from all other potential sources, only DI module was source of voltage.
    - Tested DI module to find voltage threshold at which it reads a 1 or 0.
      - Module reads 1 if input voltage is over 3 V.
      - Module reads 0 if input voltage is under 3 V.
  - ✶ Discussed next troubleshooting steps with Pete.
    - Will try using pull-down resistor to lower voltage in off state to below 3 V.
    - Replace DI module with another module that we know works to confirm wiring of RF box is correct.

Solenoid

- Connected differential probes to QD channels with Brian and Pablo to monitor voltages in QD wiring during ramp and operation of magnet.
  - ✶ See logbook entry at https://logbooks.jlab.org/entry/3554401
  - ✶ Goal is to determine whether QD electronics are tripping on noise from an unknown source.
  - ✶ Two oscilloscopes monitoring output to QD unit for QD #2 Ch 8's board and input of voltage tap to QD #2 Ch 8's board.
  - ✶ Set up webcam for remote viewing of non-network connected oscilloscope.

- Webcam hostname hallbcam09.jlab.org.

- Set up network connection for oscilloscope for remote monitoring and control of oscilloscope.
  - Scope hostname hb-oscope.jlab.org with IP address 129.57.96.41

McMullen, Marc

SVT

- Redesigned HTSB.
  - Omega PT100 will be replaced by a surface mount RTDs.
  - RTD replacement may make assembly easier.
- Ordered new surface mount RTDs to test different 4 wire applications before finalizing designed HTSB
- Received connectors for Patch Panel boards.
  - Still waiting on PCBs to arrive.

Gas System

- Completed design work on front and read panels of MFC power chassis.
- Continued development of Gas Report VI.
  - The data collection VI is running and collects gas system data every 10 seconds.
  - VI generates document containing analysis of 8640, or 24 hour's worth of, samples.