# Detector Support Group
## Weekly Report, 2019-08-07

# Summary

**Hall A – Super BigBite Spectrometer (SBS) HCAL**

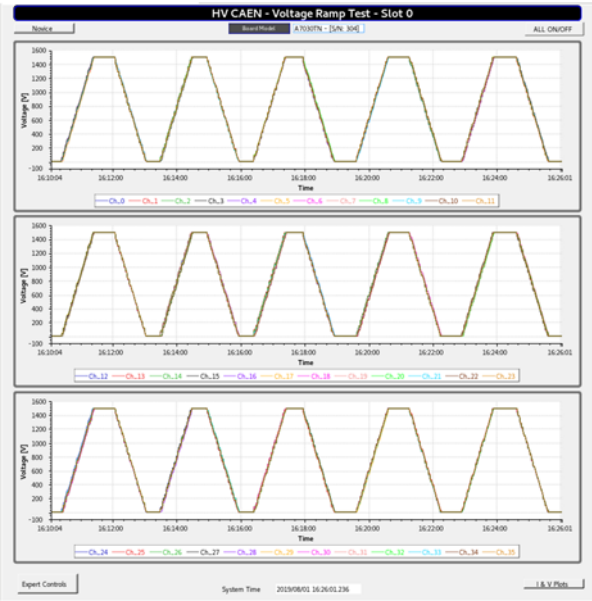
- Terminated eight BNC ends of BNC-to-LEMO cables.
- Cut 16 RG58 coaxial cable into 2 m lengths and terminated LEMO end.

**Hall C – EPICS**

- Investigated using PVTable tool in CSS for backup/restore operations.
- Added EDM calculations for maximum, minimum, and average sensor values to cryogenic WEDM screens using local CALC PVs.

**Hall C – CAEN HV Test Station**

- To test two CAEN SY4527 systems simultaneously, modified CAEN network configurations and developed CSS-BOY screens
  - ✶ Verified gateway, host name, and IP address for each CAEN-SY4527 system.
  - ✶ Modified service name to identify PVs for both system mainframes
    - *hvcaentest1* and *hvcaentest2*.
  - ✶ Changed names for all PVs used in the CSS screens. Now all PVs start with service name (hvcaentest1 or hvcaentes2) of each crate as pre-fix.
- Modified Java scripts used to set all channels on/off and main parameters simultaneously.
- Tested three HV boards (model: A7030TN) on CAEN mainframe *hvcaentest1*
  - ✶ No issues found, all channels ramped to the set voltage.
- Concluded, most probably EPICS built-in service in *hvcaentest2* fails.
- Generated spreadsheet with the details of the test performed for three HV CAEN A7030TN boards running on *hvcaentes1* system mainframe.




*HV-CAEN-A7030TN Voltage Ramp Up/Down Test* CSS-BOY screen shows plots for voltage ramp up/down from HV board S/N 304 at hvcaentest1 mainframe

- For HV Test Stand load box, calculated resistor values.

**Hall A – GEM Gas System**

- Modified gas distribution P&I diagram to allow different detector configurations.
- Updated gas supply hardware distribution system cost estimate.
- Provided flow sensor and multiplexer to be placed in Hall A to evaluate its performance under radiation.

**Hall B – Magnets**

- Tested data transfer between FastDAQ cRIO and EPICS to isolate duplicate/missed timestamps issues.
  - ✶ Tested two different version of LabVIEW programs to see if the timestamp issues is originated by the data reading from the cRIO-ADC modules or writing the data from cRIO to EPICS.
  - ✶ Program 1 with no ADC readings: Used RT FIFO functions with fixed array of zeros to simulate 10 KHz ADC data sampling and transfer cRIO-to-EPICS at 5 HZ
    - ▪ Analysis indicated non-zero counts on both duplicate and missed timestamps for every channel.
  - ✶ Program 2 with no ADC readings: Used fixed array (2000 samples) and send this array to EPICS at 5 HZ.
    - ▪ Analysis of one run test showed zero timestamps issues.

**DSG R&D – cRIO Test Stand**

- Wrote code to test readback of NI 9870. Tested 4 ports at baud rate 9600.
  - ✶ Randomly fails with a time-out error.
  - ✶ Began testing at 19,200 baud rate.

**DSG R&D – LV Chassis FPGA**

- Verified correct operation of System-on-a-Chip (SoC) portion of board using demo program.
- Successfully compiled and deployed LV chassis FPGA program on FPGA.
- Configured SoC for network access.
  - ✶ MAC address for SoC changes every time board reboots. Investigating way to use static MAC.

**Accelerator Division R&D**

- Adjustments made to bonding parameters for superconducting $Nb_3Sn$ strip resonator sample continue.

**DSG-RICH R&D**

- Completed development of measurement commands for periodic data acquisition mode from the Sensirion SHT85 integrated sensor.