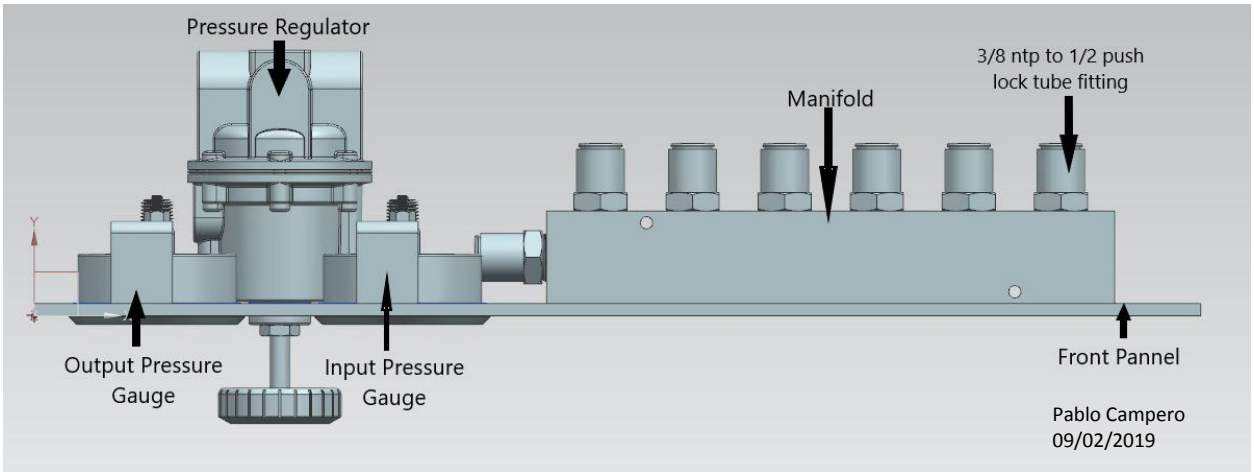
Detector Support Group
Weekly Report, 2019-09-03

Summary

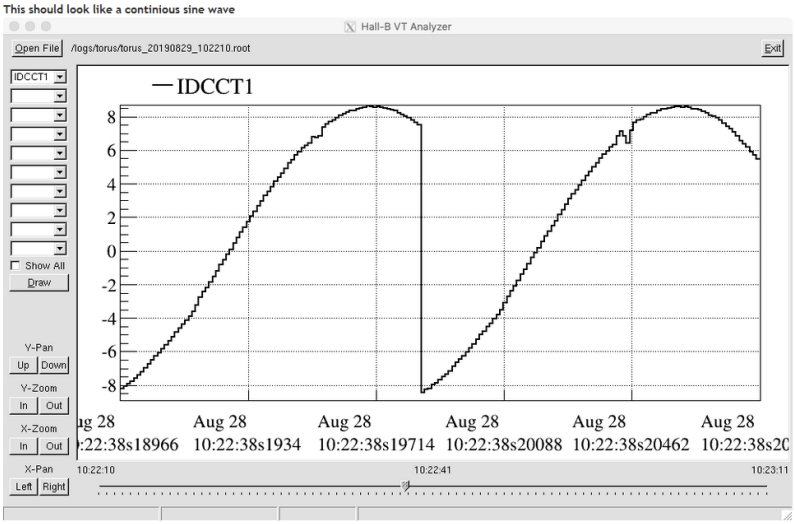
Hall A – GEM

- Developing 3D model in NX12 for Gas Distribution System



Hall B – Magnets

- Testing FastDAQ
  - ✶ Tried reading the ADC differently (200 samples over 10 loops), pushing the samples to FIFO, and reading FIFO at 5Hz
  - ✶ Experiencing readout problems: figure below should look like a sine wave



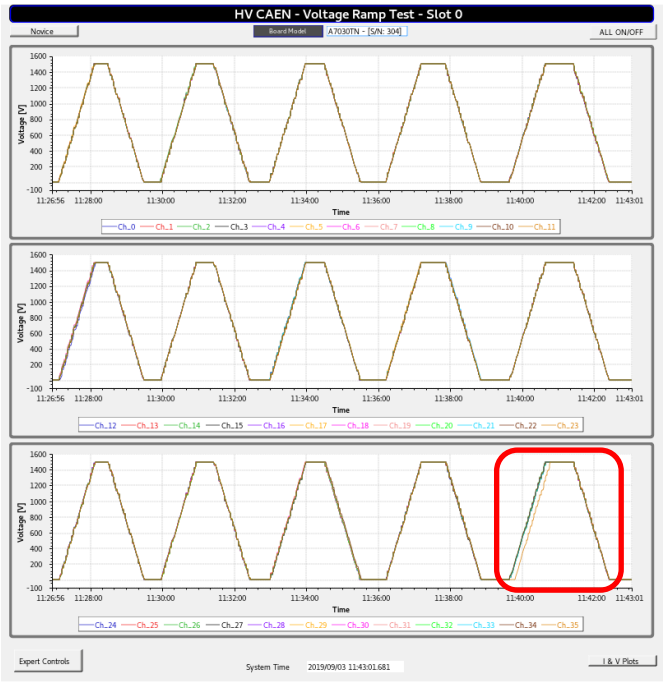
- To debug readout problem
  - ✶ Wrote Python script to check timestamps from voltage tap #24
  - ✶ No changes noticed over 300 ms differential between samples
  - ✶ Continuing to investigate

Hall B – HDIce

- Ordered 10 SMA Jacks for Molex Temp-Flex cable

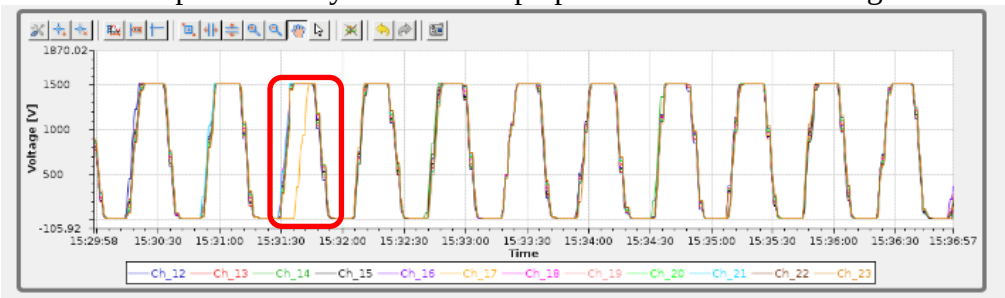
Hall C – CAEN HV EPICS Test Station

- Tested CAEN A7030 HV board per CAEN recommendation
  - ✶ Generated spreadsheet with detailed results for the tests



Voltage Ramp Test – Slot 0. CSS-BOY screen shows 15 ramp up/downs for test #3. Bottom panel shows channel 35 required restart.

- Wrote GECO script (CAEN software) to automate voltage test on A7030TN board
  - ✶ Noticed:
    - No channels failed over 100 ramps up/down
    - PV, Pw, associated with turn on/off status parameter for all 36 channels did not update while monitoring CSS-BOY screen – discrepancy between GECO and PV
    - PV update latency of 8 s to ramp up channel 17 to set voltage



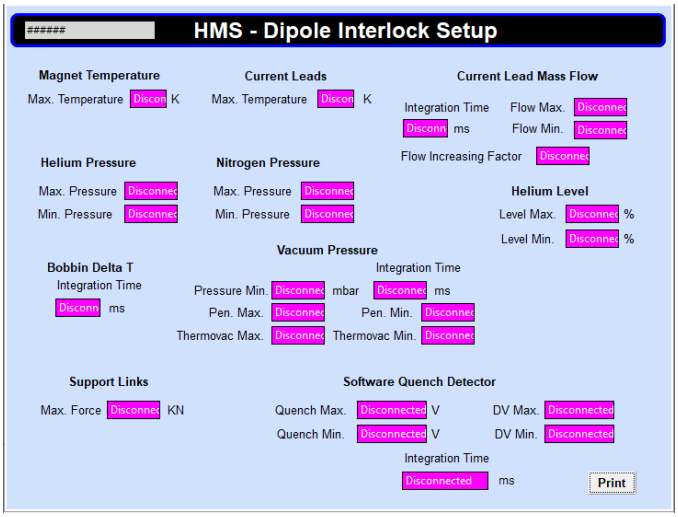
Zoomed view of *Voltage Ramp Test – Slot 0* CSS-BOY screen shows channel 17 starts ramp up 8 s after initiation

Hall C – CAEN HV Test Station

- Parts for the R52 to SHV adapters procured
- Eight A7030TN modules tested to full current (1 mA)

Hall C - EPICS

- Continuing development of HMS magnets screens



DSG R&D – cRIO Test Stands

- Completed retesting of NI-9871 RS485 Serial module
  - Margin of error for new test is 4.71%
  - Tests passed for all randomly generated alphanumeric strings on all four ports with three different baud rates for each port (450 strings per baud rate, per port)
- Wired and tested NI-9474 cRIO module
- Developed program to test NI-9402 low-voltage TTL input

DSG R&D – LV Chassis FPGA

- Developing program to read switch inputs on FPGA from SoC's hard processer system (HPS)
  - Program writes switch status to on-chip memory buffer from FPGA, reads memory buffer using HPS, and prints HPS status
  - Issues configuring FPGA-HPS buffer correctly

DSG R&D – PLC Test Station

- Testing RTD PLC module
  - ✶ Designing alarm screen HMI for RTD temperature sensor