Detector Support Group
Weekly Report, 2019-11-06

Summary

Hall A – SoLID Magnet Controls

- Contacted Allen Bradley support to solve firmware upgrade issues of high speed I/O PLC module, which could be used to read voltage tap sensors (ADCs)
  - ✶ Found issues with high speed I/O PLC module during firmware upgrade from rev. 1.4 to 3.5. Firmware version 1.4 allows a max RTS of 400 µs, compared with the firmware 3.5 version with a max RTS of 300 µs.
  - ✶ No response yet from Allen Bradley support
- Meeting with Steven Lassiter to discuss hardware and software tasks assigned to DSG

Hall B – BoNuS Target Gas Controls

- Continued work on the development of software controls
  - ✶ Still have unanswered questions by Hall B Engineering, e.g. MFC vs MFM

Hall B – Magnets

- Monitored and assisted controls systems during power up/down of both magnets on October 30, 2019

Hall B – RICH

- Installed RTDs in gas system cRIO on FC
  - ✶ Gives two additional temperature readings of L1 temperature using same RTD type as those previously moved to L4
  - ✶ Temperature sensor data readout could be used for any detector/system.
  - ✶ Generated the PVs for the RTDs sensors to be monitored and archived
- Debugged RICH temperature readout in EPICS
  - ✶ Noted that RICH temperatures were not updating frequently in comparison to other temperature sensors read by cRIO
  - ✶ Determined that IOC server (cRIO acts as client) has field for setting a monitoring dead-band. This dead-band prevents data from being written to EPICS unless change from previous EPICS value exceeds dead-band
  - ✶ Lowered monitoring dead-band from 0.05 to 0.01 resolved issue
- Debugged EP cRIO loss of humidity sensor readout
  - ✶ Verified sensors' 5V power supply, ground, and voltage signal at module is good.
  - ✶ Found that module settings had been changed from differential input to single-ended input; reverting change resolved issues

Hall B – SVT

- Two Humidity and Temperature Sensor Boards (HTSB) installed on the outside of the MVT to measure the temperature and humidity between CVT and CTOF.
  - ✶ Installed HTSBs in un-used locations on the patch panel (R4 environment sensors)
  - ✶ Each HTSB has two temperature sensors and two humidity sensors.
- Updated MPOD firmware
- Fixed bad hybrid temperature reading
- Removed broken key from the cRIO interlock chassis

Hall C – CAEN HV Test Station

- Tested multiplexer software by manually operating CAEN module.
  - ✶ All components of the test stand have been assembled
  - ✶ Running module hardware test

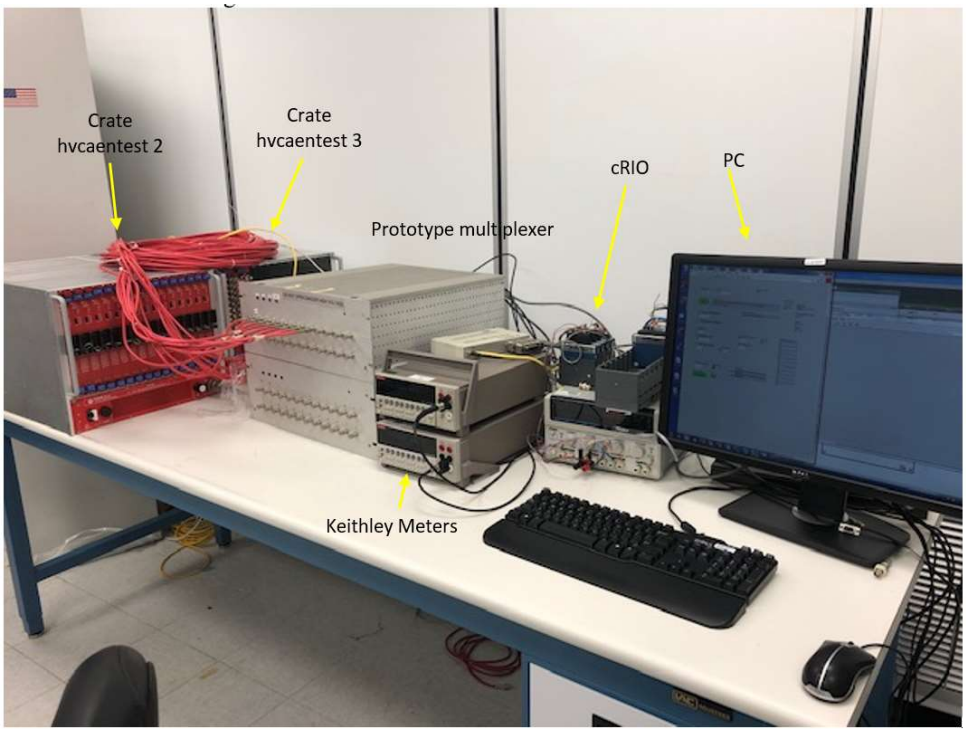

Figure shows HV Hardware test stand with multiplexer prototype

Hall C – CAEN EPICS Test Station

- Ran 24-hour stability test for SY4527 mainframe with 16 CAEN-A7030TN HV boards with all channels turned off
  - ✶ Used only GECO 2020 user interface to monitor and perform data logging for this test, since CSS-BOY screen had Java memory error while running 16 screens at the same time after ~5 hours from when the test was started.
  - ✶ From the test found that:
    - None of 36 channels' parameters for each board changed
    - Random voltage spikes occurred four times for a period of 1 s— 2 s with voltage between 15 V —237 V
- Ran 24-hour stability test for SY4527 mainframe with 16 CAEN-A7030TN HV boards with all channels at 1500 V
  - ✶ From the test found :
    - Issues to change all channel's (x576) parameters (SVMax, VSet, and IMax) at the same time
      - Forced to repeat setting up of the mentioned parameters several times
    - Recorded video showing the issues found with GECO 2020.
    - Once all board' channels were set to the desired value, none its parameters changed

Hall D WEDM

- Updated DIRC environmental screen to include liquid level sensor
- Corrected ordering of bit monitor on FCAL chiller screen

Engineering Division

- Soldered 140 components, including resistors, FPGAs, hex inverters, voltage regulators, 48 pin 16-bit transceivers, 48 pin16-bit buffer/line drivers, EMI filters, and voltage regulators

DSG R&D - SHT85 Sensor LabVIEW Readout

- Data-logging completed
  - ✶ Added LabVIEW 2019 test computer, so code can be run overnight without computer going to sleep
  - ✶ Header added to results spreadsheet
    Converted code for creating file name and header to a subVI

DSG R&D – LV Chassis FPGA

- Investigated hardware interface between sbRio and magnet LV chassis
  - ✶ An interface 40 pin IDC cable adapter between the DE0 breakout boards in the LV chassis to the NI 9694 digital I/O breakout daughter board will connect the 36 data lines to the sbRio SoC

DSG R&D – RICH

- For Sensirion SHT85 sensors, developed integrated temperature/humidity system interconnects, cable types, and chassis design for the sbRIO
  - ✶ Developed manual mode in sbRIO scan engine
  - ✶ Added FPGA select control for sensors tested by manual mode

DSG R&D – EPICS Data Logger

- Appended timestamp to data output
- Created CSS-BOY screen for real-time data plotting