Detector Support Group
Weekly Report, 2019-11-13

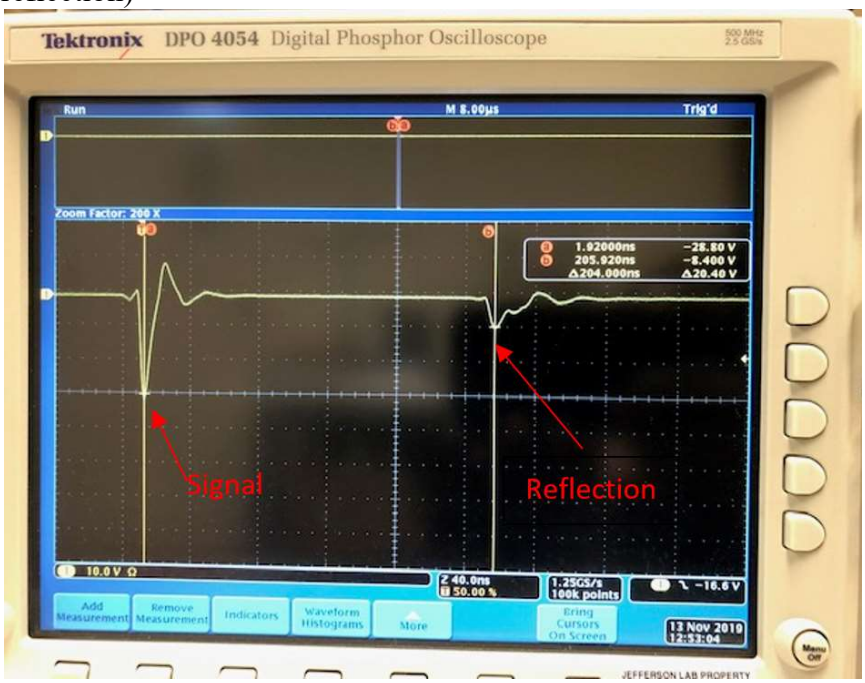
Summary

Hall A – SoLID Solenoid Controls

- Verified that Factory Talk View (HMI software) licenses are available for DSG
  - ✶ License is running in the PHYCAD58 Hall A computer
- Started preliminary design work on *Constant Current Source* board to provide fixed current for temperature sensors in the solenoid
  - ✶ Need seven boards, eight channels/board, each channel provides 100 uA
  - ✶ Contacted board manufacturer to get Gerber files to reproduce PCB design
    - ▪ Files not available
  - ✶ Checked components lists for availability of parts
    - ▪ Updated component list with on-hand quantities of parts
  - ✶ Measured dimensions of a board in Hall C
    - ▪ To confirm mounting hole locations
- Created restricted access folder to share documentation and files
- Generated tasks spreadsheet to track progress and status of individual tasks until the end of the project
  - ✶ Detailed breakdown and description of software, hardware, archiving, and technical documentation
  - ✶ Status, estimated time to complete tasks, and assigned staff

Hall B – Neutron Counters

- Labeled and tested five coax cables
  - ✶ Used signal generator with 10 KHz pulse and measured 102 ns (204 ns total reflection)



Signal reflection test coax cable, 10 KHz signal time is 204 ns, the cable is 102 ns long.

Hall B – RICH

- Developed program to read and log EPICS PV field values for hardware interlock system
  - ✶ List of fields obtained from interlock system's IOC server configurations
  - ✶ Program developed to compare PVs' monitoring dead-bands across all cRIO-based interlock systems
    - ▪ To check if the EPICS monitoring dead-band could be affecting any other systems' sensor readout
- Developed program to verify that "point-by-point" rolling average subVI used for hardware interlock systems is working correctly

Hall B – SVT

- Setting up VXS Silicon Control Module test stand
  - ✶ Destructive test required on an FSSR2 to see what the maximum voltage the inputs can handle and if that affects only a single (or multiple) channel(s) or the entire chip

Hall B – BoNuS Target Gas Controls

- Finished first pass at the controls software

Hall B – HDice

- Reviewed documentation on the new Lock-in Amplifier for NMR

Hall C – Target

- Addition of RTDs temperature sensors in progress
  - ✶ Terminated, tested, and labeled 15 RTD cables

Hall C – CAEN EPICS Test Station

- CAEN-A7030TN module received by CAEN technical support for further debugging
- Implemented EPICS data logger to record modules' PVs to compare EPICS data log with GECO data log

Hall C – CAEN HV Test Station

- Testing CAEN-A7030TN boards
  - ✶ While testing channels 0-17 of the board 0304 in slot 1 with GECO 2020 software, except for channels 14, 16, and 28, all other channels turned off
    - ▪ Software produced a status pop-up, which said there was a configuration change and shows slot 0 and slot 1 as disconnected

Engineering Division

- Soldered four 240 pin FPGAs for the Beam Position Monitor boards

Accelerator Division

- Terminated two 25 pin D-sub connectors

DSG R&D - SHT85 Sensor LabVIEW Readout

- Completed LabVIEW code and user interface to set upper and lower limits for temperature and humidity
- Completed subVI to compare readback with set limits
- Wrote subVI to count number of out-of-limit readings
    - ✶ Out-of-limits indicators added to user interface

DSG R&D – LV Chassis FPGA

- Developed timing simulator for LV Chassis DACs
    - ✶ Program developed to be able to start development of clock generation program for LV Chassis DACs without a sbRIO
    - ✶ Program displays resulting clock signals in a graph
    - ✶ Program uses PC's com port to assert/unassert serial handshaking lines to generate a real signal
- Investigated signal timing required to configure and read out LV chassis' ADCs
    - ✶ The serial interface to the ADC uses 4 DIO channels from the sbRIO SoC
    - ✶ The ADC configuration data is written to the chip upon power-up

DSG R&D – RICH

- Received and configured new sbRIO-9627 development kit
    - ✶ Obtained IP address and loaded operating system and LabVIEW on sbRIO
    - ✶ Connected SHT85 to LabVIEW project file loaded and deployed
    - ✶ Tested PCB with SHT85 sensor via FPGA DIO interface

DSG R&D – EPICS Data Logger

- Developing EPICS Data Logger to monitor EPICS PV values without dead-bands
    - ✶ Investigated and determined that to monitor PVs without dead-band the monitoring dead band field must be -1