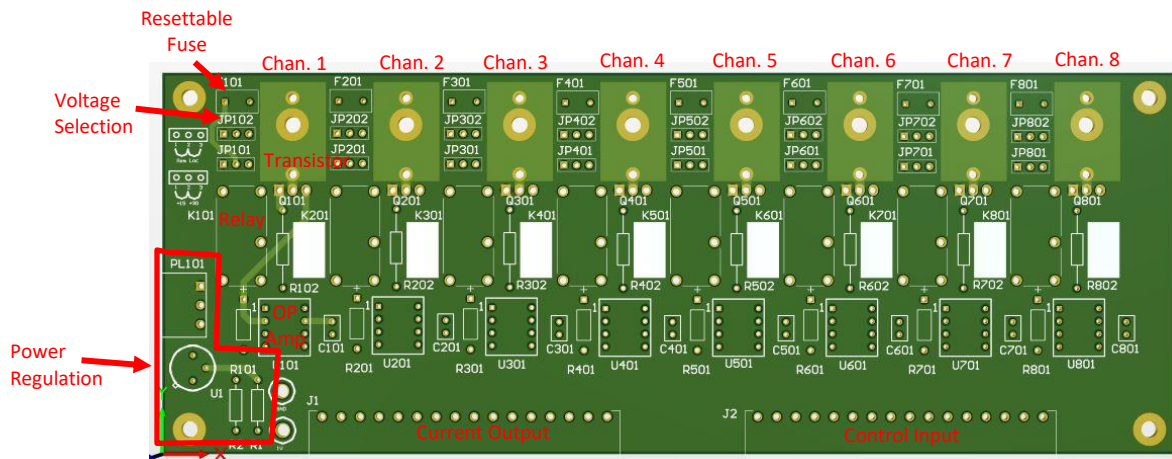


Summary

Hall A – SoLID Magnet Controls

- All components on Constant Current Source (CCS) board laid out; started routing on the power planes



3d rendering of the Constant Current Source PCB layout

- Developing PLC program to read axial and radial strain gauge sensors
- Verified KEPServer Enterprise OPC Server (PLC to EPICS) software’s licenses are available to DSG on PHYCAD58 host computer
- Developing FactoryTalk View data logger
 - ★ Tested data logger in Open Database Connectivity (ODBC) mode by storing data using ODBC data source (Microsoft Access)
 - ★ Generated PLC tag list with all potential variables that are to be logged
- Developing controls and instrumentation drawings
 - ★ Generated spreadsheet containing drawing number, description, and name for each drawing

Hall A – Super BigBite Spectrometer HCAL

- Terminated 48 BNC to LEMO cables (**100% completed**)

Hall B – HDice

- Reviewed options for saving measurement data files on Zurich UHFLI Lock-in Amplifier
 - ★ Files will be used for online and offline analysis of measured data
 - ★ Two NMR data scans were recorded (by HDice) with the file extensions of .mat and .csv
 - The .mat (MATLAB) data file is a proprietary file format from MathWorks and it could not be read directly without installing MATLAB
 - The .csv file is text and can be read directly by Excel and LabVIEW
 - ★ The lock-in amplifier can also save data in space-saving binary format using Hierarchical Data Format Version 5 (HDF5)



Detector Support Group

Weekly Report, 2019-12-10

- Backed up the Rack 2 (HDicePC2) NMR control software and drivers prior to Windows 10 upgrade.

Hall B – LTCC

- Replaced gas system UPS on Forward Carriage

Hall B – RICH

- Developed design and specifications of components for RICH dry boxes' alarm system
 - ★ System designed to alarm and notify if dry box temperature or humidity are out of user-defined limits
 - ★ Based on Hardware Interlock Systems used on RICH N2 & EP, FT, and SVT
 - ★ Uses cRIO processor and modules. Programmed in LabVIEW
 - ★ Will also monitor dry boxes' UPS units

Hall C

- RTD cables for polarized 3He target
 - ★ Fabricating 20 two wire RTDs with four magnet wires
 - ★ Cut 10 bundles and ordered sensors

Hall C – CAEN HV Testing

- Generated Excel workbook to keep track of testing status for both crates (*hvcaentest2* and *hvcaentest3*) and all HV boards
- Wrote GECO 2020 script for “Fully Populated Ramp Up/Down Test: [No Load]”
 - ★ Script ramps all channels for all boards up and down from 0 V to 1500 V for 150 cycles with a 10s dwell time at each voltage set point

Crate #2: hvcaentest2								
Date Started	Date Completed	Test Type	Control	Monitoring	Data Logging	Results	Comments	Notes
12/12/2019		Fully Populated [No Load]	GECO	GECO	GECO		3 trials each, 150 ramp ups /downs	1 trial takes approx. 2 hrs.
		Fully Populated [With Load]	GECO	GECO	GECO		3 trials each, 150 ramp ups /downs	
		Fully Populated [No Load]	GECO	GECO/EPICS	GECO/EPICS		3 trials each, 150 ramp ups /downs	
		Fully Populated [With Load]	GECO	GECO/EPICS	GECO/EPICS		3 trials each, 150 ramp ups /downs	
		Fully Populated [No Load]	EPICS	EPICS	EPICS		3 trials each, 150 ramp ups /downs	
		Fully Populated [With Load]	EPICS	EPICS	EPICS		3 trials each, 150 ramp ups /downs	
		Stability Test [With Load]	GECO	GECO	GECO		24 Hrs at 0 V and 1500 V	
		Stability Test [With Load]	EPICS	EPICS	EPICS		24 Hrs at 0 V and 1500 V	
		LabVIEW and DMM					Acceptance of modules	
		Fully Populated [With Load]	GECO	LabVIEW	LabVIEW/GECO			

Testing overview for crate #2: *hvcaentest2*.

- Modified multiplexer code to run a single channel as an additional option to the choices to run 24 or 36 channels.
 - ★ Instead of switching between channels, the channel is selected before the data acquisition loop starts, and the program runs until it times out

DSG

- DSG now has its own logbook, which can be found at <https://logbooks.jlab.org/book/dsg-logbooks>



Detector Support Group

Weekly Report, 2019-12-10

DSG R&D – EPICS Data Logger

- Timestamped PV data is now sent directly to the MySQL database
 - ★ Data is searchable using standard SQL statements
- Installed data logger on *dsg-linux2* (Hall A subnet) and *dsg-b-linux1* (Hall B subnet)
- Investigating table size limitations for MySQL
 - ★ This will determine how often archived data will need to be purged

DSG R&D – Multi-Sensor Excitation Low Voltage (MSELV) Chassis sbRIO

- Implemented FPGA read/write subVIs into LV cRIO program
 - ★ subVIs take place of serial read/write subVIs since sbRIO communicates directly to ADCs and DACs
 - ★ Successfully tested the PT100 temperature sensor inputs to the MSELV Chassis
- Investigated remote web interface options for sbRIO
 - ★ Web interface would give user ability to change configuration files or check MSELV Chassis via a web browser
 - ★ sbRIO has built-in functionality to replicate a VI's front panel for access through a web browser, however, browser plug-in required is not supported by most browsers
 - ★ Alternative is to create a web server on sbRIO that hosts an HTML page where values from sbRIO are displayed using Javascript
- Developed test web server, HTML file, and Javascript file for sbRIO to display sensor values read by MSELV Chassis

Cerenox		PT100		Load Cell		Strain Gauge		Hall Sensor	
1	325	1	36.7227115246683	1	552.87711285202	1	0.00290660820221	1	0.00036887276743
2	325	2	32.6500722484273	2	382.874604875145	2	0.0014489626982		
3	325	3	38.5002136154187	3	112.799107543577	3	0.00085606980097		
4	325	4	39.272518138605	4	123.987168704922	4	0.00106832793898		
5	325	5	34.1222254286618	5	0	5	0.00157721017095		
6	325	6	35.9694610400179	6	550.336642349146	6	0.10439925213294		
7	325	7	33.4229723758087			7	0.00171928904793		
8	325	8	41.2233117723461			8	0.00116727951273		
9	325	9	38.3996573217004						
10	325	10	39.643889971812						
11	325	11	34.9584362587247						
12	325								
13	325								
14	325								
15	325								
16	325								

Screenshot of webpage hosted on sbRIO.

DSG R&D – RICH

- Prototyping of the Sensirion SHT85 integrated temperature/humidity sensor power supply distribution scheme, interconnects, and signal distribution for the sbRIO
 - ★ Designed prototype sbRIO signal interface
 - Provides termination, sensor power, and clock and data connections between sbRIO FPGA and RJ45 distribution panel
 - ★ Fabricated prototype RIO Mezzanine Card (RMC) interface and for sensor signal tests for RJ45 power and sensor signal distribution