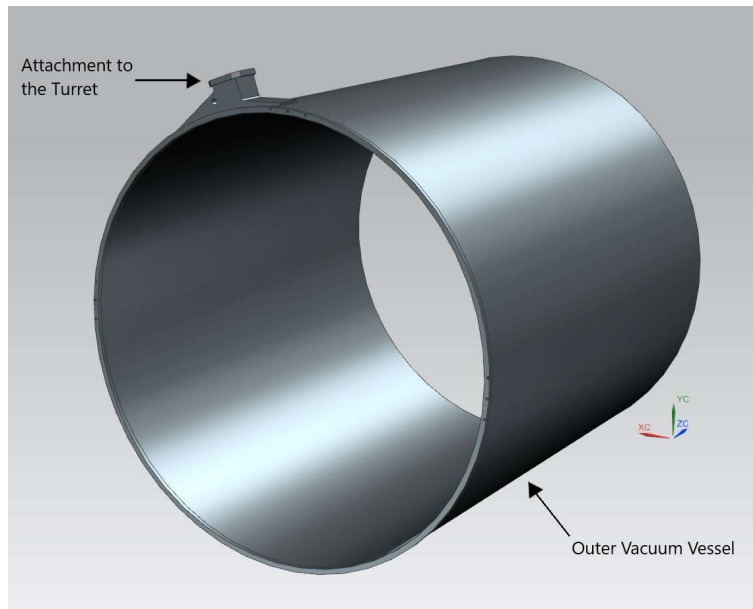# Summary

Hall A – SoLID Magnet Controls

- Completed *Interconnect System* (Overview of connections) in AutoCAD
- Completed HMI screen to show temperature sensors readout at the Neck of the magnet
- Developing NX12 3D view of the Solenoid vacuum vessel to show radial and axial load cell sensors locations

NX12 isometric view of the Solenoid outer vacuum vessel under development

- Developed PLC code to monitor temperatures in the SoLID magnet
- Generated table to show the map of the temperature sensors readout from its CCS connections with the PLC
- Generated PLC layout for PLC chassis remote #2
  - ✶ PLC layout shows the added signals required for the control and monitoring of the service tower's instrumentation
- Redesigned CCS schematic to operate using a single 24V input power

Hall A – BigBite Shower Calorimeter

- Completed termination of one 34-contact coax ribbon cable to twisted-pair ribbon cable Started second of 10 cables

Pairs soldered   Pairs with heat shrink

Hall B RTPC
- Tested full length (50') cables for hall operation of the MFC and pressure transducers

Hall B BoNuS
- Installed stand-alone cRIO in Hall and connected sensors to it
- Tested gas panel in the Hall, found that it would not maintain pressure in target side
  - ✷ Debugging issue

Hall B SVT
- Disconnected detector's cables from its power supply crates, environmental readout patch panel, and VXS crate
- Debugged Hardware Interlock LabVIEW program
  - ✷ Noticed interlock disable/enable control buttons for HFCB temperature – R2 and R3 were not working from EPICS controls GUI
  - ✷ Solved issues by assigning proper names to the LabVIEW variables linked to the EPICS PVs

Hall B HDice
- Installed *HDicepc2* in Rack # 2 and tested NMR and FRS programs
- Fabricated cable, N (connector) to BNC

Hall B RICH
- Researched fiber-optic cable, compact USB spectrometer, and stabilized source that could be used to improve reflectivity test station

Hall C – Magnet Screen Conversion
- Developing *Q1 PSU Setup* CSS-BOY screen
  - ✷ Used LabVIEW EPICS server with the test PVs to test the input and read-back functionality of the screen
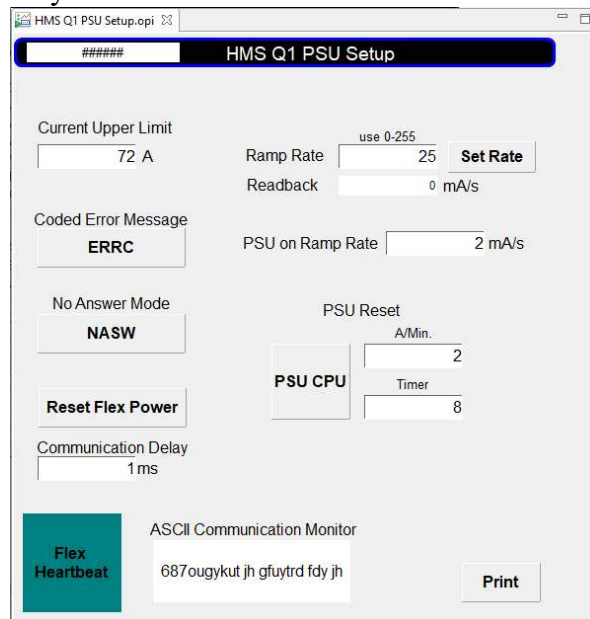
HMS Q1 PSU Setup CSS-BOY screen under development

Hall C – Polarized 3He Target
- Prepped all four pairs of wire for additional RTD magnet wire cable

Hall C – CAEN HV Hardware Testing
- Completed a stability test on A7030TN board #173 with load at 1500 V to check that connected load box didn't overheat
  * All channels on board stayed within ± 1 V of the set voltage for the duration of the test
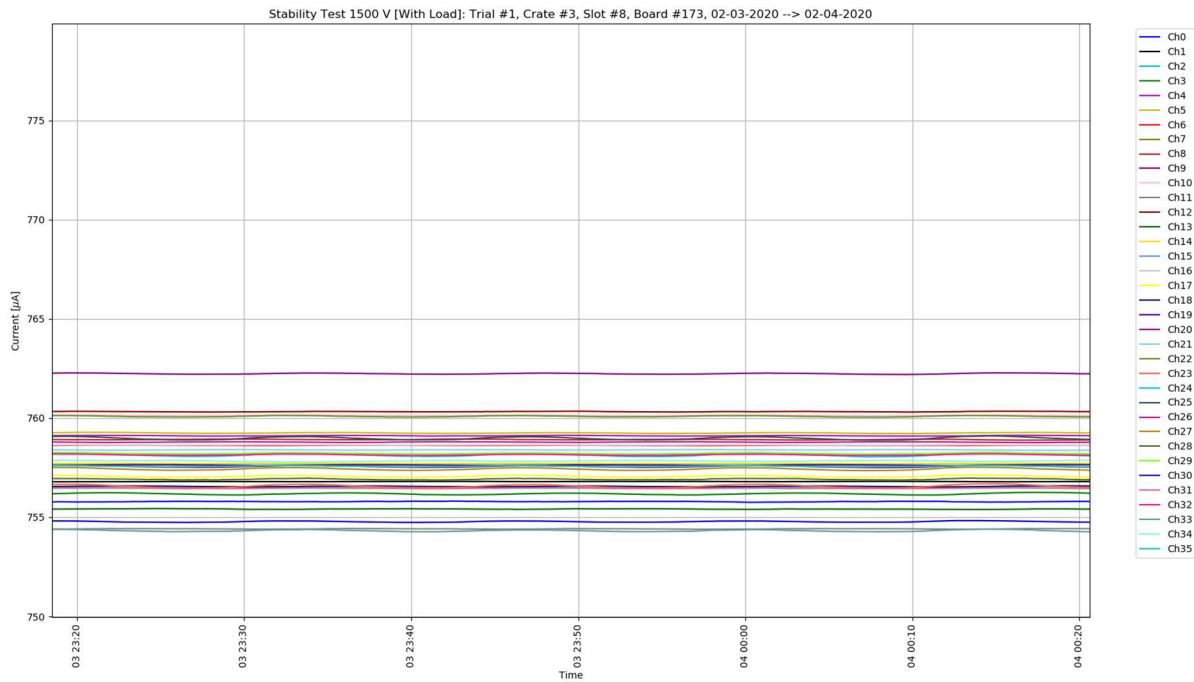 * Measured current values were close to calculated value

Figure shows the current for all channels on board #173. The calculated current value was ~750 µA, actual Imon values during test were slightly higher

Hall D – WEDM
- Investigated way to display Solenoid Interlock's SOE status indicators so first tripped interlock displays as red and any subsequent trips as yellow

DSG R&D – RICH
- Developing and integrating the sbRIO-9627 hardware and software into the Hardware Interlock System for the next RICH sector
  * sbRio-9627 supports 48 SHT85 combined temperature and humidity sensors for the RICH N2 and EP
  * Integrating the SHT85 FPGA Command Engine (FCE) and System Scan Engine into the Hardware Interlock System software

DSG R&D – MSELV Chassis

- Debugged PT100 readout board
- Added PLC communication to sbRIO
  - ✦ sbRIO moved to Hall C Development subnet to be able to talk to DSG's ControlLogix PLC
  - ✦ SubVI written on sbRIO to format and write data to PLC
  - ✦ Routine written on PLC to process data from sbRIO

DSG R&D – EPICS Data Logger

- Compared data from DSG local data logger with MYA and Hardware Interlock Analysis Package (HIAP) data for RICH PV: *B_DET_RICH_INTLK_TEMP11*
  - ✦ Comparison highlights that data archived by the developed local data logger (DSG Local) is more precise than data archived by MYA
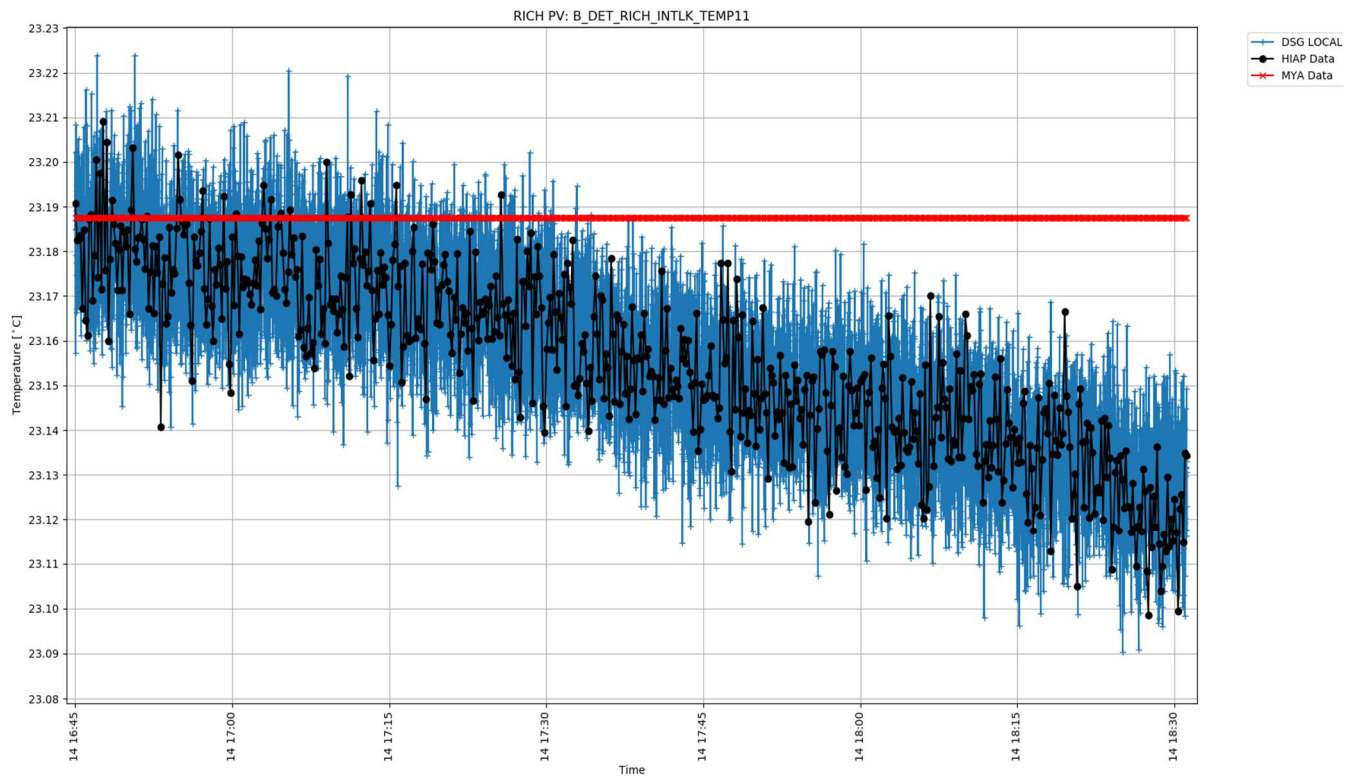

Figure shows the comparison between the three data archiving methods