Detector Support Group
Weekly Report, 2020-03-18

As a group we have done exceptionally well, each one of us should be proud of our effort and our contribution. We seemlesly transitioned to working from home, we did not miss a step. We are collaborating with each other as we did at work. We are supporting the physics runs. Indeed, we are a true representation of America and her determination to succeed, and so we should try very hard not to doubt ouselves, our community, our state, and our country. We shall prevail.

For my part, I've to mention (else, it would be a sin of omission) that I'm *so* privelged to work with such a dynamic, determined, and talented group and for an exceptional supervisor. God bless us all.

Summary

Hall A – SoLID Magnet Controls

- Developing HMI screen for *Cryo Control Reservoir Instrumentation*
- Added additional cables to drawing #0050 (interconnect system)
- Began drawing #0500, wiring diagram for current source module
- Generating parts list for SoLID Magnet Controls Part List
  - ✶ Part list will show all components and instrumentation that will be installed in the instrumentation rack
- Modified *SoLID I&C Diagram*
  - ✶ Diagram shows overview of instrumentation, controls, and communications for the SoLID magnet control system
- Assembling test stand for the Constant Current Source (CCS) boards

Hall A –GEM Gas System

- Received tubing for flow transducer connections

Hall B – HDice

- Developing "Frequency Swept NMR" (fsNMR) program
  - ✶ Work divided into two stages
    - Stage 1 – add multi-scan capabilities, add lock-in amplifier read-back data for X & Y, average cycle data and plot on front panel
    - Stage 2 – add read-back of averaged stored data file capabilities and normalize new incoming data with recalled file data

Hall B - RTPC

- Modified the *MFC Example.vi* to remove nearly all of the controls except for the valve override so that one can manually control the MFC valve
- Made an RTD extension kit and provided instructions on extending the RTD cables so that the cable disconnect will be outside of the Central Vertex Tracker bore

Hall B – SVT/EPICS

- Installed, configured, and tested Phoebus-based CS-Studio
  - ✶ Issues with Java resolved by installing openjdk-13.0.2
  - ✶ Will be used first to revise control and monitoring screens for SVT Hardware Interlock System

Hall C – CAEN HV Hardware Testing

- Continued with ramp up ramp down test with load
- Completed preliminary EPICS testing of the new HiVocs firmware upgrade

Hall C – CS-Studio Screens

- Completed layout of SHMS Q2 PS Setup, Q3 PS Setup, and Status screens
- Setup EPICS server VI in LabVIEW that is used to test the HMS Dipole PSU Internal screen
- Debugged issues with HMS Dipole PSU Internal CSS-BOY screen

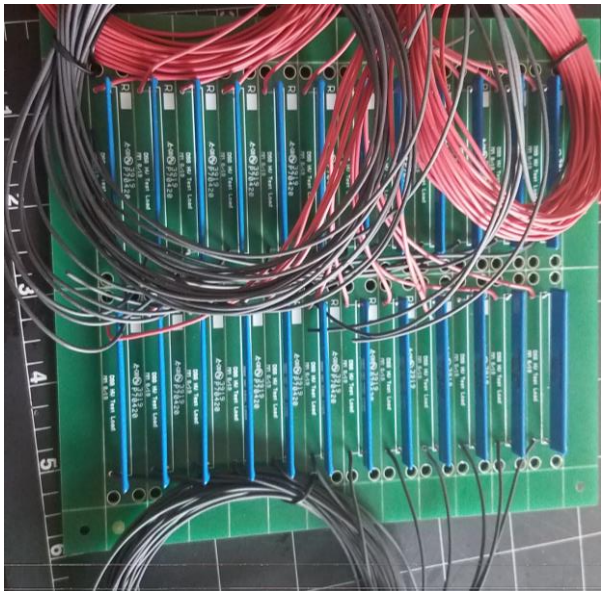
Hall D – PLC

- Researched ways to simulate an Ethernet/IP device to enable development of chiller Ethernet/IP communication to continue without new controller
  - ✶ Investigated using a local Python script or LabVIEW program as fake target for PLC communication

DSG R&D

- Populated second set of HV test load boards to be used in CAEN HV test station

Unpopulated board



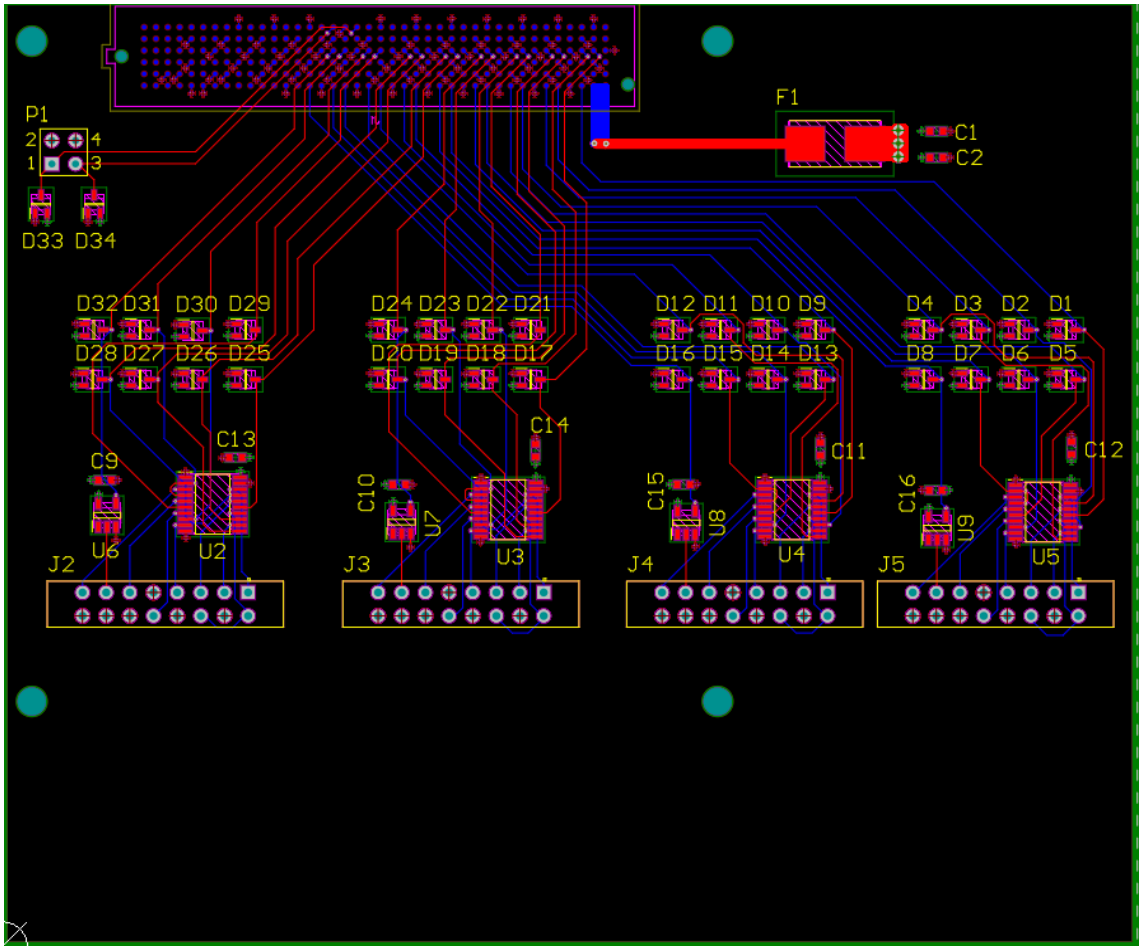
Populated board

DSG R&D – EPICS Data Logger

- Investigating if Grafana can be used to monitor the EPICS testing of the CAEN HV equipment

DSG R&D – MSELV Chassis

- Initial routing of MSELV RMC PCB completed



Real-time Input Output (RIO) Mezzanine Card (RMC) design

- Reviewed RMC design for single board Real-time Input Output(sbRIO)

DSG R&D – PXI

- Updated National Instruments software on host development computer
- Upgraded the PXIe-8840 Quad-Core embedded controller firmware
- Upgraded operating system on PXI controller to NI Real-Time Phar Lap ETS
- Upgraded LabVIEW real-time, drivers, and support software

DSG R&D – RICH

- Hardware development of RMC interface between the sbRIO-FPGA and the 24 dual-sensor temperature/humidity PCBs
  - ✶ Connected prototype board with single-channel I^2C repeater chip to the sbRIO FPGA Digital Input Output (DIO) bus