Detector Support Group

We choose to do these things “not because they are easy, but because they are hard”.

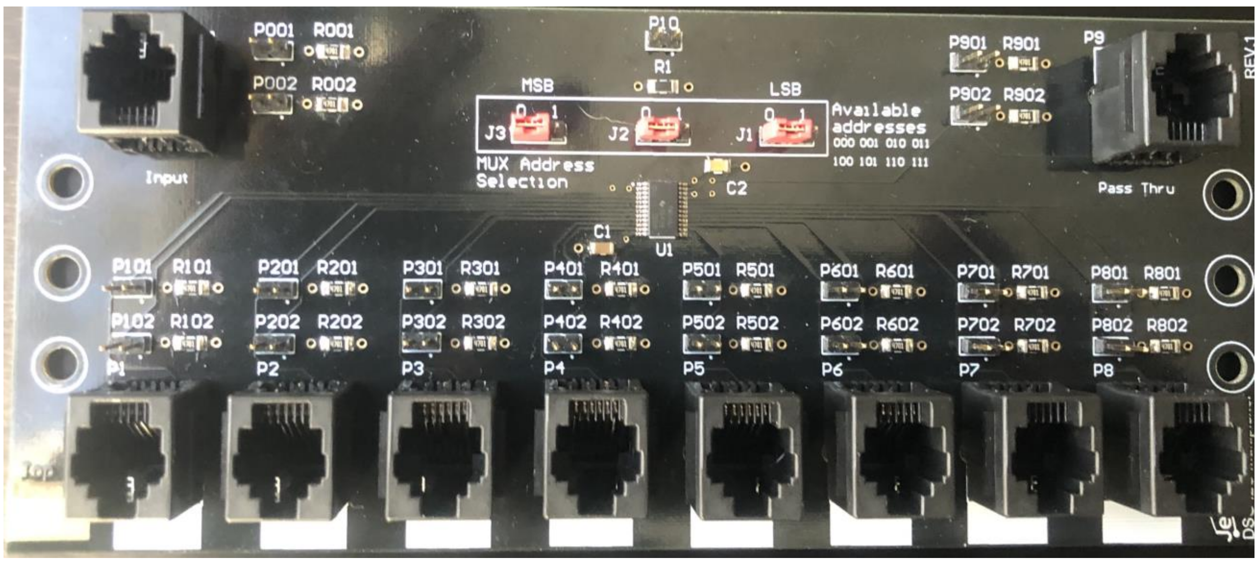
Weekly Report, 2021-06-16

Summary

Hall A – GEM

Mary Ann Antonioli, Peter Bonneau, Brian Eng, George Jacobs, Mindy Leffel, Tyler Lemon, Marc McMullen

- Populated the last of the I^{2}C multiplexer boards – 6 of 6 complete



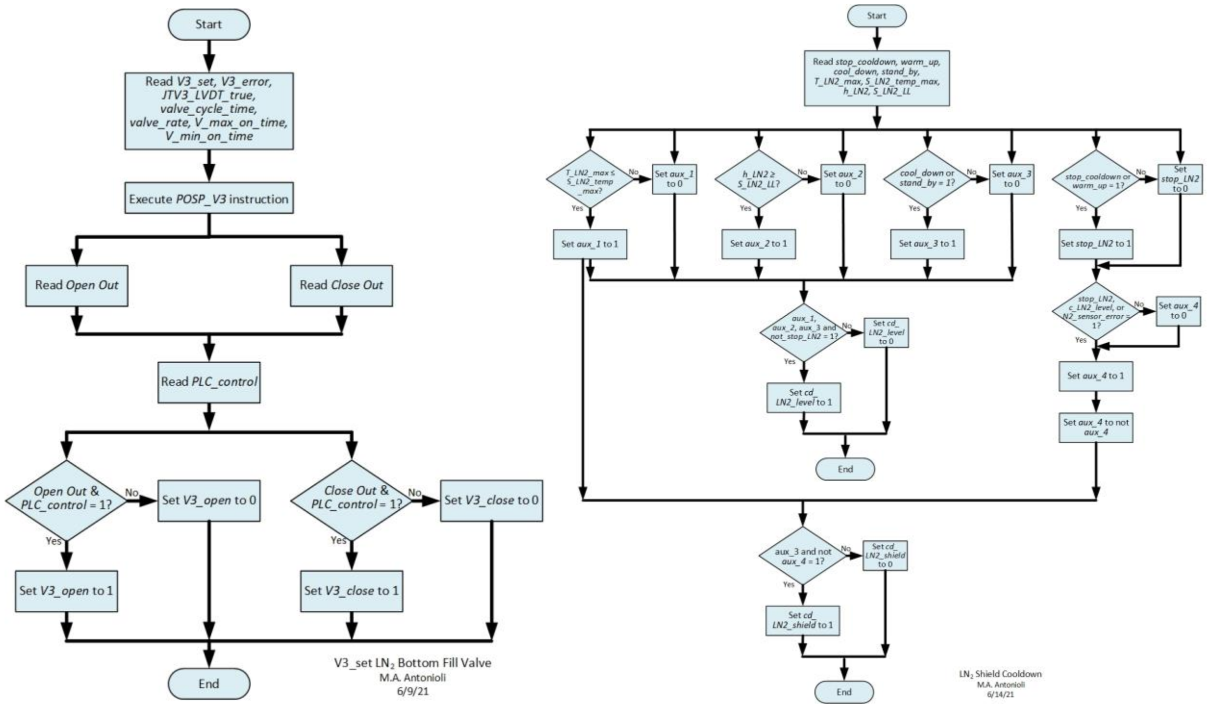
Fully populated multiplexer board for the GEM gas flow sensor chassis

- Fabricated the last gas flow sensor chassis – 6 of 6 complete

Hall A – SoLID

Mary Ann Antonioli, Pablo Campero, Mindy Leffel, Marc McMullen

- Modifying *Instrumentation Rack Drawing* (A00000-16-03-0101)
    - ✶ Added terminal blocks to wire JT and electric ball (EB) valves’ motor drivers
- Completed, and generated PDFs for, electrical drawings: *CCR JT and EB Valves Cable Diagram, Linear Voltage Differential Transducers (LVDT), LVDT Voltage Readout,* and *Electric Linear Actuator Drive Motors*
- Generated Visio drawings of flowcharts for *V3_set LN$_2$ Bottom Fill Valve* and *LN$_2$ Shield Cooldown*



Flowcharts for V3_set LN_2 Bottom Fill Valve (left) and LN_2 Shield Cooldown (right)

- Procured cables, connectors, and tooling for current lead, heat exchanger, and LVDT

Hall B – Magnets

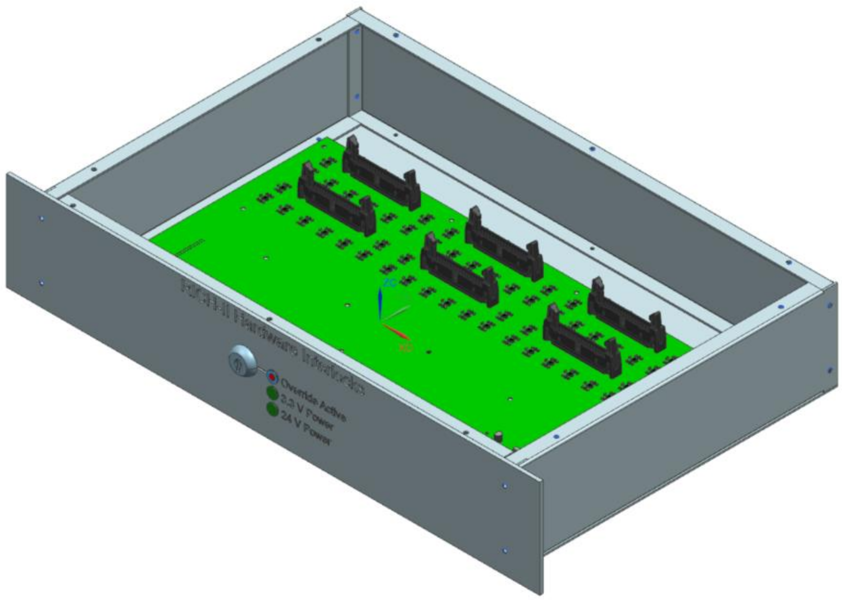
Tyler Lemon

- Repeated Solenoid pre-power-up instrumentation checks before full-power test

Hall B – RICH-II

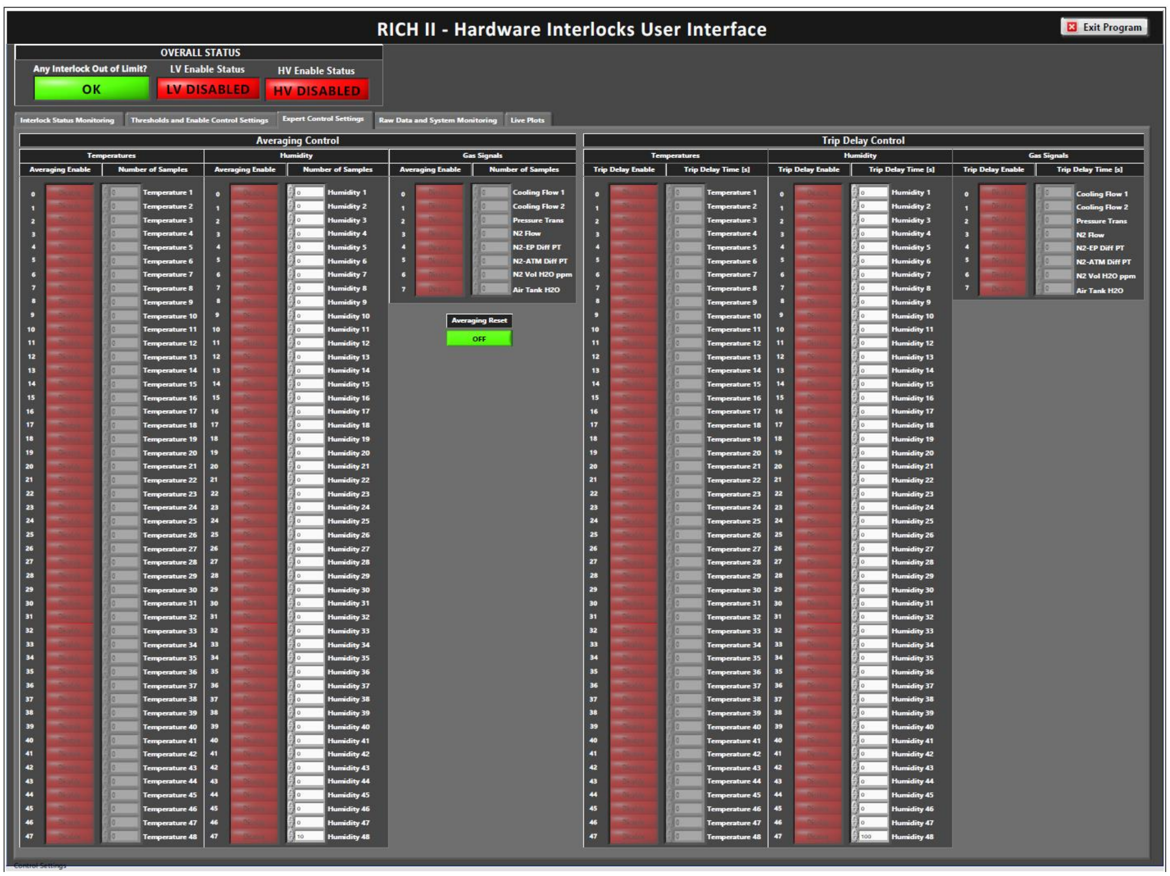
Mary Ann Antonioli, Peter Bonneau, Pablo Campero, Tyler Lemon

- Analyzing, using ANSYS, thermal heat generation of sbRIO-9629
- Developing ANSYS thermal simulation for electronic panels
  - ✶ Simulated convective heat transfer from air at 20°C in the interior of base panel and nitrogen gas in the exterior at 10°C
- Developing design of hardware interlock system chassis, using NX12, to house sbRIO, RMC, and backplane PCB
  - ✶ Chassis includes keyed override switch and LED indicators for override status, 3.3 V power status, and 24 V power status



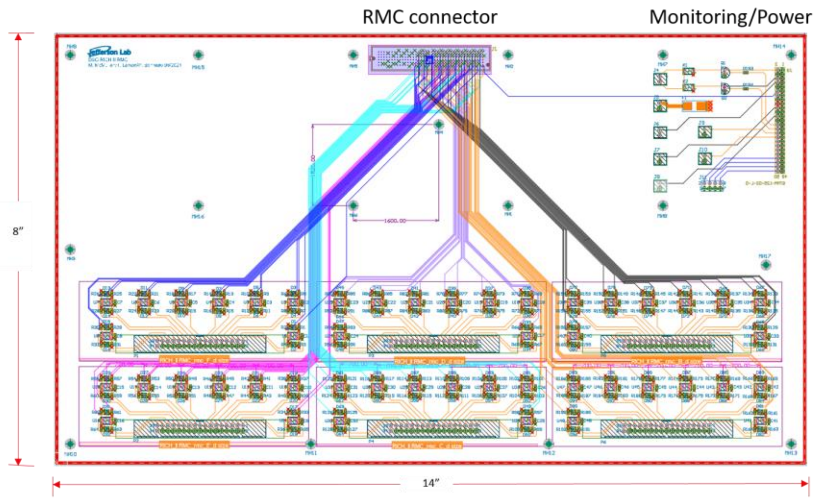
Isometric view of interlock chassis in NX12

- Developing LabVIEW front panel for the Hardware Interlock System program



Screenshot of LabVIEW front panel for RICH-II Hardware Interlock System program

- Developing RMC PCB for hardware interlock system
    - ✶ Added input/output headers to schematic and started placement and routing of components

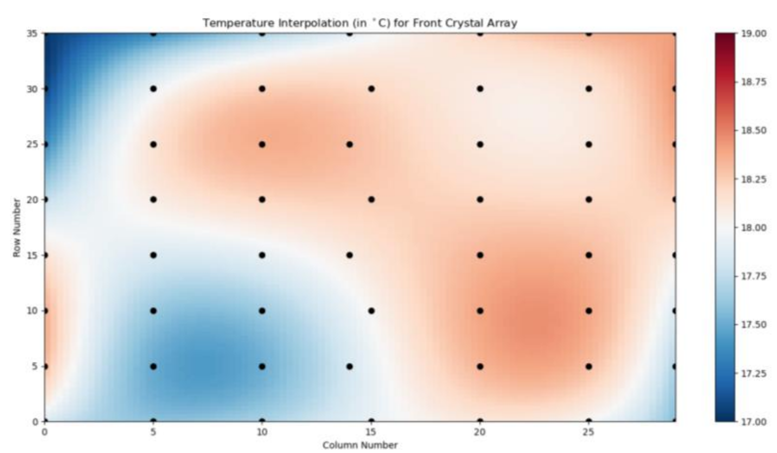


Connectors to Backplane PCB

<u>Hall C – NPS</u>

<u>Mary Ann Antonioli, Peter Bonneau, Aaron Brown, Pablo Campero, Brian Eng, George Jacobs, Mindy Leffel, Tyler Lemon, Marc McMullen</u>

- Developing code for averaging and displaying crystal zone cooling circuit temperatures for LabVIEW Hardware Interlock System program
- Generated surface plot, using Python, of front crystal zone temperatures
    - ✶ Plot was created using randomly generated temperature values 17°C ≤ T ≤ 19°C for the 56 temperature sensors in the front crystal zone
    - ✶ A bivariate spline interpolation was used to estimate the temperature values between sensors



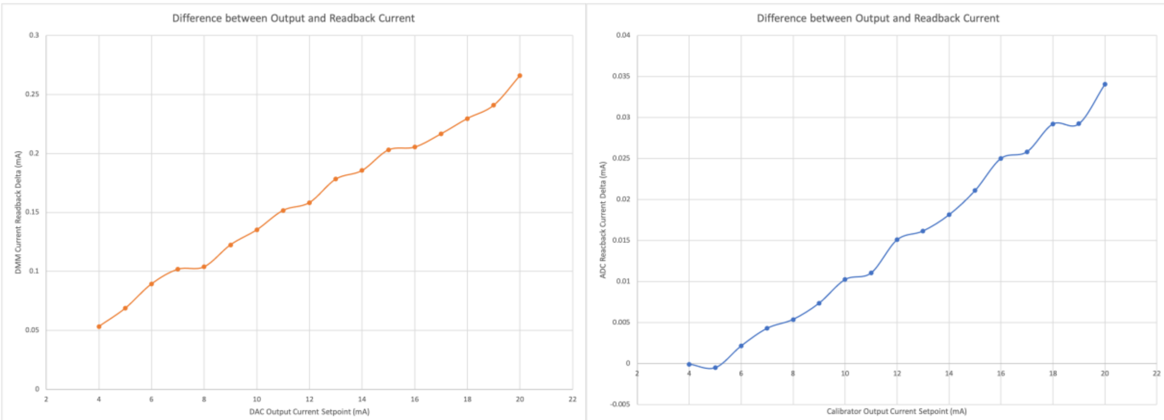
Temperature map of front crystal zone generated using random numbers

- Developed spreadsheet to detail number of multiplexers used for Keysight scanning program and the type and number of sensors connected to each multiplexer
- Fabricated the last of the HV supply cables: 40 of 40 complete
- Long-term load testing of HV supply cables: 26 of 40 complete

DSG R&D - GEM

Brian Eng

- Tested DAC and ADC Raspberry Pi add-on boards with calibrator and DMM
- Found that error (current input and output being off by ~0.5%) is due to the DAC whose current output tends to drift upward over time
- The ADC performs much better, comparatively, which is the only board needed to read the differential pressure sensors



Plots showing ΔI between DAC output current and DMM readback current (left) and between calibrator output current and ADC readback current (right)