



Detector Support Group

We choose to do these things "not because they are easy, but because they are hard".

Weekly Report, 2021-07-28

Summary

Hall A – SoLID

Mary Ann Antonioli, Pablo Campero, Brian Eng, Mindy Leffel, Marc McMullen

- Generated electrical drawing: *PLC Relay Module, Remote B, Slot 2 Wiring Diagram*
- Updated *Cable List* spreadsheet; added basic specifications required for cables to connect
 - ★ Motor Drive signals from PLC-TS (Terminal Strip) to PLC-TB (Terminal Block) for heat exchanger valves
 - ★ Temperature sensor signals from 5 VDC power supply to Dataforth backplane

Hall B – Magnets

Pablo Campero, Brian Eng

- Debugged Torus PLC, Solenoid Cryocon #1, and Distribution Box PLC communication faults due to power outage: <https://logbooks.jlab.org/entry/3888214>

Hall B – MVT Gas

Brian Eng

- Debugged communication issues due to power outage:
<https://logbooks.jlab.org/entry/3888754>

Hall B – RICH-II

Mary Ann Antonioli, Peter Bonneau, Pablo Campero, Brian Eng, George Jacobs, Tyler Lemon, Marc McMullen

- Developed interface between hardware interlock system's sbRIO card and the expansion chassis
 - ★ Currently, data is shown as raw voltage or current; will be converted to flow (L/min) or pressure (psi)
- Developing Hardware Interlock LabVIEW User Interface
 - ★ Added new tab to monitor and control SHT-35 sensors
 - ★ Added indicators and control buttons for all 48 sensors; configured buttons to reset and clear status of 48 sensors at once
- Completed initial routing of the backplane PCB, started on design changes
 - ★ Redesigned RJ-45 LED circuit
 - ★ The LEDs on the RJ-45 connectors will now be used to monitor the sensor communication activity
- Developing air cooling P&I diagram and components list

Hall C – NPS

Mary Ann Antonioli, Peter Bonneau, Aaron Brown, Pablo Campero, Brian Eng, George Jacobs, Mindy Leffel, Tyler Lemon, Marc McMullen

- Generated MySQL database for CAEN HV module testing analysis plots
- Researching methods of embedding a MySQL database within webpage
- Revised Hardware Interlock System program LabVIEW front panel



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- ★ Added temperature limit to both crystal zones (front and back) and the crystal zone cooling circuit
 - Each crystal zone has: high-high, high, low, and low-low temperature limits to control LED indicator colors

nperatures		Back Temperatures	Cooling Circuit Temperatures	Temperature Map	Plots	Expert Settings
Front Crystal Zone Temperatures		Back Crystal Zone Temperatures	Cooling Circuit Temperatures			
Front Crystal Zone Temperature Alarm Limits [C°]						
# of pts. to average	crystal	low-low	low	high	high-high	crystal
100	0	13.0	16.0	20.0	22.0	540
run type	5	13.0	16.0	20.0	22.0	550
random numbers	10	13.0	16.0	20.0	22.0	560
random # bounds	15	13.0	16.0	20.0	22.0	570
lower bound	20	13.0	16.0	20.0	22.0	684
11.0	25	13.0	16.0	20.0	22.0	689
upper bound	30	13.0	16.0	20.0	22.0	694
25.0	35	13.0	16.0	20.0	22.0	699
	180	13.0	16.0	20.0	22.0	704

Screenshot of Expert Settings tab's Front Crystal Zone Temperature Alarm Limits tab from front panel for Hardware Interlock System LabVIEW program

- Completed long-term load testing of HV supply cables
- Repaired 35 HV supply cable wires; labeled 20 of 40 cables

EIC

Brian Eng

- Working on a more detailed schedule for Silicon, Time Projection Chamber (TPC), and Micro-Pattern Gas Detector (MPGD)

SAFETY – POAM 10 Implementation Team

Marc McMullen

- Discussed roll-out of application to the lab; Electrical Safety Group is planning a multilevel outreach to inform workers