Detector Support Group

We choose to do these things "not because they are easy, but because they are hard".

Weekly Report, 2021-09-15

Summary

DSG Projects

1. Hall B
    1. RICH
2. Hall A
    1. SoLID
    2. ECal
    3. Detector HV Controls and Monitoring with EPICS (Phoebus)
    4. SBS and BBS
3. Hall C
    1. NPS
4. EIC
    1. Ansys Analysis of Beam Pipe
5. DSG R&D
    1. MySQL Database
    2. PLC PID Analysis
    3. EPICS Alarm Handler
    4. PCI-based DAQ System

Hall A - Detectors

Brian Eng

- Developing Python script to import map files for multiple detectors instead of just SBS and generate EPICS Phoebus screens

Hall A – GEM

Mindy Leffel

- Populated second of two I^2C test boards

Hall A – SoLID

Mary Ann Antonioli, Pablo Campero, Brian Eng, Mindy Leffel, Marc McMullen

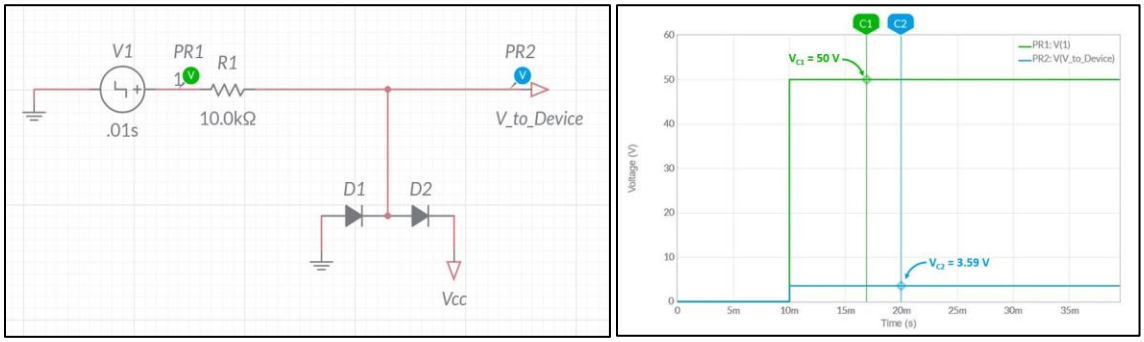
- Completed drawing A00000-16-03-350 *Power Distribution Wiring Diagram*
- Modifying Instrumentation Rack layout based on changes done for power distribution
    - ✶ Changed locations for circuit breakers
    - ✶ Added extra terminal strips and 24 VDC power supply
    - ✶ Added DIN-rail to add extra instrumentation
- Cut three 20-conductor ferrule-to-ferrule cables; terminated 21 of 24

Ferrule-to-ferrule cables with cut (left), stripped (center), and terminated (right) ends

Hall B – RICH-II

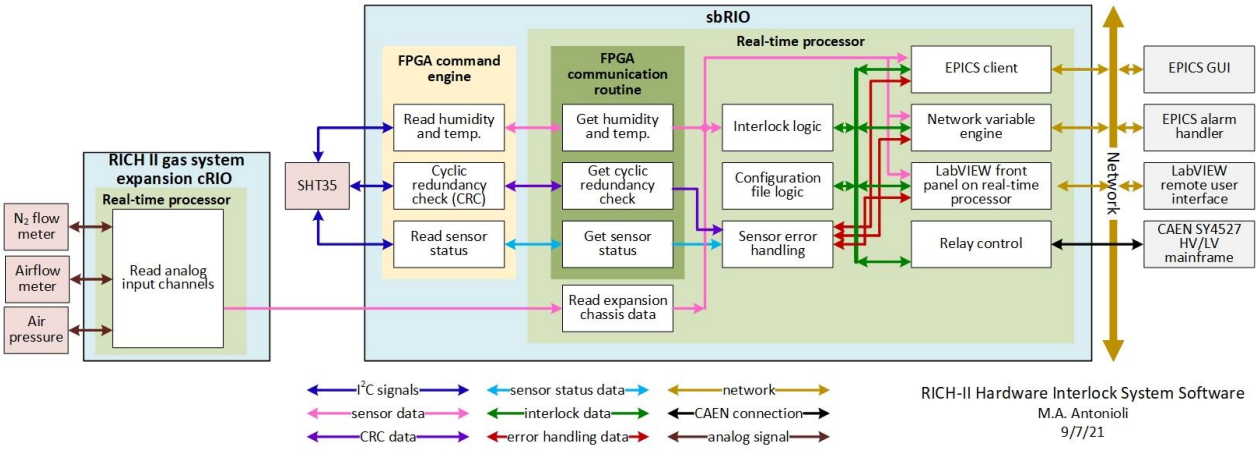
Mary Ann Antonioli, Peter Bonneau, Pablo Campero, Brian Eng, George Jacobs, Tyler Lemon, Marc McMullen

- Conducting simulation of the RMC's Schottky diode circuit using Multisim Live (a SPICE-based, online simulator from NI)
  - ✶ Input voltage is a 50 V step
  - ✶ Simulation shows that while the voltage input to the circuit can be large, the voltage level at the device will stay ~3.3 V



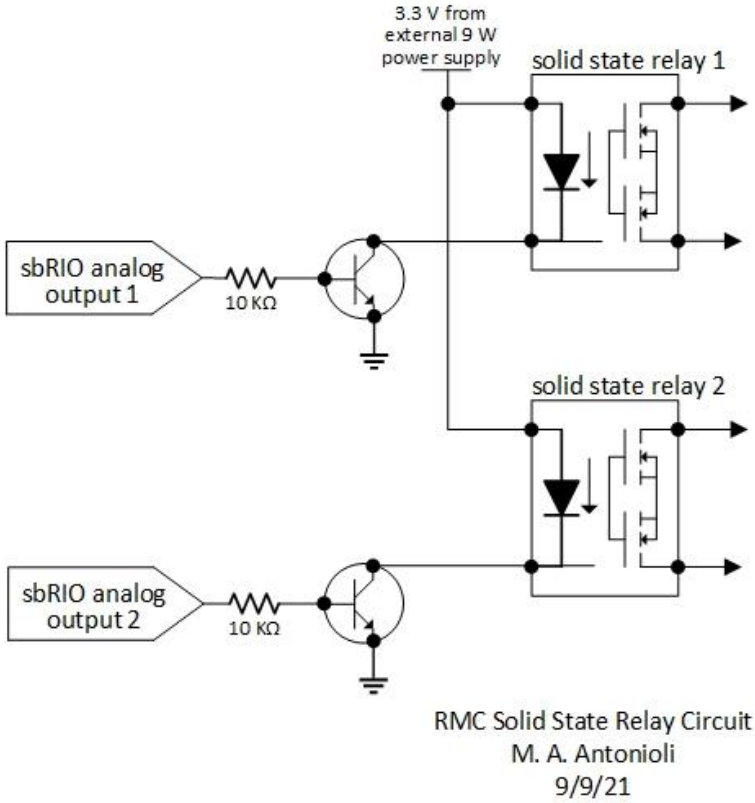
On left, schematic used in Multisim Live. On right, plot of voltage during simulation; green plot is input voltage, blue plot is voltage at device (sbRIO or buffer driver)

- Developed signal map for the hardware interlock system to aide in the development of RMC/sbRIO software
- Revised *Hardware Interlock System Software* Visio drawing



Visio drawing of the RICH-II Hardware Interlock System software

- Generated Visio drawing of the RMC Solid State Relay Circuit

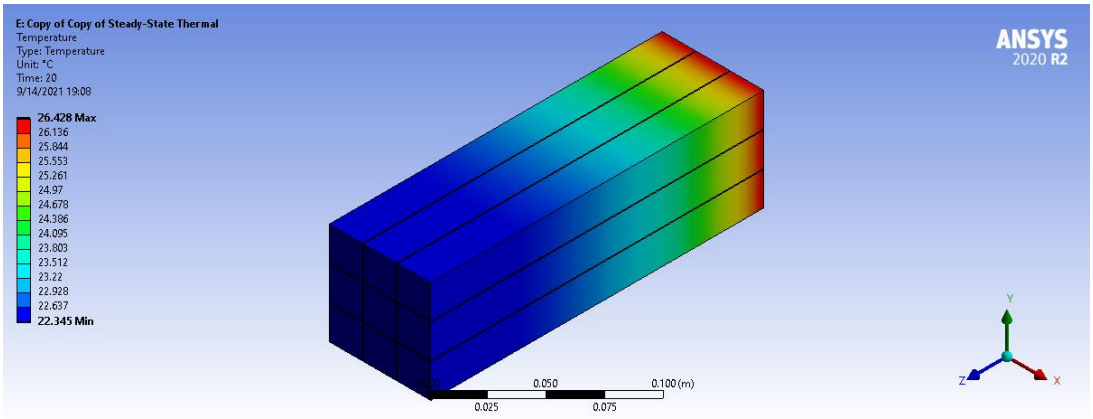


Visio drawing of the RMC Solid State Relay circuit

Hall C – NPS

Mary Ann Antonioli, Peter Bonneau, Aaron Brown, Pablo Campero, Brian Eng, George Jacobs, Mindy Leffel, Tyler Lemon, Marc McMullen

- Developed new model of 3x3 block of $PbWO_4$ crystals without carbon fiber dividers and cooling Cu shell
  - ✶ Analysis conducted using 0.5 W heat load on rear face of each crystal
  - ✶ All components have a film coefficient of 2.5 $W/m^2 \cdot °C$
  - ✶ Front face is at 22°C and the rear face is at 26°C



Screenshot of 3x3 block of $PbWO_4$ crystals with no dividers and no copper cooling shell

- Modified LabVIEW Hardware Interlock Monitoring program
  - ✶ Added detector house temperatures to the *Detector House and Hall Temperatures* tab
  - ✶ Developing map of absolute value of temperature difference between front and back crystal zone temperature sensors
- Developed Phoebus EPICS Temperature Maps screen with embedded Python script to generate random numbers
  - ✶ Maps for readback temperatures of sensors in front and back of crystal array, for difference between front and back temperatures, and for temperature deviation from operating temperature of 18°C
- Developed diagram of HV Supply cable test stand for testing readback voltage
  - ✶ A Krohn-Hite voltage calibrator will supply voltage to cable housed in a plastic enclosure
  - ✶ Voltage will be measured at unterminated end with a Keithley 2001 DMM

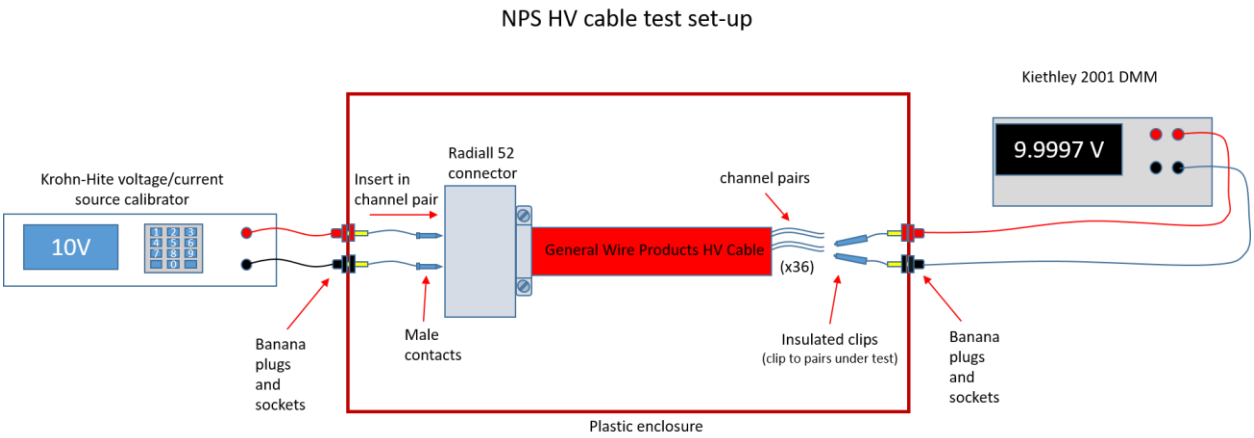


Diagram of HV supply cable test stand

EIC

Pablo Campero, Brian Eng

- Started thermal analysis for beam pipe and silicon tracker – using NX12, reviewed Vertex detector and support
- Attended ATHENA and ECCE tracking working group meetings – both presented updated designs with Micro Pattern Gas Detector (MPGD) as outer tracking layers (no TPC)

DSG R&D – NPS

Peter Bonneau

- Investigating the readout and control of the Keysight switch/measurement unit using Python

DSG R&D – SoLID

Pablo Campero

- Developing PLC code to simulate PID control over the valves
- Generating HMI screen to facilitate controls and monitoring of the simulation