Brookhaven National Laboratory

Simplified LGAD structure with fine pixelation

Gabriele Giacomini (PI), Wei Chen, Gabriele D'Amen, Enrico Rossi, Alessandro Tricoli
Brookhaven National Laboratory
535B, Brookhaven National Laboratory, Upton, NY, 11973
giacomini@bnl.gov

Simone Mazza, Jennifer Ott, Bruce Schumm (co-PI)
University of California at Santa Cruz
1156 High Street, Santa Cruz, CA 95064
baschumm@ucsc.edu

July 25th 2022

ABSTRACT

Low-Gain Avalanche Diodes are widely studied silicon sensors which are characterized by an internal moderate gain that enhances the signal amplitude induced by mips and by fast signals: because of these two properties LGADs have excellent timing performance. For example, they will be used in the next upgrades of the ATLAS and CMS detectors at the High Luminosity Large Hadron Collider (HL-LHC) at CERN in their timing detectors. However, to achieve a spatially uniform multiplication a large pixel pitch is needed, preventing a fine spatial resolution. To overcome this limitation, the AC-coupled LGAD approach was introduced and other LGAD-based sensors are under development, towards detectors with 100% fill factor that can simultaneously provide excellent timing and spatial resolution. AC-LGADs are the established baseline sensors for some detectors of EIC (for example Roman Pots) and their suitability for other detectors is presently under study. With this proposal we plan to fabricate and test a novel device based on the LGAD concept, which overcomes some limitations of the AC-LGADs and can therefore be of interest for some EIC detectors, other than the Roman Pots. As the AC-LGAD, it features 100% fill factor, good spatial and timing resolution, while potentially having a simplified fabrication process in clean room.

Table of Contents

Project Narrative

1. Introduction

It is crucial for some EIC detectors to extract the timing from the events. For example, it is required that each detector plane in the Roman Pots has a timing resolution of about 35ps, for background rejection and reduction of vertex smearing from the crab cavity rotation. Another example is the proposed all-silicon Time-of-Flight, which adds timing layers in the outer tracker. These two examples require 4D silicon detectors, i.e. silicon sensors (and associated electronics) featuring good timing and spatial resolutions.

The Low-gain Avalanche Diode emerged recently as a silicon technology in the HEP horizon for the fast detection of mips, to distinguish events generated in the same bunch crossing but slightly separated in time. The importance of the topic led a vivid and successful research resulting in two timing detectors: the ATLAS HGTD (High-Granularity Timing Detector) and the CMS MTD (Mip Timing Detector). LGADs equipping these two huge detectors have however a granularity of 1.3mm x 1.3mm, hardly the one of a 4D detector. Research has been done and is underway to provide silicon sensors with: 100% fill factor, spatial resolution in the order of a few microns and timing as good as in LGADs (20-30ps).

The sensor baseline of the Roman Pot is the AC-LGAD, capable of the above-mentioned performance. However, some intrinsic limitations may lead to the impossibility to use this technology in other timing detectors at EIC. Clearly, study is still undergoing so that such limitations may be overcome either by design, by technology or by the overall system, but it is wise to look for alternatives to mitigate the risks. One of the alternatives is the Deep-Junction LGAD, which is under fabrication in these days (July 2022). We propose an innovative silicon device concept, again LGAD-based, featuring 100% fill factor, high spatial and timing resolution, as an alternative to the existing 4D silicon detectors, that can be deployed in one or both detectors. Another characteristic is that it should be straightforward to fabricate, for an overall reduction of risks and costs.

2. LGAD

A Low-Gain Avalanche Diode (LGAD) has the structure depicted in Figure 1 [1]. LGADs are based on simple p-n junctions which are engineered to specifically detect mips traversing the substrate. Under the n+ implant, a boron implant is placed (gain layer). Upon depletion of such gain layer, a high electric field develops, high enough to lead electrons to impact ionization, while is kept low-enough to avoid an important multiplication of holes and therefore preventing breakdown (it is an intrinsic property of silicon that ionization coefficients are higher for electrons than for holes (for the same electric field)). As in a conventional diode-based sensor, mips generate electron/hole pairs into the substrate along their track which promptly drift away following the electric field lines. The gain layer multiplies the electrons passing through the high field region by a factor of a few tens. The gain holes drift towards the substrate contact and give origin to most of the signal. The signal is high enough to be read-out even by a fast (and therefore noisier) electronics. If the LGAD is fabricated on thin substrates (the “epitaxial layer-p“ in Figure 1), for example 50um thick, the current pulse is about 1-ns long with a

500ps rise time. So, the main features of this device are the fast and boosted signals that are due to both the thin active silicon substrate and the amplified charge. Timing resolutions of less than 30ps are measured for LGADs 50 um thick, and even less for thinner devices (about 20ps for 20um thick devices)

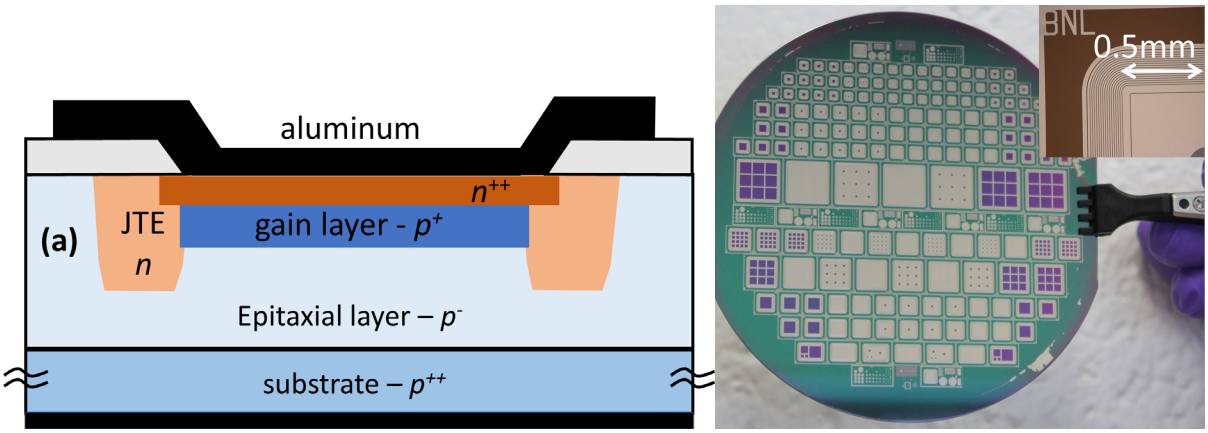

Figure 1. sketch of a section of a Low-Gain Avalanche Diode (LGAD) and picture of one of the first wafers fabricated at BNL.

However simple electrostatic considerations will tell how electrons created in the gap between pixels and at the border of the n+ implant do not go through the high field region created by the depleted gain region but rather are collected at the Junction Termination Extension (JTE, protection structure to avoid breakdown) at the edge of the n+. Therefore, the resulting signal from the inter pad region is small and likely to stay below the threshold for detection. To have a decent fill factor, the pixel lateral dimensions must be much larger than the substrate thickness, preventing a fine pixelation of the LGAD sensors. For example, LGADs for the timing detectors of both ATLAS and CMS are at a pitch of 1.3mm. A 4D detector based on this type of devices is therefore not achievable, as it gives excellent timing performance but very poor spatial resolution.

<u>Problem:</u> LGADs cannot achieve good spatial resolution

3. AC-LGAD

To preserve the excellent timing resolution of the LGADs and add a fine spatial resolution to the same device, other sensors have been developed (or are under development). One of these devices is the AC-coupled LGAD [2], Figure 2.

The AC-LGAD consists of a uniform gain layer that, as in the standard LGAD, is implanted below the n-implant: these two layers run seamlessly overall the active area. A main difference is that, in the AC-LGAD, the large uniform n-implant is about 10 or 100 times less doped than the n+ implant of a standard LGAD. Its sheet resistivity is therefore much larger (in the order of the kOhm/square). The gain layer is implanted in the usual

way as in the case of the LGAD. The n-implant is covered by a thin dielectric layer which is typically silicon oxide, silicon nitride, or both, while it is grounded through a contact at its border. Over the dielectric, there are finely patterned metal electrodes (of arbitrary shape), which will be connected to the read-out electronics. Signals are generated in the usual way and they induce a current pulse to the metal electrodes through the capacitance, whose parallel plates are defined by the metal electrodes and the n+. The high resistivity of the n-layer limits the spreading of the signal to the nearby electrodes; on the other hand, such spreading – inducing a cross talk – can be used to interpolate the hit position. A 100% fill factor has been demonstrated, with uniform multiplication and no dead areas. Since the metal electrodes are separated from the n-layer by an insulator, they do not collect charge and the signal pulse is bipolar. Since two neighbor electrodes see, through the capacitance, a small resistance between them (due to the n layer), they share the signal from charge collected in the n+ layer. On one hand, this increases the position resolution by interpolation of the signal from two or more electrodes. On the other, it increases the occupancy. Therefore AC-LGADs are not suitable in high-rate environments. Moreover, signal sharing in some application has to be avoided.

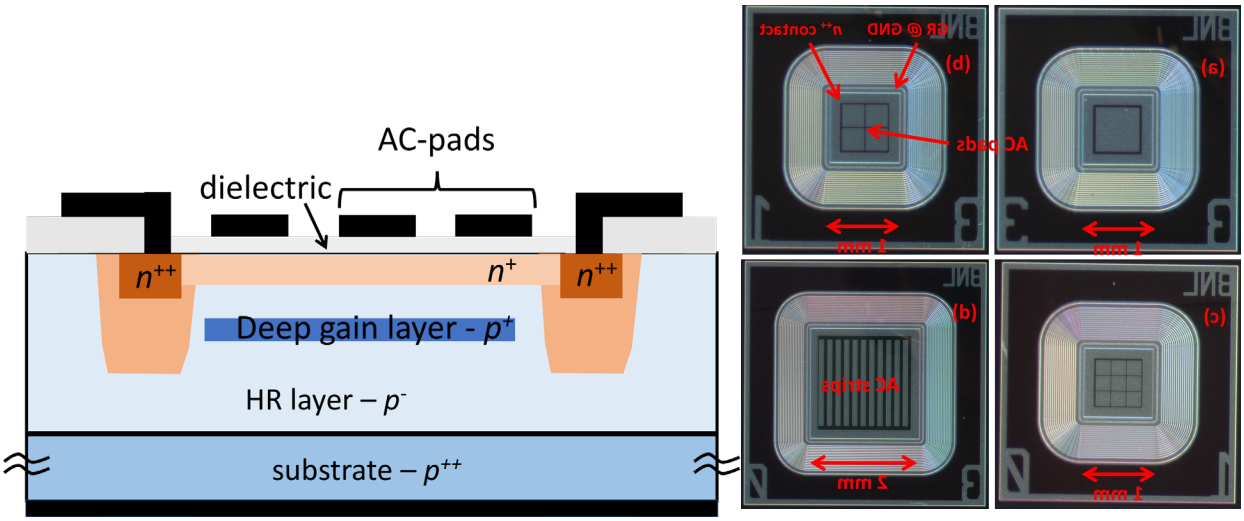

Figure 2. sketch of a section of an AC-LGAD and pictures of a few examples of small-area devices fabricated at BNL.

In beam tests [3], as well in laser based TCT tests in the lab, exceptionally good position resolutions have been measured, down to 1/20th of the pitch in AC-LGAD strip sensors. A very sparse read-out is therefore possible, and an excellent spatial resolution is possible with a limited number of read-out channels. However, in beam tests, it was observed that long strips (order of a few cm, see Figure 3) have lower and slower signals. While these results are preliminary and not fully understood, it is clear that the higher capacitance of the AC-LGADs plays a role. An optimization of the strip and pixel geometry is still ongoing, with prototype sensors routinely fabricated at BNL for test purposes and distributed to the community (FermiLab, Santa Cruz, INFN, University Geneva, Rice, UIC, LANL, etc), and tested with both discrete electronics and ASICs. In any case, AC-LGADs are the baseline detector for the Roman Pots at EIC, where they will be patterned with

pixels at a tentative pitch of 0.5 mm x 0.5 mm, hence presenting low capacitance at the input node. The design of the metal readout will be finalized with the input of on-going tests.

Advantages: 100% fill factor, good timing resolution, excellent spatial resolution

Problems: high occupancy, high capacitance (?)

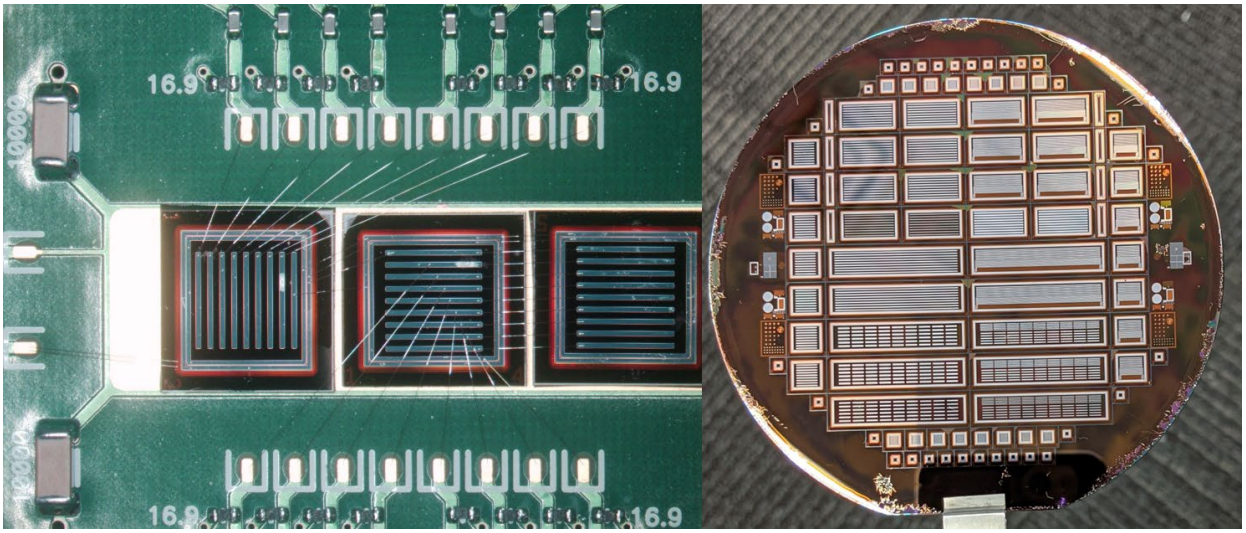

Figure 3. left: AC-LGAD in strip configuration mounted on a 16-ch RF amplifier board (FNAL), as used in test beams. Right: 4" wafer fabricated by BNL and populated with AC-LGAD strips of different length, for test purposes.

4. Deep-Junction LGAD

To prevent a high occupancy and at the same reduce the capacitance of the device, while keeping a 4D detector, the Deep-Junction LGAD was conceived. In a Deep-Junction LGAD (Figure 4), a n-p junction is placed roughly 5um deep into the detector. The junction is built with two highly doped p and n layers (p++ and n++ respectively) that generate a high field region contained in the detector but keeps the electric field low at the surface.

There are several ways to fabricate such a deep junction: in one the P++ region is deposited on the top of a 20-50 um thick high-resistivity p-type silicon wafer (same starting substrate as LGAD and AC-LGAD), then a thickness of a few um of silicon is deposited over it. Another procedure is to implant separately a p and a n wafer with p++ and n++ and then wafer2wafer bond and thin the two wafers to form the deep junction at the desired depth. N+ electrodes are eventually implanted on the top of the wafers and metallized. This multiplication region for the electrons is uniform and 100% fill factor should be achieved. Electrons are multiplied in the high field region of the deep junction and collected by the DC-coupled n+ implant: the spatial resolution is as in a standard silicon strip sensor (with the same S/N) while the timing resolution is the same as in an LGAD. However, the latter statements are theoretically as the fabrication of devices has not been completed yet (as of July 2022, prototypes are set to arrive in August 2022).

The fabrication is carried on by Cactus Materials Inc. under an SBIR Phase II program (UCSC and BNL as sub-contractor) as the fabrication requires not-standard clean-room techniques, namely the deposition of the few microns of epitaxial silicon over the deep junction (or the wafer bonding) which is available at Cactus.

Advantages: 100% fill factor, good timing resolution, good spatial resolution

Problem: device not demonstrated yet

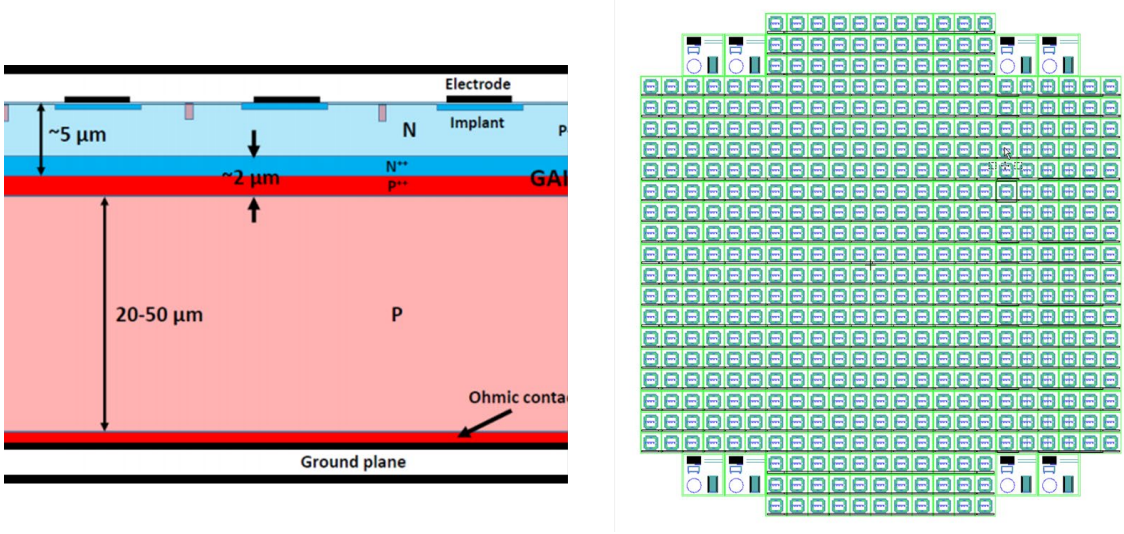

Figure 4. sketch of a section of a Deep-Junction LGAD (DJ-LGAD) and, right, layout of the 4" wafer populated with many small DJ-LGADs, under fabrication at Cactus Materials Inc.

5. A Novel LGAD structure

The structure we propose to develop with this proposal is the following (figure 5):

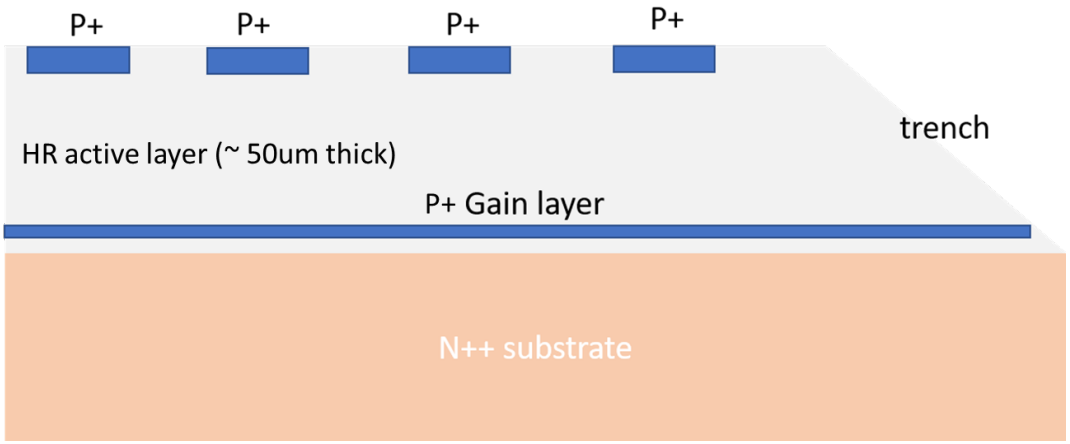

Figure 5. sketch of a section of the new proposed structure, that we aim at fabricating under this proposal.

The handling wafer is a low-resistivity n-type wafer (while in the other LGAD-type device the handling wafer is a low-resistivity p-type). Over it, at about 1-micron or more, the gain layer is placed. This can be achieved, for example, by wafer-bonding a high resistivity p-type wafer where such an implant has been performed in advance. The opposite side of the p-type wafer can then be thinned down to 20-50um and acts as the active thickness of the device, where the mips deposit the electron/hole pairs. P+ electrodes are eventually created on the surface by ion implantation and metallization. Electrons drift down towards the n+ substrate and get multiplied in the high electric field created by the depleted p-gain layer. Gain holes drift up towards the p+ electrodes.

As in the case of the DJ-LGAD, electrodes are DC-coupled. The spatial resolution is the same expected in a regular silicon sensor (given the same S/N and geometry) and timing resolution as in an LGAD with the same doping profiles and applied voltage. We expect therefore good timing and spatial resolution (and, being the gain layer uniform, also 100% fill factor). The capacitance is the same as in a Deep-Junction LGAD and given approximately by the capacitance of the electrode towards the back ($C = \varepsilon$ Area/Thickness) as the interelectrode capacitance is suppressed because of the small thickness of the device (the back acts as an electrostatic shield). Compared to AC-LGADs, it has therefore lower capacitance and no cross-talk.

Moreover, the fabrication is simplified: the starting point is n+ handling substrate, on which a blank-implanted wafer is bonded and thinned down (this step however is not standard and must be outsourced). The rest of the process is just one implantation (p+ implant to define the closely spaced electrodes on the front side (energy not critical)) and – possibly - termination of the structure with (for example) a trench. A trench must have the bevel shown in Figure 5, and this is what it is achieved typically with standard methods (dry or wet). Notice that as the gain layer can be blank and there is only one implantation on the front side of the device, the yield is expected to be quite high and the fabrication, overall, quite cost effective.

TCAD numerical simulations have been conducted and proved the device is working as expected.

This would be a new device in the sensor arena and can be a candidate of 4D detector where AC-LGAD devices are not usable, because of their high crosstalk and occupancy, or their higher capacitance. It will be an alternative to the Deep-Junction LGADs, mitigating the risks of not having an LGAD based sensor which satisfy all the sought-after specifications needed to achieve the physics reach.

Advantages: 100% fill factor, good timing resolution, good spatial resolution, simplified fabrication process.

6. Interaction with Companies

The collaboration of external companies is needed because the first step towards the fabrication of the LGAD device presented in this proposal is wafer-bonding, which is not a common technique usually found in small laboratory-based clean rooms. We are having proficient collaborations with Cactus Materials Inc (Tempe, AZ), which has been granted

a few SBIRs for the prototyping of several LGAD-based devices (Deep-Junction, Deep-Layer LGADs and Double-sided LGADs). One of their expertise is wafer bonding so they are well positioned in fabricating the initial substrates (low-resistivity n-wafer bonded to a high-resistivity wafer, already blank implanted with the gain layer). If the device shows proper functionality, the technology can be transferred to Cactus (initially by means of SBIRs) which has a medium volume fabrication capability and may be able to supply all detectors for the all-silicon TOF and other detectors requiring 4D LGADs with long strips.

7. Towards a monolithic LGAD

It must be noted at this point that this novel LGAD structure can be the baseline for a type of monolithic LGAD built on CMOS technology, and therefore prone to mass fabrication in commercial facilities in a cost-effective, high-yield, low-risk way. It is one of the options that BNL is investigating to create a monolithic LGAD or ACLGAD. In fact, as in the case of the pixel detectors the scientific community has migrated from hybrid structures (sensor bump-bonded to read-out chip) to monolithic devices (sensor embedded in the CMOS substrate), it appears the next logical step in the development of this technology to monolithically integrate the LGAD structure in a CMOS process. To build the LGAD in CMOS technology based on this structure, a standard pixelated CMOS sensor has first to be fabricated on a high-resistivity p-type substrates, where deep p-wells collect the holes and within which all the fast-timing electronics sits. The thick low-resistivity substrate is then removed (by grinding and polishing), and wafer bonded to a n+ wafer over which a gain layer has already been placed (by epitaxy and ion implantation, for example). A sketch is presented in Figure 6. Of course, before engaging in this important step, which is a natural evolution of the LGAD concept, the functionality of the basic structure needs to be proven first.

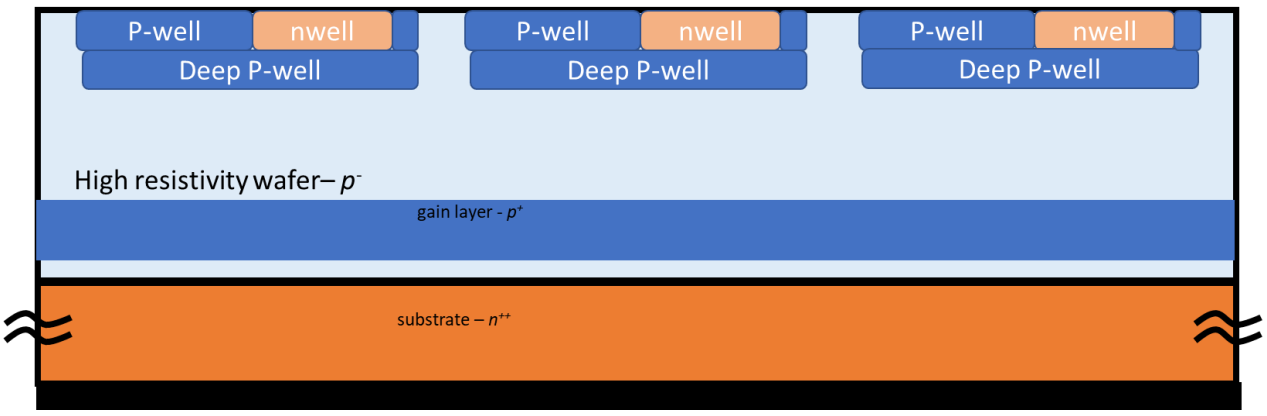

Figure 6. possible section of a monolithic LGAD, based on the new structure.

8. Deliverables and milestones

For the first year of the project (FY23) we foresee the following deliverable:

month 1: design of the photolithographic masks and final decision of the process to follow, with generation of a spreadsheets with the list of the fabrication steps to be performed in clean room. Submission and fabrication of the photolithographic masks to Photronics Inc.

- **Deliverables**: **production of photolithographic masks and definition of the clean-room process**

month 2: preparation of the substrates, ion implantation of the gain layer on one side of the high resistivity wafer. TCAD numerical simulations will dictate the optimal dose and energy, however a few wafers differing for the gain layer dose will be prepared. The full batch will have a few wafers (maximum of 4). We have experience with LGAD fabrication and therefore pinpointing the correct ion-implantation parameters should not be such a hard task. Moreover, for a first fabrication, also a not-optimized device – which however shows some level of amplification – is acceptable as it proves the concept.

- **Deliverables**: **initial wafer ready for wafer-bonded**

month 3-5. Shipment of wafers to an outside company (most likely Cactus Materials Inc.) for wafer bonding and thinning. This may require some months to accomplish because of our low-volume fabrication. In the meantime experience with the trenching of silicon can be acquired.

- **Deliverables**: **wafers bonded together**

month 6. (Conservatively) The rest of the fabrication will be carried on at BNL's clean room. The fabrication requires p+ implant to define the electrodes, contact opening and metallization (three lithographies). On some wafers or on limited parts of it, trenches may be etched. Some wafers instead will be without trench etching to prove if the dry etching step can be skipped at all, to further simplify the process.

- **Deliverables: LGAD devices completed at BNL**

month 7. static testing in the lab (IV-CV) to check basic functionality of the devices

- **Deliverables**: **results of static tests**

month 8 -12. If functional, dicing of a wafer and shipping of working devices to UC Santa Cruz for functional testing (beta scope, TCT). Also at BNL these tests can be carried on in parallel.

- **Deliverables**: **results of functional tests at UCSC**

9. Budget

Budget (full funding)

- Consumables for device fabrication: 10k$

3K$ for lithographic masks, 2k$ for ion implantation, 2k$ for miscellaneous clean room expenses (gas, acids, wipes, etc), 3k$ for PC boards and related components for testing.

- Wafer-bonding process: 15k$
- Personnel:

BNL: 1 month scientist (PI) to coordinate the work and perform studies, 2 months of an engineer to define the process flow in clean room and follow most of the process, 1 month of a technician to follow standard tasks in clean room, 0.5 month for a technician to mount board for tests, 1 month research assistance to conduct the testing.

UCSC: 25k for sensor testing.

	Sensor fabrication	Sensor testing	
BNL	$145k	$45k	$190k
University California at Santa Cruz	N/A	$25k	$25k
	$145k	$70k	**$215k**

Budget scenario (80% full funding)

Testing will be skipped at BNL (0.5 month for a technician to mount board for tests and 1 month research assistance to conduct the testing are not supported).

All deliverable as in full budget, except no testing results will be obtained by BNL and all the testing effort will be carried on by UCSC.

Budget scenario (60% full funding)

Testing will be skipped at BNL (0.5 month for a technician to mount board for tests and 1 month research assistance to conduct the testing are not needed) as in the 80% full-budget scenario.

Important delays in the fabrication are foreseen as time is not allocated for personnel to work specifically on this project. Personnel will be working on other projects and will

work on the present in parallel, time allowing. Fabrication may not be concluded at the end of the FY. Results of the functional characterization of the device may not be concluded in FY23, and carried out in FY24.

In detail, the deliverables are as follows:

1) **month 1-3: production of the photolithographic masks and definition of the clean-room process**

2) **month 4**: **initial wafer ready for wafer-bonded**

3) **month 5-7**. **wafers bonded together**

4) **month 8-9**. **LGAD devices completed at BNL**

5) **month 10: results of static tests at BNL**

6) **month 11 -12: (partial) results of functional test at UCSC**

10. Cost Effectiveness

The fabrication of the present device is simpler than the one of the other versions of LGADs, as it requires a smaller number of lithographic steps. Moreover, as some of the process steps are carried out on blank wafers (gain layer implant, wafer bonding) and the only patterned side of the sensor undergoes one ion-implantation only, there is little room for defects in the process, therefore increasing the yield and decreasing the time and the material needed to accomplish the total needed number of devices. For the small fabrication contemplated in this proposal, the capabilities of industrial domestic (i.e. US based) suppliers will be leveraged for part the process: wafer bonding (Cactus Materials Inc., Tempe, AZ) and, as usual, ion implantation (Innovion), while the rest of the process will be carried out by BNL. If the devices proves successful and it is chosen as sensor of choice for parts of the EIC detector(s), fabrication can be entirely carried on at Cactus Material Inc , or in another US company. Supply of silicon wafers is also not a concern, as both low-resistivity n-type wafers and high-resistivity (n or p-type) are relatively easy to obtain. Clean room supplies are not a concern, if orders are properly and timely dispatched. Furthermore, chemicals commonly used in the fabrication in clean room have a very long shelf life, so they can be ordered well in advance. At the time of writing, BNL is well equipped to start immediately the fabrication.

11. Diversity, Equity and Inclusion

BNL understands the importance and has a strong commitment to work with underrepresented or underserved minorities following DEI guidelines. If the proposal is funded, we will attract students from underrepresented neighborhoods surrounding BNL, and mentor them to work on multiple parts of the projects. We will accept undergraduates for the spring and summer terms, as well as high school students. They will be in the

outstanding position to observe the research work leading to the fabrication of a brand-new device, starting from scratch. Hopefully, it will inspire young researchers from underrepresented minorities to undertake much needed careers in instrumentation, electronic engineer, or STEM at large.

UCSC PI Schumm is the Director of UC Operations for the inter-segmental Cal-Bridge Program (https://www.cpp.edu/calbridge/index.shtml), currently funded at $5M per year by the California Legislature, that mines the diverse talent of the California State University undergraduate student body, bringing competitively-selected students into close mentoring relationships with UC faculty and cultivating them for admission to graduate school. In addition, Postdoctoral Fellow Mazza, who will lead much of the day-to-day work on the proposal, has been a leader in the development of Cal-Bridge's Peer Mentoring program. As a result, SCIPP has access to a significant pool of talented graduate students from historically under-represented backgrounds. Two such students (fourth-year Rene Mora Padilla and second-year Miguel Escobar Godoy) are currently active in the Fast Sensors group that will host the UCSC portion of the proposed work, which would provide significant additional opportunity for their education and professional development.

References

[1] Giacomini et. al.: Development of a technology for the fabrication of Low-Gain Avalanche Diodes at BNL, NIMA 934 (2019) 52, https://doi.org/10.1016/j.nima.2019.04.073

[2] Giacomini et al.: Fabrication and performance of AC-coupled LGADs, 2019 JINST 14 P09004, https://doi.org/10.1088/1748-0221/14/09/P09004

[3] Heller et al. Characterization of BNL and HPK AC-LGAD sensors with a 120 GeV proton beam, https://arxiv.org/abs/2201.07772?context=physics

[3] Ayyoub et al.: A new approach to achieving high granularity for silicon diode detectors with impact ionization gain, https://arxiv.org/abs/2101.00511