Silicon Tracking and Vertexing Consortium EIC Generic Detector R&D Proposal for FY23

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Abstract

Monolithic Active Pixel Sensors (MAPS) offer the possibility of high granularity and low power consumption, making them a prime choice for the charged-particle tracking and vertexing subsystems of the central detector(s) at the future EIC. The performance of the inner tracking system will have a direct impact on several key observables at the EIC, including the precision measurement of the scattered electron in DIS, the reconstruction of heavy-flavour decays and the measurement of the charged constituents of jets. This proposal builds on prior R&D efforts of the EIC silicon consortium for tracking and vertexing and related efforts in support of the recent detector proposals submitted to the Detector Proposal Advisory Panel as well as the selected project detector. Generic R&D effort is proposed in four areas for FY23, namely on embedded MAPS towards large(r) instrumented areas with minimized material, on investigating commercial capabilities towards manufacturing aluminum flexible circuits in the U.S., on developing of a multi-modal modeling environment that will integrate the physical space, signal processing, generation of data flows and data transmission, as well as on conducting functional verification of the EIC MAPS detector complex based on Universal Verification Methodology (UVM), and on exploring the viability of core concepts for a future ultra-fast MAPS. The proposed efforts are independent of and complementary to our ongoing project R&D efforts.

[0]The authors and institutions explicitly named on this page are proponents of this proposal. They are all members of the Silicon Tracking and Vertexing Consortium, which has additional members and member institutions.

The science program at the EIC imposes stringent requirements on the charged-particle tracking and vertexing subsystems [1]. High granularity, low power consumption, and large acceptance are all paramount considerations. Monolithic Active Pixel Sensors (MAPS) are the sensor prime choice for a well-integrated inner tracking and vertexing detector subsystem consisting of barrel layers and disks surrounding the EIC nominal interaction point because of the possibility of high granularity and low power consumption. We propose to pursue generic EIC detector R&D in FY23 in four areas. Section 1 discusses efforts to advance embedded MAPS towards large(r) instrumented areas with minimized material. A specific motivation for this effort is the desire to drive the material in the sagitta layers of the EIC reference detector design to an absolute minimum, proposed as one of two modification options to the reference design towards achieving the momentum resolutions in the EIC Yellow Report [1] at mid-central pseudorapidities. Section 2 discusses potential possibilities of commercial capabilities towards manufacturing aluminum flexible circuits in the U.S., motivated by material minimization and risk considerations, and section 3 development of a multi-modal modeling environment that will integrate the physical space, signal processing, generation of data flows and data transmission, as well as on conducting functional verification of the EIC MAPS detector complex based on Universal Verification Methodology (UVM). Section 4 presents a effort on exploring the viability of core concepts for a novel future ultra-fast MAPS aimed at integrating PID capabilities by time-of-flight measurement. The efforts described in sections 1 and 2 may find use in the EIC project detector, whereas the timeline of the R&D proposed in section 4 and any subsequent development towards a production-ready sensor is more geared towards an upgrade of detector-1 and/or detector-2.

1 Embedded Monolithic Active Pixel Sensor R&D

P.I.: Nicole Apadula (LBNL), Giacomo Contin (Trieste/INFN), Nicolas Schmidt (ORNL)

1.1 Motivation

Silicon tracking detectors are an integral part of collider experiments and their utilization at the EIC is critical to achieve the expected physics program. Multiple layers of tracking sensors are needed in order to reconstruct and constrain the trajectory of charged particles. Such layers are generally arranged in cylindrical configurations at varying radii close to the interaction point or on disks around the beam pipe at varying positions along the beam directions to cover the central or forward regions, respectively. In order to reduce the effects of multiple scattering, which can drastically reduce the track reconstruction performance in an experimental apparatus, the material budget of sensors as well as support and cooling structures of such layers needs to be minimized. With these goals, the size of the sensing element used to equip the tracker layers is evolving from single reticle dice to wafer-size sensors, which embed in the CMOS circuitry the power, data and control signal distribution, allowing for the removal of interconnection and powering busses in most of the detector acceptance. Further developments have expanded such designs to wafer scale sensors that can additionally be bent in cylindrical shape without a significant efficiency loss as currently envisioned for ALICE ITS3 [13, 12].
The MAPS technology demonstrated to have the potential to meet this requirement within the timeline foreseen for the development and construction of the EIC Detector 1. Nevertheless, in the large area flexible stitched sensor which has been chosen to form the EIC Detector ver-

texing layers, the capability to distribute power from the edge connections across the sensor through the CMOS metal stack has yet to be qualified and validated. In addition, depending on the measured fabrication yield, the size of the sensor used to form the outer tracker layers and disks will have to be adjusted to reduce the cost and simplify the construction and quality assurance procedures. Different layouts need to be designed to form building blocks of large area layers, integrating electrical and mechanical connections, in a way that is easy to produce serially, given the wide area to cover (around 10 m^2). Moreover, a versatile way to embed the signal and power distribution in the sensor itself also for the outer tracker would allow for a flexible design, able to meet the production requirements.
As such thin silicon sensors are at risk of being damaged while being handled, mounted, or electrically interconnected. We propose a dedicated R&D project for the mechanical and thermal evaluation of embedded silicon sensors for risk reduction of the EIC project detector 1 silicon tracking layers [2] and future large scale silicon pixel sensor applications. Moreover, we would like to explore joining multiple existing ALPIDE MAPS-sensors [3] within the same embedded setup using thin copper clad polyimide structures as interconnections in junction with a thin copper layer on top of the sandwich structure. These can be added using classical edging techniques or via additive manufacturing.

This R&D builds on top of previous "MAPS foil" [4] developments for the ALICE ITS3 at the CERN Large Hadron Collider (LHC), where kapton-based laminated silicon sensors were initially considered and first lamination tests were performed. The silicon sensors for this R&D are based on ALPIDE MAPS which can be thinned to a thickness of 50μm at which they can be bent into cylindrical shape without significant performance loss. The mechanical properties of such thinned silicon sensors make them prone to shattering under small shear stress without additional supports. This R&D therefore aims to evaluate the mechanical properties of Kapton embedded silicon sensors. While kapton foils transfer heat to a certain degree it has so far not been investigated how well the silicon sensors in this laminated setup can be cooled. Thus we would like to perform a thermal evaluation of such sensors in order to determine the integrated cooling requirements of multi-sensor detector modules. The interconnection of embedded sensors is additionally included in this R&D as a crucial component for large scale application of this technology.

This is of particular importance for the MAPS-based sagitta layers of the silicon tracking system of the EIC Detector 1 or future large scale silicon layers within the second EIC detector system. The sagitta layers of Detector 1 are required to be of cylindrical shape and at radii of $R \approx 20$cm from the interaction point, see Fig. 1 (left). In the reference detector design, a material budget of $0.05\%X/X_0$ was assumed for these layers, which corresponds to pure silicon sensor layers of 45μm thickness without additional support structures or cooling material. Such a design is proven to be viable at small radii ($R < 5$cm) for vertexing layers [5], but has not yet been mechanically and thermally evaluated at larger radii. In addition, the vertexing layers are based on single large wafer-scale sensors per half-cylinder (meaning for 180° in azimuthal coverage). The proposed sagitta layers will require multiple of these sensors (8 or 9) per half-cylinder and thus require further evaluation of their internal support or the need for additional reinforcement. This design based on bend wafers is however only possible if the tiling of the half cylinders can be kept to a minimum. Otherwise, additional mechanical supports might become necessary which might put additional strain on the wafer-scale sensors and thus increase their risk to shatter under the constant air flow required to cool the sensors. Moreover, the cooling requirements of these layers need to be evaluated in order to integrate the optimal and most lightweight cooling solution in terms of material bud-

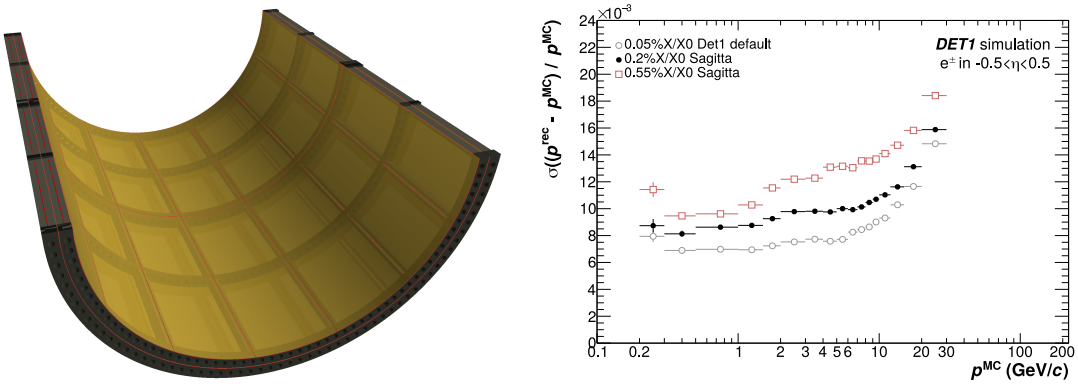

Figure 1: Left: View of the envisioned Detector 1 silicon sagitta layer half-shell. Each wafer-scale sensor is framed by a red line to visualize the sensor layout. Right: Track momentum resolution at mid-rapidity in EIC project Detector 1 with three different configurations for the silicon sagitta layer material budget (0.05%–0.55%X/X_0).

get in Detector 1. More traditional designs for the sagitta layers at the same location based on staves (0.55%X/X_0), on the other hand, lead to a signification deterioration of the detector performance, which would not allow to access the desired physics performance at the EIC, see Fig. 1 (right). More aggressive approaches for the stave designs might allow to reduce the material down to 0.2%X/X_0. Beyond that only the proposed embedding techniques or similar processes could offer a possibility to reduce the material even further. The lamination process might also reduce the need for wafer sized sensors ($\sim 28x9$ cm), which often have a comparatively low yield during the production due to micro defects during the production process. This is possible, as the process might allow to mechanically and electrically connect sensors of smaller sizes to larger superstructures with similar mechanical properties.

1.2 Proposed R&D

The R&D plan will first focus on single sensor size lamination similar to the process outlined in Fig. 2. The lamination process will be evaluated for ease of application and possible large scale applications. Both working and non-working sensors will be laminated for further study. The working sensors will be interconnected via through-hole copper plating and then be further evaluated. Mechanical and thermal tests will be conducted on non-working sensors. In particular, not much is known about how these sensors will behave thermally once they are laminated, so careful consideration will need to be taken on their cooling requirements. Both liquid and air cooling will be studied.

After evaluation of single sensor lamination, larger size structures will be laminated. The Detector 1 vertex layers will be wafer-scale size, but the sagitta and disc layers will need to be built out of multiple single or stitched sensors. This introduces multiple joints where the sensors need to be placed close to one another, thus leading to extra mechanical stress that will need to be tested.

Air cooling is currently being studied as a means to cool the outer barrels and discs for Detector 1. Project R&D eRD111 aims to see if air cooling is feasible for those larger surface area structures using carbon foam and carbon fiber. The laminated sensor does not have a

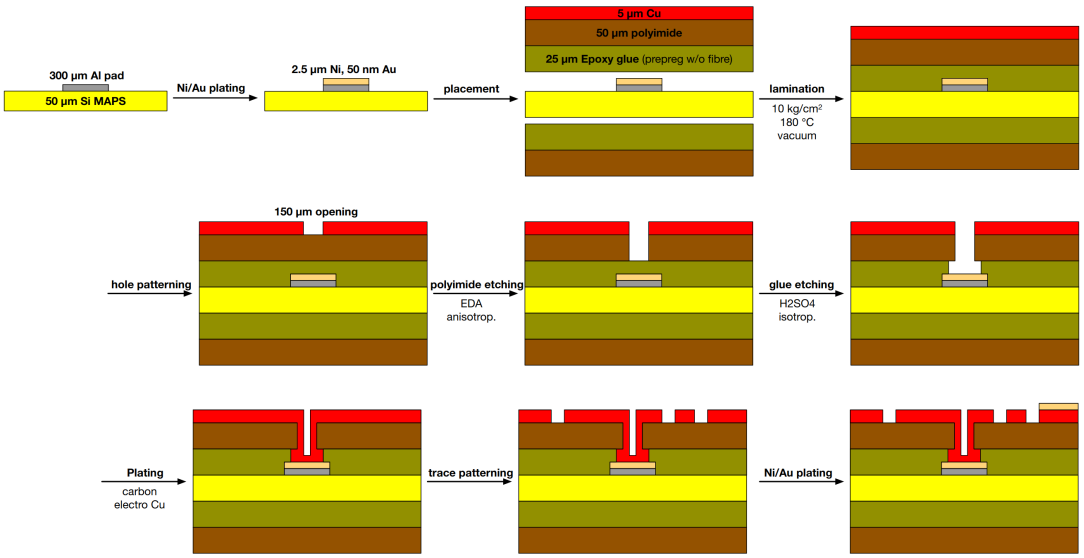

Figure 2: Kapton foil lamination process developed in Ref. [4] for thinned MAPS sensors. The process includes a through-hole copper plating for interconnection of sensors and copper structures for electrical traces.

porous structure like carbon foam and the thermal properties will need to be examined with and without cooling. Close attention will need to be paid to how the material deforms under air flow. Liquid cooling options will also be studied, including how to construct the cooling circuit on the laminated sensor.

As mentioned, the vertex layers will be constructed of wafer-scale size sensors bent around the beam pipe. The possibility of creating such structures that are mechanically held by the kapton lamination could potentially eliminate some of the deformation expected from the current plan of carbon foam wedges or longerons. It also has implications for creating larger cylinders out of these curved sensors, rather than planar staves that are formed into a cylinder as is the current standard. For FY23, the R&D would focus on a first try at making a curved sensor that can hold its shape with the kapton lamination. As part of this R&D project we would also like to explore alternative materials for the embedding which offer different mechanical and thermal properties, whilst still maintaining the functionality of the sensors themselves.

In addition to the mechanical and thermal tests on the laminated sensors, we propose to explore additive manufacturing (AM) technologies like Ink-Jet Printing (IJP) and Aerosol Jet Printing (AJP) for the embedding of a redistribution layer on large-area thin silicon sensors for the propagation of power and signal lines and test its performance in the specific conditions the ITS3 65nm CMOS sensor is expected to operate. AM techniques like AJP can perform digital printing and dense integration of functional electronics on diverse substrates and with a large variety of materials, with high resolution capabilities, a minimum trace width of 10 µm, and the possibility to deposit a stack of layers to reach the desired trace thickness, all carried out at room temperature.

We also propose to extend the study of the performance of such a process when applied

to flexible silicon in curved geometry, in order to overcome possible weaknesses in the power distribution network embedded in the 65 nm CMOS large area sensors used to build cylindrical vertexing layers. The mechanical and electrical effects of bending will be measured.

1.2.1 Milestones & Deliverables

We anticipate giving twice yearly progress reports on the status of the R&D. More specific deliverables for each section can be found below.

Embedding small ALPIDE sized silicon mock ups
The FY23 deliverables for the embedding of small ALPIDE sized silicon mock ups will include:

- Production of test pieces to be used in mechanical, cooling, and interconnection tests.
- Written report in conjunction with the large area mock ups.

Embedding large scale silicon mock ups
The FY23 deliverables for the embedding of large scale silicon mock ups will include:

- Production of large scale (stave size) test pieces to be used in mechanical, cooling, and interconnection tests.
- Written report in conjunction with the single sensor mock ups.

Mechanical and thermal properties of laminated sensors
The FY23 deliverables for the mechanical and thermal properties of laminated silicon will include:

- Written report detailing the mechanical and thermal properties of the laminated sensor.

Additive manufacturing of power and data redistribution layers on thin large-area silicon
The FY23 deliverables for the interconnection of laminated sensors will include:

- Written report detailing the electrical properties of the different additive manufacturing technologies.

1.2.2 Funding request

The funding request for the proposed embedded MAPS R&D effort in FY23 is shown in Tab. 1 for all participating institutions. The money requested for INFN will fund half of a postdoc who will be stationed at INFN and supervised by Giacomo Contin working on the additive manufacturing of power and data portion of this activity.

2 Aluminum Flexible Circuit Manufacturing Capability

P.I.: Yuan Mei (LBNL)

Table 1: Funding request and breakdown for each institute according to different categories for the proposed embedded MAPS R&D effort in FY23.

institute	**cost in k$**					**total in k$**
	mech. engineer	**technician**	**postdoc**	**material**	**travel**	
LBNL	32.4	57.6		5.0	2.5	97.5
ORNL	41.4	60.8		17.5	2.5	122.2
INFN			34.0	15.0		49.0
UTK						(in kind)
UCB						(in kind)
	73.8	118.4	34.0	37.5	5.0	**268.7**

Table 2: Funding request and breakdown for investigating aluminum conductor manufacturing capabilities in FY23.

institute	**cost in k$**		**total in k$**
	material	**travel**	
LBNL	12.5	2.5	15.0
Total			**15.0**

While stitching is a particular attraction of the proposed ALICE-ITS3 derived MAPS sensors for the EIC, thereby integrating part of the conductors into the sensor itself, external flexible circuits are essential components of an EIC MAPS-based tracking and vertexing subsystem. Care needs to be taken to minimize material in these flex cables, since they can otherwise become significant contributors to the overall traversed material. In the case of the STAR MAPS-based HFT PiXeL detector, for example, a double-sided design in aluminum conductor technology with 30 μm thick aluminum conductor on both sides and a 50 μm thick Kapton dielectric was used. This contributed 0.128% to X/X_0 for each detection layer, or about a third of the overall material budget. Use of industry-standard copper technology would have doubled this contribution. Micro-conductors in aluminum technology have been produced in the CERN PCB shops and at the SRTIIM institute in Kharkov. Prototypes have been obtained from Hughes Circuits Inc. in the US in the past as part of development for ALICE-ITS2 and promising, relevant, new commercial capability appears to have come in existence motivated in parts by applications in Quantum Computing.

We request seed funds in the amount of 15k$ in FY23 in material and possibly travel to be able to further investigate the possibilities of commercial manufacturing of aluminum flexible circuits in the U.S. in view of their importance in minimizing material in the sensitive detector areas at the EIC. If this turns out successful, we anticipate a follow-up through SBIR to ramp up the U.S. manufacturing of aluminum flexible PCB. The funds are requested at LBNL. The funding request for this effort is summarized in Tab. 2.

3 Functional Verification Model of EIC Tracking and Vertexing Detectors R&D

P.I.: Grzegorz Deptuch (BNL)

3.1 Motivation

The proposal in this part focuses on investigating the possibility of building a multi-modal modeling environment that will integrate the physical space, signal processing, generation of data flows and data transmission, as well as on conducting functional verification of the EIC MAPS detector complex based on Universal Verification Methodology (UVM). Universal Verification Methodology is defined in terms of developing system through architecting test-benches and test cases, and also comes with a library of classes that helps in building efficiently constrained random test-benches in a convenient way as part of the paradigm of the SystemVerilog framework. The modeling of the entire detector, which may have several versions, will allow for its specific, virtual operation, giving the possibility of testing in conjunction with continuous stimulation from EIC event generators. It should also be seen as R&D towards risk reduction and optimization of the detector structure.

3.2 Proposed Verification R&D

We propose a dedicated R&D project aiming at developing a model of the full scale EIC tracking and vertexing detector complex to allow as complete as possible understanding of the operation of the detector planes and carrying out the necessary optimization. This R&D builds on top of the ALICE ITS3 [13, 12] Monolithic Active Sensors (MAPS) developments at the Large Hadron Collider (LHC) in which the EIC Silicon Consortium is actively involved. These advanced design of MAPS that are planned to be stitched on the reticle and bent into cylindrical shapes for decreasing to the achievable minimum material budget for these layers to $0.05\%X/X_0$ are expected to be directly or with some modifications used for construction of the tracking and vertexing planes at the EIC.

Our R&D proposal targets investigation of how to approach development of a formalized description grasping functionality of the structures, including generation of charge signals, their processing through the front-end circuitry then going up to the data flow problem, congregation of the data links and transmission off the detector that would be coupled with the physical properties of the detector, modeled purely on the electrical level, for analyzing impacts on the localized electrical properties of the sensors as well as handling of data flow without entering into overruns. One of the big concerns in Large Area Sensors are static, and, more importantly, dynamic IR (voltage drops due to the resistive nature of power supply lines conveying supply currents) power supply voltage drops that are dangerous for the high fidelity operation of the front-end circuitry of the finely segmented pixels.

The scale and depth of the hierarchy of the sensors excludes any spice-like modeling. Also performing all the verification tasks requires an agreed framework within which reusable verification components can be created and test environments, utilizing constrained random stimulus generation and functional coverage methodologies, can be assembled. Therefore we propose building a model of the full scale EIC tracking and vertexing detector complex using SystemVerilog and the Universal Verification Methodology (UVM). The latter is a commonly

used framework of SystemVerilog classes for reflecting the architecture of whole detector system and building functional test benches. It is characterized by:

- modularity (modular components: Driver, Sequencer, Agents, Env, etc.) and reusability (horizontal and vertical).
- separation of tests from testbenches.
- sequence methodology, and
- possession of configuration mechanisms.

SystemVerilog is a language just like Verilog and has its own constructs, syntax and features that is commonly used in the digital part for writing synthesis-ready Register Transfer Level or behavioral code for designing complex mixed-mode integrated circuits as well as providing a convenient way of describing complex system arrangements composed of multiple ASICs, commercial chips and FPGAs. UVM is infinitely popular in industrial applications. In the field of nuclear electronics, or in general in the development of detector systems in particle or nuclear physics experiments, the UVM has been used successfully in the development of single integrated circuits, e.g. by RD53 collaborations [10, 11]. The introduction of the UVM formalism coupled with the physical level for modeling and verifying the entire detector, which is postulated, is a new approach and the scale of application in the experiment such as the EIc detector requires knowledge of ASIC design, detector system integration and the physics.

3.3 Impact of the proposed R&D on other areas of development of MAPS for EIC

We believe that through realization of this proposal, we will be able to open or facilitate other research activities such as:

- development of efficient powering schemes of LAS to handle IR drops, including investigation of serial powering.
- introduction low-swing and low-power data transmission links for carrying our data on long distances within individual LAS to the edges and study possible levels of resource reduction.
- development of dual port, area-efficient Static Random Access Memory (SRAM) and their embeddement in the full detector structure.
- study and optimizing data flow to address efficient of serving zones with increased rates, etc.

Modelling and verification is a vital need for any large scale electronic system. It has been proven that being able to cover not only a structure of the complex system in a formalized description, but also its operation, using either generated, random data or physics based input, leads to the optimization and elimination of issues that can be overlooked otherwise. In scientific environments, this verification has not been explored to the same extend as in the industry. The scope of the EIC MAPS detector system is unprecedented, strongly justifying reaching for formalized verification methodology.

3.4 Resource request and schedule

In FY23, we request about three months of a combined efforts of an ASIC design researcher and physicist at BNL to perform the ground setting analyses of the modeling and verification using the standardized SystemVerilog and UVM framework. The funds allocated for travel are intended for travelling to CERN to establish an efficient platform for exchanging databases and establishing common practice for building modeling and verification constructs.

In the case of a 20% funding reduction, this would not allow for investigating the full scope of how to adapt the industry standard methodology to a scientific instrument that, effectively, has not been designed conforming to the verification methodology from the start point. A 40% funding reduction would allow only for minimum level investigations, such as reviewing interfaces existing in the system and what can be critical.

Table 3: Funding request and breakdown for Functional Verification Model of EIC Tracking and Vertexing Detectors R&D effort in FY23.

institute	**cost in k$**		**total in k$**
	ASIC research staff	**travel**	
BNL	100.0	8.0	108.0
Total			**108.0**

4 Ultra-fast Timing Monolithic Active Pixel Sensors

P.I.: Yuan Mei (LBNL)

4.1 Motivation

The tracking requirements to accomplish the EIC science program, worked out in the EIC Yellow Report [1], make Monolithic Active Pixel Sensors a natural choice for the inner tracking and vertexing system of the general-purpose central collider detector(s) because of the possibility of higher granularity, low power consumption, and hence lower material compared to other technologies. Indeed, all three detector proposals submitted to the Detector Proposal Advisory Panel past December 2021 have settled on ALICE-ITS3 derived MAPS-based subsystems for vertexing and inner tracking for these reasons. A limitation of the current generation(s) of MAPS sensors is their relatively long integration windows, projected to be of$\mathcal{O}(2\,\mu\text{s})$ for the EIC. This precludes their use in time-of-flight based particle-identification at the EIC based on studies that have been made by us and within the broader EIC community. It will also limit use cases including time-based rejection of backgrounds and 4D tracking [7], which are both areas where simulations are still under development for the EIC. The time-of-flight systems proposed for the EIC detectors thus far rely on AC-LGAD technology with a projected resolution of $\mathcal{O}(25\,\text{ps})$. However, the material budget associated with AC-LGAD technology precludes their placement near the interaction vertex even when their timing resolution would otherwise be sufficient for low-momentum particle-identification needs because of the challenges to meet the tracking resolution requirements. The EIC reference design, for example,

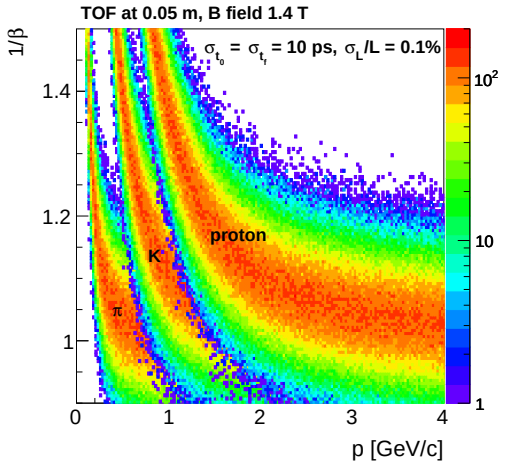

Figure 3: Simulated separation power of pions, Kaons, and protons represented as the inverse of the relativistic fraction β for a time resolution of 10 ps and flight-path reconstructed with 0.1% relative precision over a radial distance of 5 cm. Pion-Kaon separation at the three standard-deviation level is achieved for momenta p below 0.7 GeV, while Kaon-proton separation is achieved below 1.2 GeV in this simulation.

has an AC-LGAD barrel layer at a radius of $\mathcal{O}(65\,\mathrm{cm})$ outside of the volume enclosed by the MAPS-based subsystem.

This proposal aims to investigate the viability of a concept towards a Monolithic Active Pixel Sensor that could achieve $\mathcal{O}(25\,\mathrm{ps})$ timing resolution or better, while preserving the advantages of high granularity and low power consumption. If the concept proves successful and, subsequently, a longer-term development path is undertaken, such a sensor would have a natural application as an upgrade (or staging) path for detector-1 or detector-2. Specifically, it would complement particle identification capabilities for low momenta, below the DIRC firing treshold, could serve as a compact start-time system for other time-of-flight based subsystems, and should be anticipated to aid in background rejection and 4D tracking.

To illustrate the above, we have performed simulations of particle identification by time-of-flight for a pertinent range of parameters. Figure 3 shows the simulated separation for mid-rapidity pions, Kaons, and protons as the inverse of the relativistic ratio β versus momentum, p, for a time resolution of 10 ps and flight-path reconstructed with 0.1% relative precision. The 1.4 T strength is characteristic of EIC detector-1 solenoidal magnetic field and the 5 cm radius is characteristic of the inner MAPS vertexing subsystem. Pion-Kaon separation at the three standard-deviation level is achieved for momenta p below 0.7 GeV, while Kaon-proton separation is achieved below 1.2 GeV in this simulation.

In figure 4, We show the momentum coverage of 3 standard-deviation separation between pions and kaons by implementing a time-of-flight system with various intrinsic timing resolutions (left) at different radial location and the impact of reconstructed path length uncertainties (right), in comparison with the Kaon threshold of the DIRC barrel PID subsystem of the EIC detector-1 reference. Time-of-flight capability within the envelope of the MAPS-based inner vertexing subsystem and its sagitta layers, a volume with a radius of $\mathcal{O}(25\,\mathrm{cm})$, is clearly seen

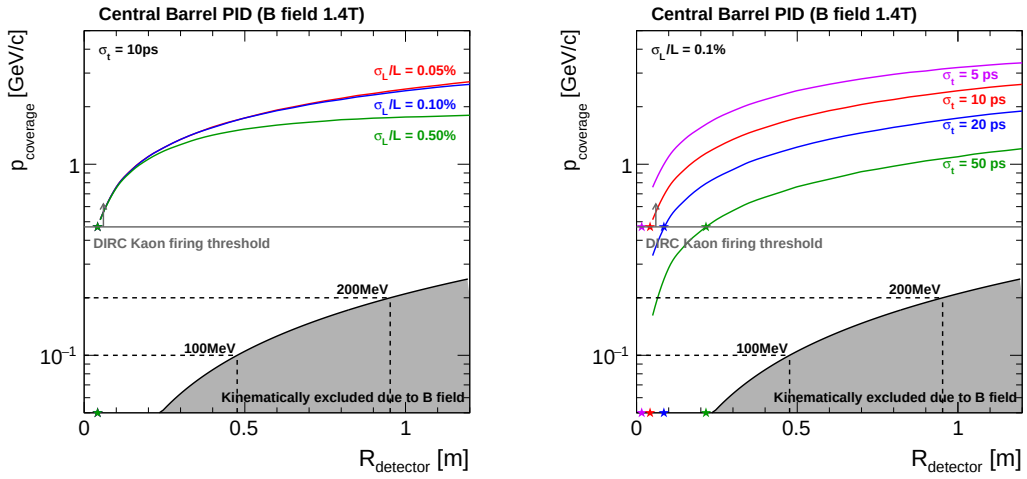

Figure 4: Simulated Kaon momentum reach using the time-of-flight technique for a range of time resolutions (left) and reconstructed path lengths (right) versus the radial detection lever arm. The DIRC firing threshold for Kaons in the EIC detector-1 reference is shown for comparison.

to complement particle identification with the DIRC subsystem for low momentum values.

An ultra-fast Monolithic Active Pixel Sensor that could achieve $\mathcal{O}(25\,\mathrm{ps})$ timing resolution or better, while preserving the advantages of high granularity and low power consumption, is thus well motivated by additional particle identification capabilities it would provide even in the 1.4 T field of the EIC detector-1 reference. A higher field value, which has been considered for the alternative EIC detector proposals, further strengthens these arguments. In addition, it should be anticipated to aid in background rejection and 4D tracking at the EIC and will have broader applications. The full development of a production-ready sensor will be a major, long-term effort. This proposal aims to enable initial R&D that will serve as a timely verification of its core concepts, discussed below.

4.2 Concept and proposed R&D

We propose to explore the possibility of a novel in-CMOS Avalanche Diode (AD) – Transmission Line (TL) – Time-to-Digital Converter (TDC) scheme that could simultaneously achieve $\mathcal{O}(10\,\mu\mathrm{m})$ spatial and $\mathcal{O}(10\,\mathrm{ps})$ timing resolution while retaining all other advantageous characteristics of the current generation MAPS sensors.

MAPS is the technology of choice for the EIC tracking and vertexing subsystem and has a wide range of other applications. The technology combines the signal generating material and the readout electronic circuits in one monolithic piece of silicon and relies on industrial standard CMOS mass-production processes. Figure 5(a) shows the cross-section view of a typical MAPS sensor. To achieve sufficiently low noise, small electrodes (and thus small capacitances) are used to collect the thermally drifted electrons before entering a front-end charge sensitive amplifier. This necessitates that the electrodes be sparsely distributed, often $20-50\,\mu$m apart. Due to this distance, when the center of the charge cloud changes location from event to event,

the time it takes for the closest electrode to see charge varies significantly. The typical variance in timing due to this is about 25 ps, posing a fundamental limit on typical MAPS timing resolution. Moreover, because of power constraints, the amplified analog output pulses are slow and further limit timing applications.

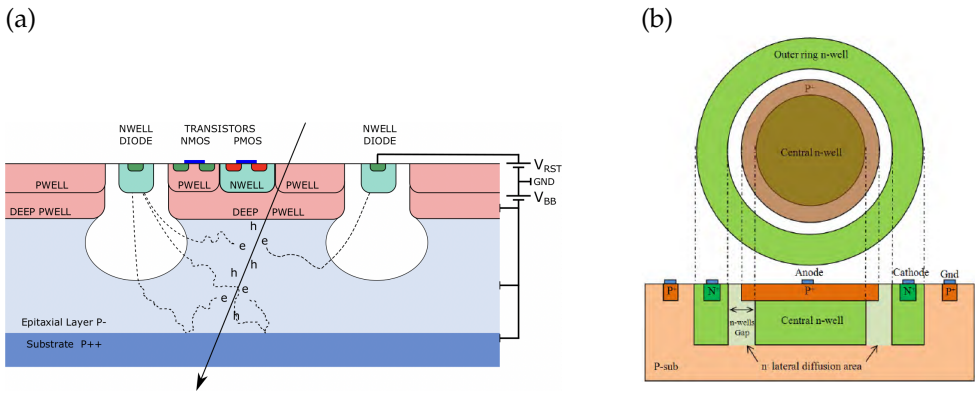

Figure 5: (a) Cross-section view of a typical MAPS sensor. (b) A representative Avalanche Diode structure implemented in CMOS.

An alternative for front-end charge detection is an avalanche diode (AD), another structure that has widely been implemented in CMOS technology, most commonly as single-photon avalanche diode (SPAD) [8]. The structure of a typical SPAD is shown in Fig. 5(b). SPADs can respond to the incident photon or collected charge by undergoing an avalanche, which results in a fast pulse. Single-photon sensitivity is unnecessary in charged particle detection, which makes it possible to lower the gain and hence drastically reduces dark counts. ADs are much smaller in size, $\mathcal{O}(1\,\mu\text{m})$, and do not consume power when there is no signal. These features make it possible to consider implementing a dense array of ADs to capture charge.

The AD in the array that first fires after a charged particle traverses the silicon will determine the leading edge of the generated pulse. The $\mathcal{O}(25\,\text{ps})$ timing variation of typical MAPS sensors is mitigated by the much finer AD pitch of $\mathcal{O}(1\,\mu\text{m})$ in the array and the leading edge of the pulse is sufficiently fast because of the avalanche process. While ADs, specifically SPADs, implemented in CMOS are in principle a mature technology, the mode of their usage in the proposed architecture is new. We thus propose to study their properties and search for optimal design parameters by simulation and prototype testing.

When pulses leave the pixel in the proposed architecture, they propagate in both directions along a transmission line that is read out from both ends with TDCs. The proposed sensor architecture is shown schematically in Fig. 6(a). The pixels are arranged in a regular 2D array. The outputs of the pixels in two adjacent columns drive two common transmission lines. The transmission lines are U-shaped so that their readout with TDCs can be organized in the periphery of the sensor where area and power requirements are less stringent, thereby facilitating high-performance design. Upon particle impact, the hit pixel emits a pulse onto the TL. The pulse travels in both downward and upward directions on the TL. The TDCs attached at both ends of the TL register the arrival times of the two pulses, t_1 and t_2. The location of the hit pixel, y, and the arrival time of the hit, t_o, can be calculated as $y = h - u(t_2 - t_1)/2$ and $t_0 = (t_1 + t_2)/2 - h/u$, respectively, where h is the height of the column and u is the propagation speed of the TL.

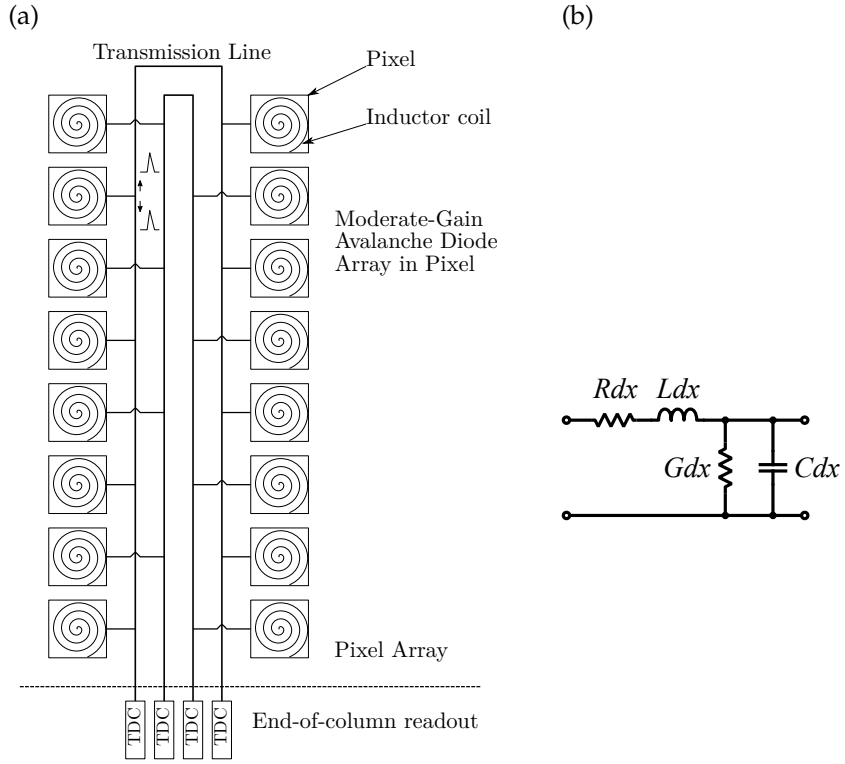

Figure 6: Sensor structure. (a) Pixel array structure with transmission line and TDC readout. (b) Transmission line model with distributed lumped components.

The TL must have appropriate propagation speed, low dispersion, acceptable loss, and matching impedance to the ADs and the TDCs. We propose to implement an entirely passive transmission line using metals in the CMOS chip. Such a transmission line can be seen as a chain of distributed inductors, capacitors, and resistors and modeled by the telegrapher's equations (c.f. Fig. 6(b)). The characteristic impedance is $Z_0 = \sqrt{\frac{L}{C}}$ and the wave propagation speed $u = \frac{1}{\sqrt{LC}}$, where L, C, and R are defined per unit length. For adjacent pixels to be distinguishable by measurement of the arrival time difference, the propagation speed u must be slowed down to below 10^{-2} times the speed of light. A way to achieve this is to enlarge L by designing metal-layer coils in each pixel, as depicted in Fig. 6(a). We anticipate that implementing a transmission line that satisfies all criteria will be a major challenge. We request resources to support design and simulation effort as well as manufacturing prototypes to validate the design.

High-performance TDC designs that achieve $< 5\,\text{ps}$ resolution have been demonstrated years ago [9] and improved on continuously. Unlike most of the existing use cases of TDCs, where signals are coupled to the TDCs via bonding wires and pads which carry large parasitic inductance and capacitance as well as imperfections in impedance matching, the signals are directly coupled to the TDC input from the TL in the proposed sensor architecture, ensuring best matching and low noise/interference. While engineering a high-performance TDC is challenging, we consider it a well-constrained and tractable engineering task. We will leverage

excellent existing designs and focus the effort on coupling and system level integration.

4.3 Resource request and schedule

In FY23, we request 3 months of an IC design engineer's time at LBNL to perform designs of critical components and assemble test chips for manufacturing submission. Two silicon chip manufacturing submissions (tapeouts) are planned. With SPAD capabilities in CMOS, each tapeout in MPW (multi-project wafer) will cost about 40k$ based on prior experience. The two tapeouts are planned 6 months apart, to allow time for manufacturing (3 months) and characterization (3 months) in each run. Existing equipment at LBNL will fully cover the measurement needs of the chips.

The two silicon chips will test various designs of SPADs and quantify their performance under the proposed scheme. Various transmission line designs will be produced and tested as well. We anticipate that there will be insufficient time to demonstrate full TL-TDC coupling but smaller test structures that help characterizing impedance matching, loss measurement, etc. will be included.

Table 4: Funding request and breakdown for fast MAPS R&D effort in FY23.

institute	**cost in k$**			**Total in k$**
	IC design engineer	**material**	**travel**	
LBNL	(3 months) 100.0	80.0	2.5	182.5
Total				**182.5**

In the case of a -20% funding reduction, the IC designer time will be reduced to allow the total funding to be within such an adjustment, which will result in the reduction of designed and tested components. In the case of a -40% funding reduction, the tapeouts will be reduced from 2 to 1 and the IC designer time will be reduced as well to reflect the change. It will further reduce the scope of the design and testing.

Last, we note that an active interest in contributing to this area of R&D is shared with proponents at BNL and ORNL, even though funding is requested solely at LBNL.

5 Money Matrix and Budget Scenarios

Our total funding request for the proposed generic R&D effort in FY23 in an optimal scenario is shown in Tab. 5. Table 6 shows the breakdown of totals per activity for each instituion. We refer to the preceding sections for further specifics and details about each of the four proposed R&D activites.

In a sub-optimal scenario constrained by a 20% reduction from our total funding request (breakdown shown in Table 7), the reductions are as follows:

- Forego the section 2 activity on conductors,
- Forego the alternative embedding techniques portion of the section 1 activity on embedded MAPS,
- Reduction of fast MAPS as detailed in section 4,

Table 5: Total funding request and breakdown by institution.

institute	cost in FY23 k$ eng. and tech.	postdoc	material	travel	total cost in FY23 k$
BNL	100.0			8.0	108.0
INFN		34.0	15.0		49.0
LBNL	190.0		97.5	7.5	295.0
ORNL	102.2		17.5	2.5	122.2
Total	392.2	34.0	130.0	18.0	**574.2**

Table 6: Total funding request by institution for each R&D activity.

institute	Section 1	Section 2	Section 3	Section 4	total in FY23 k$
BNL			108		108
INFN	49				49
LBNL	97.5	15		182.5	295
ORNL	122.2				122.2
Total	268.7	15	108	182.5	**574.2**

- Reduction of modeling and functional verification efforts as outlined in section 3.

Table 7: Total funding request by institution in the sub-optimal, 20% reduction scenario.

institute	Section 1	Section 2	Section 3	Section 4	total in FY23 k$
BNL			84.8		84.8
INFN	49				49
LBNL	97.5			150	231.5
ORNL	97.2				97.2
Total	227.7		84.8	150	**462.5**

In a minimal scenario constrained by a 40% reduction from our total funding request (breakdown shown in Table 8), the reductions are as follows:

- Forego the section 2 activity on conductors,
- Forego the alternative embedding techniques portion of the section 1 activity on embedded MAPS,
- Reduction of fast MAPS as detailed in section 4,
- Reduction of modeling and functional verification efforts as outlined in section 3

6 Diversity, Equity, and Inclusion

The proponents of this proposal recognize the importance of a diverse, inclusive environment that offers equitable opportunities for everyone. All participating institutes operate extensive

Table 8: Total funding request by institution in the minimal, 40% reduction scenario.

institute	Section 1	Section 2	Section 3	Section 4	total in FY23 k$
BNL			65.6		65.6
INFN	49				49
LBNL	75.1			80	155.1
ORNL	72.2				72.2
Total	196.3		65.6	80	**341.9**

DEI programs to further the goal of a diversified academic workplace. The proposed research will advance diversity, equity, and inclusion initiatives of the proposing institutions. Several of the lead-proponents of the proposed R&D are female early-career scientists. They are role models with a track record of attracting and engaging female students in nuclear physics and instrumentation, thereby increasing female representation and narrowing the gender-gap in instrumentation-related experiences in a differentiating development stage.

7 Summary and Outlook

In summary, we propose to pursue generic detector R&D in four areas in FY23, namely on kapton-embedded MAPS, on potential manufacturing of aluminum flexible circuits in industry, on developing a multi-modal modeling environment integrating space, signal processing, data generation and transmission and verification, and on the viability of two core concepts towards a future ultra-fast MAPS. If kapton-embedded MAPS prove a viable option in time and are adopted as part of the detector-1 baseline, the outlook for continued R&D needs in this area will be pursued through project R&D. We envision a follow-up via SBIR to ramp up the U.S. manufacturing of aluminum flexible PCB if our initial exploration in this proposal is funded and turns out successful. Making a start now on the proposed development of modeling and functional verification using industry standard UVM procedures is topical for the EIC, since efforts so far have been limited mostly to single sensors within the community; an initial investment now will inform future steps that may significantly reduce technical risk for the large scale MAPS-based tracking and vertexing subsystem. If the two core concepts towards a future ultra-fast MAPS aimed at a detector-1 upgrade or detector-2 are shown to be viable, we anticipate to make one or more generic R&D follow-up requests in the future.

References

[1] R. Abdul Khalek, A. Accardi, J. Adam, D. Adamiak, W. Akers, M. Albaladejo, A. Albataineh, M. G. Alexeev, F. Ameli and P. Antonioli, *et al.* [arXiv:2103.05419 [physics.ins-det]].

[2] ECCE Collaboration, "EIC Comprehensive Chromodynamics Experiment Collaboration Detector Proposal," https://www.ecce-eic.org

[3] M. Šuljić [ALICE], "ALPIDE: the Monolithic Active Pixel Sensor for the ALICE ITS upgrade," JINST **11**, no.11, C11025 (2016) doi:10.1088/1748-0221/11/11/C11025

[4] S. Beolé, F. Carnesecchi, G. Contin, R. de Oliveira, A. di Mauro, S. Ferry, H. Hillemanns, A. Junique, A. Kluge and L. Lautner, *et al.* "The MAPS foil," [arXiv:2205.12669 [physics.ins-det]].

[5] B. Abelev *et al.* [ALICE], "Technical Design Report for the Upgrade of the ALICE Inner Tracking System," J. Phys. G **41**, 087002 (2014) doi:10.1088/0954-3899/41/8/087002

[6] G. Contin, L. Greiner, J. Schambach, M. Szelezniak, E. Anderssen, J. Bell, M. Cepeda, T. Johnson, H. Qiu and H. G. Ritter, *et al.* Nucl. Instrum. Meth. A **907**, 60-80 (2018) doi:10.1016/j.nima.2018.03.003 [arXiv:1710.02176 [physics.ins-det]].

[7] H. F. W. Sadrozinski, A. Seiden and N. Cartiglia, Rept. Prog. Phys. **81**, no.2, 026101 (2018) doi:10.1088/1361-6633/aa94d3 [arXiv:1704.08666 [physics.ins-det]].

[8] E. Charbon, *et al.*, in: F. Remondino and D. Stoppa (eds) TOF Range-Imaging Cameras. Springer, Berlin, Heidelberg. https://doi.org/10.1007/978-3-642-27523-4_2

[9] L. Vercesi and A. Liscidini and R. Castello, "Time to digital converter based on a 2-dimensions Vernier architecture," 2009 IEEE Custom Integrated Circuits Conference, 2009, pp. 45-48, doi: 10.1109/CICC.2009.5280922.

[10] S. Marconi, E. Conti, P. Placidi, J. Christiansen and T. Hemperek, "The RD53 collaboration's SystemVerilog-UVM simulation framework and its general applicability to design of advanced pixel readout chips", IOP Publishing, Journal of Instrumentation, Oct 2014, Vol 9, Nr. 10, pp 1005, 10.1088/1748-0221/9/10/p10005

[11] C. Gonzalez Renteria, "RD53 Status and the Role of Verification in Digital Design", 2019, https://agenda.hep.wisc.edu/event/1391/contributions/6956/attachments/1688/1901/cpad2019_cgr.pdfe (2022-07-20)

[12] ALICE Collaboration, "Letter of intent for ALICE 3: A next generation heavy-ion experiment at the LHC", Geneva, Mar 2022, "CERN-LHCC-2022-009, LHCC-I-038", https://cds.cern.ch/record/2803563

[13] ALICE Collaboration, "Expression of Interest for an ALICE ITS Upgrade in LS3", Oct 2018, https://cds.cern.ch/record/2644611