A new radiation tolerant low power Phase-Locked Loop IP block in a 65 nm technology for precision clocking in the
EIC frontend electronics

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Abstract: Nowadays frontend electronics of modern particle physics experiments require very precise clock signals for different elements in the readout chain. Clock distribution systems, analog and time to digital converters, gigabit serial links are examples of the components that require clock signals with very low jitter. The proposed project aims to develop a new radiation tolerant Phase-Locked Loop (PLL) IP block for clock signal generation with a jitter lower than ten ps, or even better with the addition of a digital path in the PLL control. This block will be developed in the modern TSMC 65 nm technology, to allow its integration in future readout ASICs that are considered for the EIC project, and in particular in the SALSA MPGD readout chip that our groups are presently developing. The PLL can also be a basis of a low-power standalone clock fan-out ASIC with phase adjustment capabilities, which might be needed for specific EIC frontend applications. The project will cover the simulation and design of the IP block, as well as its prototyping and validation.

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1. Motivations

The proposed project aims to provide the EIC community, working on the detector readout, with a radiation hardened Phased Locked Loop (PLL) IP block designed in a modern 65 nm technology. We ambition to produce a compact low-power design with a wideband range of its input reference clock and fast locking features yet achieving the low jitter of the synthesized clocks required for the precision timing applications. The PLL IP block could be integrated within the readout ASICs or be used as a standalone clock fan-out component, without any noticeable power consumption impact on the EIC detectors frontend electronics.

A PLL component is an essential element to achieve the high quality clock signals needed for precision timing and amplitude measurements and for reliable Gbit/s serial communications. It is also vital to derive within the frontend electronics all the auxiliary clocks, with frequencies multiple of the distributed system clock frequency, needed, for example, in embedded digital signal processing. The PLL block allows to adjust and to maintain a desired phase relationship between the frontend clocks used for measurements and the central system clock. Thus not only the frontend leaves of sub-detectors are kept synchronous, but also the sampling instance can be finely tuned to achieve the best possible precision.

Jitter cleaning capability of the PLL component is yet another crucial feature for accurate measurements. Clock quality may suffer over the distribution path from the central DAQ to an individual frontend board. A poor quality clock affects the effective number of bits (ENOB) of the analog to digital converters (ADC) resulting in a lower signal to noise ratio (SNR). Similarly, clock uncertainty adds in a quadratic way to other inaccuracies of time to digital converters (TDC) degrading timing precision. The frontend PLLs, being the very last elements within the clock distribution chain, allow restoring its quality in order to achieve the desired measurement precision.

A typical deployment of the PLL IP block within a detector readout ASIC is shown in Figure 1. Its frequency synthesis capability is exemplified by generation of a set of three clocks at 50, 200 and 500 MHz used respectively in analog, digital and high-speed link domains. In this particular case, the input clock distributed within the system is 100 MHz (to mimic the EIC bunch-crossing rate) but could be higher or lower. The 50 MHz ADC clock can be phase-adjusted to sample the signals issued from collisions near to their peak values.
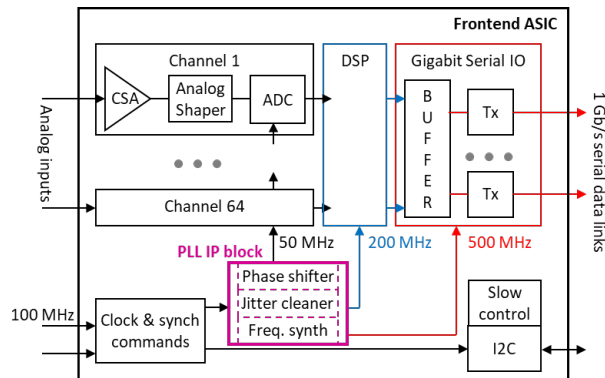

Figure 1: PLL IP block within a frontend ASIC

Note that the I2C slow control communication does not require a PLL-generated clock. It uses either the input clock as is or its slower version derived by simple division. As the relatively slow I2C

communication does not need a high quality clock, this approach allows configuration of the PLL at startup and its monitoring during the operation.

The PLL IP block can be as well the base for a radiation hardened fan-out ASIC used for precision clock distribution within the fronted boards, as shown in Figure 2. Depending on the EIC sub-detector type, the system clock can be distributed to frontends either embedded in a serial data stream (DAQ-frontend downstream link) or via a dedicated precision clock distribution path (especially for ToF sub-detectors with targeted timing measurement precision of ~30 ps).
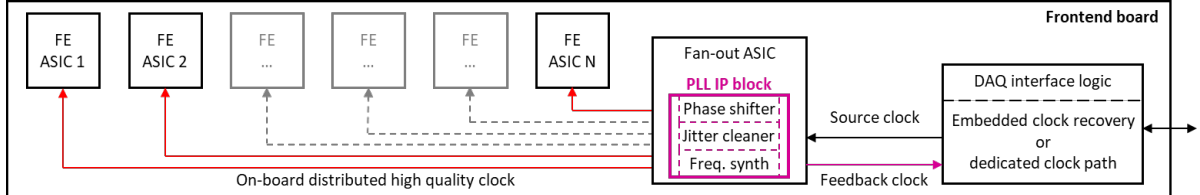

Figure 2: PLL IP block within a fan-out ASIC for on-board precision clock distribution

In the embedded clock distribution case, the clock-data recovery (CDR) circuitry may not be able to guarantee the required quality of the extracted clock. This is especially true if the DAQ interface logic will be implemented on a (low-power) FPGA device. An external jitter cleaner ASIC will be required to improve the clock quality and to distribute N phase-adjusted copies of it to the frontend ASICs.

In the case of dedicated precision clock path, only a single copy of the system clock will be delivered to frontend boards. Most probably, the multi-drop topology for the clock distribution among the N precision-timing frontend ASICs will not be acceptable as it may degrade the clock quality even further, especially if N is high. A radiation-hard fan-out ASIC integrating the PLL IP block can simplify the clock distribution task, improving its quality and adjusting its phase (DAQ-frontend path length compensation, sampling point selection).

Note that having a clock feedback path from frontend to DAQ, as shown on Figure 2, can be beneficial for both distribution schemes. It makes possible to monitor slow O(100 Hz) to moderate O(10 kHz) rate phase drifts at the backend level and to derive calibration constants for on-line or off-line data corrections.

2. State of the art

Phased-locked loop components are widely used in communications, whether over the high-speed optical or copper media or wireless. Wideband devices with excellent jitter cleaning capabilities exist in industry, for example, from Skyworks [Si534x] or Texas Instruments [LMK5C33216]. Certainly, the use of these readily available components should be possible within the frontend boards, but mostly for the sub-detectors with the radiation environment ensuring a very low rate of single event upset (SEU) errors. Usually, the radiation tolerance figures for the COTS PLL are scarce. They are mostly available for components destined for space applications (see further in text). Even though the EIC radiation conditions are not challenging, they may still provoke SEU errors or, may-be, even a latch up event. Therefore, careful evaluation will be needed to determine whether a commercial PLL with interesting jitter cleaning capabilities and power consumption figures can be used within the EIC detector frontends.

In general, the very impressive features of the COTS components, in terms of wide input frequency range, fast locking time and jitter performance, is achieved with a complexity of their design (frequently a succession of two PLLs), subtleties of their fine-tuning in a large configuration phase-space and relatively high power consumption (1-3 W). Low power PLLs exist (e.g. [LMX2571] – 0.2 W), but the number of outputs is usually limited and the use of an external fan-out component

might be required. The commercial PLLs support zero delay mode of operation guaranteeing a deterministic phase relationship between the input and output clocks. In addition, often phased clock outputs (90°, 180°, 270°) are also available, but not the programmable fine phase adjustment.

The industrial PLL IP blocks do exist, but they are bound to the provider's process. The [PLL400MRHA] from Microchip is one example. The manufacturer provides its radiation tolerance figures. Based on its [ATMX150RHA] radiation-hard mixed signal technology for space applications, the PLL IP block has a very low power consumption (20 mW), but on expense of a poor jitter performance (up to 750 ps). In addition, it is designed in an old node technology (150 nm) that may not last long enough and that is not compatible with modern high-resolution mixed-signal microelectronic developments.

Probably the most performant PLL IP block available within the HEP community is the one designed for the lpGBT ASIC within the CERN Versatile Link Plus project [lpGBT]. The ASIC and hence the PLL has been implemented in 65 nm technology for low power operation (1.2 V supply) and extremely high radiation tolerance (200 Mrad and above, low SEU). Jitter cleaning capabilities of the IP block are excellent, with output clocks exhibiting less than 5 ps random jitter, and the RMS jitter varying from 4 to 10 ps for the frequencies in the range of 40-320 MHz. In addition, the lpGBT design provides the phase-adjustment possibility of some of the derived clocks with a step of ~50 ps.

Deploying the lpGBT PLL IP block within the 65 nm node frontend ASICs for the EIC experiments seems to be a right way to go. However, some important obstacles exist. The PLL is specifically designed for the LHC bunch-crossing clock of ~40 MHz on its reference input and with a narrow bandwidth of 1 MHz (the lock is achieved within the input frequency range of 39-41 MHz). The EIC bunch-crossing clock of ~100 MHz is far outside the range, so that even if its ½ harmonic is distributed, the lock will not be achieved. Tedious modifications are necessary to make the original design compatible with the EIC clock. The CERN design should be shared with the EIC electronics designer community (or at least with some part of it) requiring official establishment of a nondisclosure agreement (NDA) – a relatively long process. The PLL block is sufficiently complex and its redesign will necessitate an important support from the CERN lpGBT team – currently extremely busy with the LHC Phase 2 upgrade activities. Other non-trivial legal aspects, related to the use of the technology and the design utilities, will need to be solved as well.

Another jitter-cleaner clock synthesizer PLL available with the community is the one designed for the CMS high granularity calorimeter readout ASIC [HGCROC]. The design is done in the TSMC 130 nm technology. Though also meant to operate with the 40 MHz input clock, its locking bandwidth range is sufficiently high and can accommodate the sub-multiples of EIC 100 MHz clock. The radiation tolerance specifications of the IP is similar to those of the lpGBT, as both ASICs operate in the same environment. The access to the original design is simplified for its translation to the 65 nm technology as it belongs to the Irfu, CEA.

The trend of recent years, in industry and in academic research, is the development of all-digital PLL components (DPLL). They are gaining popularity due to their advantages in surface and in power consumption reduction, as well as due to improved scalability in advanced CMOS processes avoiding bulky passive elements of analog loop filters [DPLL]. Designers have demonstrated superior performance beyond the traditional analog PLLs thanks to abundant digital control loop architectures. Yet another novelty consists in deploying analog and digital loop control circuits in parallel. The resulting so-called hybrid PLLs (HPLL) allow sub-ps performances [HPLL]. In addition, new techniques such as the sub-sampling, the track-and-hold and the automatic loop gain control (ALGC) ensure robustness of PLL operation.

3. Research program

We propose to implement a new jitter cleaner clock synthesizer PLL IP block in the TSMC 65 nm technology. To assure the rapid initiation of the developments and minimize the failure risk, the design will be based on our experience with the 130 nm PLL. It will be extended with the fine phase adjustment capability of the output clocks and endowed with a compact ring oscillator to reduce the probability of single event transients. In addition to this safe development path, we intend to investigate the possibility of providing a digital regulation path in loop control circuitry of the PLL, introducing a novelty of hybrid PLL designs available within the HEP community. The goal is to achieve a superior jitter performance with a minimal increase in area and power of the IP block.

We have chosen the 65 nm technology from TSMC, in order to benefit from a large density of components, a high speed-over-power ratio and a demonstrated high radiation tolerance. We consider that the 65 nm node is an optimized price-performance tradeoff. In addition, this technology has been proven in many designs for elementary particle or nuclear physics, which is a good premise to reduce the development time and risks. In the following, we will present the specifications of the envisaged development.

The scheme of the proposed PLL block is shown on Figure 3. The frequency range of its reference input is deliberately wide in order to make its use possible for a large variety of the EIC detector frontends, as well as for non-EIC related applications. The PLL will operate with input clocks ranging from 75 to 125 MHz (100 MHz ± 25%). The performance optimization will be achieved by tuning several programmable parameters (by slow control over I2C bus) such as, for example, the charge pump biasing and the bandwidth of the low pass filter in the loop. The synthesizer stage will deliver multiple frequencies of the reference, up to at least 1.6 GHz, with the jitter lower than 10 ps. As has been already mentioned, the large variety of frequencies generated in the ASIC is mandatory for high-speed ADCs, fast digital processing and high-speed communications. In addition, the generated clocks can be phase shifted in steps as low as 300 ps.
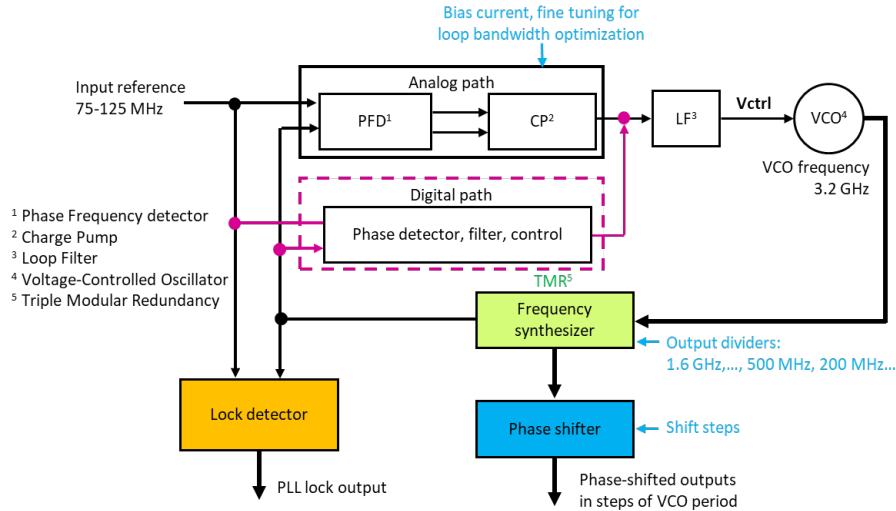

Figure 3: Schematic of the hybrid PLL with programmable parameters (in blue), main triplicated blocks and an optional digital loop control path in parallel with the traditional analog circuitry

Substantial effort will be devoted to build a low power, low area PLL. In particular, the technique based on the use of skewed gated delay cells [Sgdc] should allow to design a compact and stable voltage controlled ring oscillator (VCO) – a key element of any PLL – that we expect to be significantly less bulky than the LC-type ones. Naturally, the small area of the VCO, presenting a lower interaction cross-section with ionizing particles, will be favorable to achieve a high radiation immunity of the circuit. In addition, the radiation hardening of the entire PLL will be attained by deploying special layout techniques for Total Ionizing Dose (TID) tolerance and classical Triple

Modular Redundancy (TMR) techniques for SEU mitigation. Concerning the power consumption of the IP block, we aim to make it as low as 3 mW, in order to facilitate integration of the PLL in frontend ASICs and boards without adding an additional burden on their power and cooling requirements.

As has been already mentioned, during the initial studies, we would like to evaluate the opportunity to introduce an optional digital path in the loop control. In particular, an integral regulation holds a promise to bring a better stability and improve jitter characteristics of the PLL. Extensive simulations will be performed to elaborate an optimal architecture achieving negligible time and frequency quantization errors (*e.g.* number of TDC and DAC bits if respectively the digital phase detector and control units will be based on these elements). The digital regulation will be included in the design if it presents a noticeable improvement of jitter figures while requiring low additional area and power. The design will foresee the possibility to stop the digital path and operate the PLL through the conventional analog regulation only. The addition of a digital part allows to reduce the total size of the PLL especially on the LF part and also to better control the current injections in the charge pump in order to gain in jitter. Of course, it will be necessary to harden the digital logic nodes in order to keep the performance of the PLL in radiation environments. The challenge of this development is to combine these both aspects that drive our motivation to make this development. Nevertheless, this R&D study has a strong motivation, as it will allow evaluating potential area reduction of the loop filter in a future all-digital PLL, avoiding bulky passive components required by the analog control.

The table below summarizes the specifications of the PLL IP block.

Table of the characteristic of the proposed PLL IP block

Technology	CMOS 65 nm
Power voltage	1.2V
Input reference frequency range	75-125 MHz
VCO frequency	3.2 GHz
Number of output clocks	4
Output frequency	Programmable fractions of VCO frequency, up to 1.6 GHz
Phase shifter step	< 300 ps
Time interval jitter: analog path only	< 10 ps RMS up to 1 GHz with graceful degradation beyond
Time interval jitter: with digital paths	~3 ps RMS up to 1 GHz with graceful degradation beyond
Power consumption	< 3 mW, < 6 mW with digital regulation
Size	~0.1 mm²
Radiation mitigation	TMR, SEL free, TID up to 4 MGy

The project will pay special attention to validate thoroughly the PLL IP block. Testing a jitter-cleaner PLL with frequency synthesis and phase adjustment capabilities requires high-end equipment, in addition to a very accurate test bench design, deploying signal and power integrity techniques. The

envisaged organization of the test stand is shown on Figure 4. The team will adopt a modular approach to shorten the production time of the test bench and to lower its cost.

In order to assess ultimate performance of the PLL, keeping the possibility to evaluate its part-to-part variation, a PLL ASIC carrier board will be designed with a minimal on-board functionality. As a baseline option, the project favors encapsulation of the PLL IP block in a widely used package (*e.g.* QFN), rather than working with bare chips. The latter is considered as a backup option if for some reasons packaging cannot be done in time (*e.g.* delay due to mismatch with the foundry tape-out schedule). It is worth to note that our groups have at their disposal advanced wire-bonding machines from FEK Delvotec [5632], [5832] and can therefore mitigate the risk related to foundry delays by deploying bare chips on the test bench PCBs. The production of a relatively simple PLL carrier board in quantities necessary for the tests will be fairly fast and should not be costly. For radiation tolerance or environmental tests, the carrier board can be placed in the irradiation facility or in the climate chamber connected to the rest of the system over high performance cables.
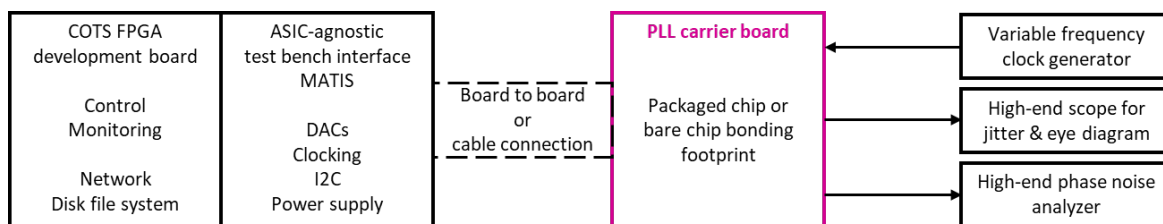

Figure 4: Test bench organization for the PLL IP block

The control and monitoring of the PLL will be performed through a proven combination of a COTS FPGA evaluation kit [ZedBoard] and IRFU in-house development [MATIS]. The latter is a versatile electronics board providing generic interfaces to implement rapidly test bench systems for the ASICs produced by the local microelectronics group.

A variable frequency clock generator will deliver the reference input clock to the PLL IP block. We own a very accurate clock source [HPTC] that can generate precision 80 MHz clocks (the HPTC is used as a standard benchmark component in the precision timing evaluation systems at CERN). We also have at hand various clock-synthesizer PLL evaluation boards [*e.g.* Si5344-D] allowing us to scan the whole range of input frequencies of the designed PLL. Deliberately miss-programming the external clock-synthesizer PLL, it is possible to degrade the input clock quality in order to verify the jitter-cleaning capability of the PLL IP block under test.

The high-end measurement instruments, the LeCroy [SDA 820Zi] scope and the Milexia [5125A] phase noise spectrum analyzer, will be used for accurate performance assessments of the PLL. The former is a 20 GHz bandwidth 80 GSPS 4-channel scope with serial data analysis features such as time-interval error (TIE) jitter and eye diagram measurements. The latter performs phase noise analysis of up to 400 MHz clock in the 1 kHz-10 MHz frequency range. Both appliances can be remotely controlled, making it possible to perform automated scans to validate the phase shifter capabilities of the PLL. In addition, the phase noise analyzer will be particularly useful to study the power supply ripple rejection (PSRR) of the proposed design.

The very first target for the new PLL IP block is the versatile SALSA ASIC currently under development for the MPGD readout [SALSA]. It will be readily available for other frontend ASICs to be designed for the EIC detector 1 or detector 2 experiments. In addition, the EIC community will benefit from the base design for radiation hardened jitter cleaner fan-out ASIC to be used for precision clock distribution within the sub-detector frontends.

4. Task definition and schedule

The research program is divided into four tasks.

Task 1: design and simulations

Development of the PLL block will be done by staff microelectronics engineers at IRFU, who are skilled in the design of precision timing circuitry. Simulations will be done using the 65nm PDK kit provided by TSMC with the standard 9-metal layers option. The design will be augmented with a fine phase shifting capability of the generated clocks. A serial slow control interface will allow tuning of various configuration parameters to adjust the PLL performance to the desired application. Four months are foreseen for this task. The deliverable of this task will be the final design ready for prototyping.

Task 2: production

The design will be submitted to TSMC using the mini@sic program suitable to produce up to 2x2mm² dies. This is large enough to house the PLL block and the required support logic. The production delay is between 3 to 4 months. The deliverable will be a set of 100 prototype dies.

Task 3: packaging, tests and performance measurements

To simplify the handling of the dies it is intended to package them. But the constraint to test bare dies is not ruled out and the project will be prepared for this eventuality. The choice will be done in time, according to the prospected schedules of the foundry and packaging companies. With the modular test bench architecture described above, only the low-complexity design of the PLL carrier board will be altered by the decision. The validation of the PLL functionality will be carried out at IRFU by an intern student supervised by an experienced staff electronics engineer. All the equipment necessary to wire-bond the dies, to exercise the PLL IP block with a reference clock of variable frequency and quality, and to perform precision jitter and phase noise measurements are readily available in the lab. The deliverable will be a report on the performance of the PLL block.

Task 4: environmental tests

The prototypes will be tested in harsh environmental conditions, in particular under ionizing radiation and at low temperature. The TID irradiation campaigns are foreseen by the University of Sao Paulo facility to study the aging impact on the PLL performance. The SEU resistance of the design will be studied in a proton beam, for instance, at the PS accelerator at CERN. The opportunity of neutron irradiation at Jozef Stefan Institute (Ljubljana, Slovenia, EU) will be evaluated too. The climate chamber at Irfu allows studying the PLL performance in the temperature range from -30°C to +60°C.

The timeline of the project is presented in the following Gantt diagram (Figure 5).
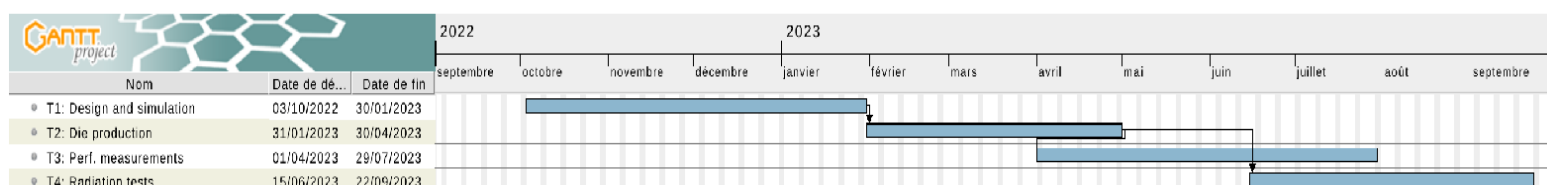

Figure 5: GANTT diagram of the project, with the four tasks described in the text

5. Budget

The requested budget would be mainly dedicated to the production and packaging costs of the PLL prototypes, as well as the production cost of the PLL carrier board and the test bench assembly.

The prototypes will be produced through the mini@sic program from TSMC, for a cost of about 18 k$. The packaging of the chips can be performed by the French SERMA company. Together with the PLL carrier board design and the test bench infrastructure a 10 k$ budget should be secured for this activity. As it has been already mentioned, all clock generation and precision measurement equipment is already available within the project.

As described above, the TID radiation tests will be done in an irradiation facility at University of Sao Paulo for a cost of 5 k$. If decided, the neutron irradiation tests at Jozef Stefan Institute (Ljubljana) will require about 1 k$. Other radiation tests will be done in a proton or hadron beam facility, for instance at PS accelerator at CERN.

An intern student will participate in the instrumentation of the test bench at IRFU and to the validation and performance assessment of the PLL prototypes. Other participants are staff technicians, engineers and physicists.

Table of the requested budget of the project

Nature of expenses	Cost	Group
Mini@sic submission	18 k$	IRFU
Packaging and test card production	10 k$	IRFU
TID radiation tests	5 k$	U. Sao Paulo
SEU radiation tests	10 k$	IRFU
4-6 month intern student ?	6 k$	IRFU
Travels for radiation tests	5 k$	IRFU
Total	54 k$	

a. Case of budget minus 20%

With a decrease of the nominal budget by 20%, it will not be possible to hire the intern student. The corresponding work will be taken in charge by the staff members, with the drawback of the PLL performance exploration in a partial parameter space only. The radiation tests will be limited to shorter TID and SEU campaigns, while the neutron irradiation tests will be excluded.

b. Case of budget minus 40%

With the decrease of the nominal budget by 40%, in addition to the above, the expenses will be limited to the mini@sic production and to the performance measurements on bare dies. The latter will certainly compromise the assessment of the part-to-part variations of the PLL performance. In addition, the radiation test campaigns will be seriously endangered, most probably excluding the SEU studies. In this condition, one of the major objectives to develop an SEU tolerant component will remain questioned.

6. Money matrix

A summary of all expenses per institute and per activity of the project are presented in the table below.

Table of the money matrix

	ASIC production	Tests	Radiation tests	Travels	
IRFU CEA Saclay	18 k$	16 k$	10 k$	5 k$	49 k$
U. Sao Paulo			5 k$		5 k$
	18 k$	16 k$	15 k$	5 k$	

7. Abbreviations

ADC – analog to digital converter
COTS – commercial off-the-shelf
CSA – charge sensitive amplifier
DAC – digital to analog converter
EIC – electron-ion collider
ENOB – effective number of bits
I2C – inter integrated circuit (bus)
IP – intellectual property
LPF – low pass filter
MPGD – micro-pattern gaseous detector
PDK – platform development kit
PFD – phase frequency detector
PLL – phased-lock loop
PSRR – power supply ripple rejection
SEL – single event latch-up
SEU – single event upset
SNR – signal to noise ratio
TDC – time to digital converter
TID – total ionizing dose
TIE – time interval error
TMR – triple modular redundancy
ToF – tile of flight
VCO – voltage controlled oscillator

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