Development of a Generic, Low-power and Multi-channel Frontend Readout ASIC for Precision Timing Measurements at EIC

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Abstract:
Among the key components of precise timing detectors is the frontend readout ASIC chip that will measure both the arrival times and amplitudes of signals, and its integration with the sensor and data acquisition system. This research builds upon the completed development of a single-channel timing ASIC developed at Fermilab and will extend it to larger systems. The proposed solution can be used for a variety of applications, such as AC-LGADs, or photon sensors of Cherenkov detectors, to extract timing at 25 ps resolution and signal amplitude. The research program presented in this proposal will develop a *generic, low-power multi-channel* ASIC to measure both the arrival times and amplitudes of signals from such detectors. The proposed solution will utilize an ASIC with Constant Fraction Discriminator (CFD) that does not require offline corrections, calibrations or corrections and is simple in operation and can have a better overall performance over extended periods.

Proposal Section

Overview

Precise timing measurement plays a critical role in future collider experiments. Detectors capable of achieving around 25 ps and around 10 μm position resolution are needed for many proposed future experiments including the FCC-hh [1, 2] and Electron–Ion Collider (EIC) [3]. Such detectors are included in the EIC Project Detector design, including a layer of AC-coupled Low Gain Avalanche Detector (LGAD) detectors for Time-of-Flight (TOF) particle identification (PID) and tracking, and in the far-forward detectors to measure the scattered protons in exclusive processes. Precise timing information is also highly desirable for photon sensors (SiPM, MCP-PMT, or LAPPD) of Cherenkov detectors at EIC, including time-based imaging of Detection of Internally Reflected Cherenkov light (DIRC), and reconstruction of the Cherenkov angle by suppressing ambiguities due to reflections in the bar and prism. Ultimately fast timing may even make it possible to mitigate the influence of the chromatic dispersion of the Cherenkov angle and to further improve the PID performance [4]. **The research program presented in this proposal will develop a *low-power multi-channel* ASIC to measure both the arrival times and amplitudes of signals from such detectors. This program will build upon our recent successful development of a *single-channel* prototype.**

Front-end electronics (FEE) is the interface between the detector and DAQ. Efficient hit detection, while maintaining excellent timing, is the main task of the FEE. Moreover, The FEE has to provide calibration, monitoring and slow control functionality, e.g., setting thresholds or monitoring temperatures. Last, but not least, it must cope with the tight volume constraints and low power consumption demands. To achieve the desired timing resolution, various approaches have been taken. Traditionally, TOF detectors use a discriminator in combination with TDCs to measure the Time-of-Arrival (ToA) and Time-over-Threshold (ToT), or TDC and ADC to measure the ToA and signal amplitude. The ToT or signal amplitude is needed to apply time walk correction on the measured ToA to reduce the dependence of the ToA on signal amplitude. Such a dependence can change with bias voltage, temperature, or total irradiation dose that affect the signal amplitude. Therefore, a time walk correction needs to be applied to each channel separately to accretive the optimal timing resolution. Alternatively, the baseline design for EIC Cherenkov detectors uses FEEs with waveform sampling digitization which require more power and larger bandwidth than the ToT approach, which could become more severe as the dark current increases due to irradiation damage. **Our proposed solution utilizes an ASIC with Constant Fraction Discriminator (CFD) that does not require offline corrections, calibrations or corrections and is simple in operation and can have a better overall performance over extended periods.**

This research program will leverage on the ongoing efforts of the PI and his collaborators at FNAL to develop and characterize precision timing sensors (e.g., AC-LGADs and MCP-PMTs) and timing ASICs. The main deliverable of this project is a low-power multi-channel frontend readout ASIC that achieves time resolution of around 25 ps. The ASIC will also provide information on signal amplitude, which can be used to determine hit position with a resolution around 5 μm when combined with AC-LGAD sensors. The potential scientific and technical impacts of the project are substantial: the design of a novel precision timing multi-channel ASIC that will enable exploration of entirely new and unexplored phase space at EIC and future experiments.

Proposal

We propose a development of an ASIC using a novel approach based on ASIC that uses Constant Fraction Discriminator (CFD) for time-of-arrival timestamping of signals [5]. The CFD approach does not require time-walk correction, unlike traditional approaches that use Leading Edge discrimination. Therefore, in combination with low power TDC, such a readout architecture can provide excellent time resolution with low power consumption and provide a reliable operation without continuous monitoring and time-walk corrections. The performance of the ASIC developed in this research program will be continuously characterized using the existing testing infrastructure, such as the precision timing laboratory at Fermilab SiDet and UIC. At the end of the research program a single-layer demonstrator system will be installed and tested at FTBF to simultaneously measure particle timing and position with resolutions of 25 ps and 5 μm.

A typical ASIC for detector readout consists of both analog and digital processing blocks. The analog block incorporates a fast preamplifier and discriminator to perform the time of arrival measurement. The digital block receives the output from the analog block and generate a timestamp using a Time-To-Digital Converter (TDC), plus perform the overall configuration of the device, send and receive communications from the detector back-end, etc.

Design of the front-end electronics capable to extract precision timing information from LGAD sensors presents many challenges but plays a key role in the applications of the LGAD technology. The Fermilab and UIC team has been studying optimal methods for extraction of timing information from LGADs, using either Leading Edge (LE) or Constant Fraction Discriminator (CFD). Timestamping using the LE requires time-of-walk correction for optimal time resolution of the reconstructed signal, due to the dependance of the threshold-crossing on the signal amplitude. The CFD discriminant does not require such a correction and is therefore much simpler to operate and implement in large systems, without a need to derive and monitor signal dependence as the detector ages. Additionally, our studies in [5] showed that CFD outperforms LE for smaller signals, making it a preferred choice for AC-LGAD sensors which have smaller signals in non-primary channels due to signal sharing.

Following the studies presented in [5] the Fermilab team designed and produced the single-channel version an ASIC based on the CFD concept using TSMC 65nm technology (Fermilab CFD version 0, or FCFDv0). The FCFDv0 uses several new techniques to achieve low power, area, jitter, time walk. This enables a simple and robust timing measurement (~30 ps) of LGAD signals that vary in amplitude by at least a factor of 10, with no critical threshold setting or corrections required. The FCFDv0 is a single-channel ASIC that only contains analog blocks, i.e. the amplifier and discriminator. Another critical feature in the design and implementation of the ASIC was complete testability with simple bench-top equipment, to properly characterize and adjust the settings on the chip for optimal operation.

The FCFDv0 forms both an attenuated and a delayed version of the amplified input pulse. The input stage is an integrator with a feedback capacitor and a parallel feedback resistor to provide "slow" continuous reset. The attenuated signal is derived very efficiently by splitting the integration capacitance into two series capacitors and buffering the midpoint node. The delayed signal is formed by a programmable RC delay on the integrator output, followed by a buffer. These

two buffered signals then directly feed a fast differential amplifier. The single-ended output of the differential amplifier feeds a very simple output comparator that compares it to an internal DC threshold voltage. The biasing of the integrator and differential amplifier chain is critical to achieving the best performance and eliminating the need for any trimming. The integrator capacitor midpoint must have a DC bias established, and the differential amplifier has a significant random input offset. A servo loop is used to establish the differential amplifier output voltage by sensing and filtering it and comparing it to an on-chip DC level setting. The capacitor midpoint is then driven appropriately to establish the desired DC output level of the differential amplifier. In a classical CFD, the output comparator would have its threshold set to the quiescent value of the differential amplifier output. However, large signals have more comparator overdrive than small signals, and thus smaller delays. To compensate for this effect, the differential amplifier output is biased at a critical level away from the comparator threshold.

The FCFDv0 chip has been characterized using internal charge injection circuit [6], and recently using an infrared (IR) laser at SiDet. The performance of the FCFDv0 chip was initially tested using the internal charge injection circuit. The LGAD-like pulse corresponding to a 50 μm thick DC-LGAD with 1.3x1.3 mm^2 pixels (C_{in}=3.4 pF) was injected into the circuit to emulate the realistic signals, and signal size was varied from 2.4 to 25.8 fC. The input transistor current was varied from 520 μA to 820 μA to study the dependance on the gain of the amplifier. Results are shown in Fig. 1 and demonstrate that the chip can measure the ToA down to about 8 ps with simulated signals. We also studied the delay of signals of various signals, to evaluate whether any residual time-walk correction is still necessary and observe negligible dispersion of the ToA of signals of different sizes, therefore demonstrating no need for time-walk correction.

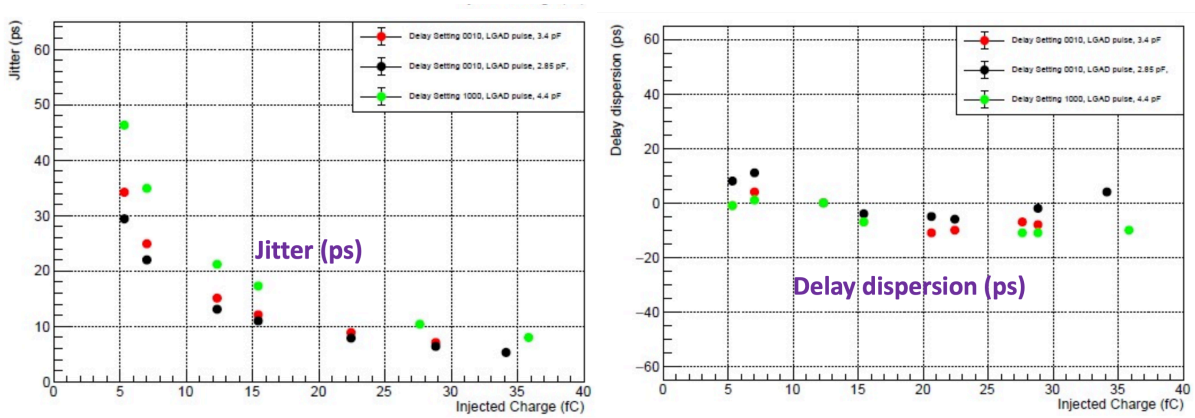

Figure 1: Measured delay jitter (left) and delay dispersion (right) vs. input charge. Red, black, and green points correspond to 3.4, 2.85 and 4.4 pF respectively.

As a next step we moved to characterize the performance of the FCFDv0 chip using signals from DC-LGAD sensors. A specialized readout board was designed by the Fermilab team for the measurements with source, shown in Fig. 2. For this test, sensors of 1.3x1.3 mm^2 are used. Sensors mounted on the dedicated readout board were placed inside an environmental chamber, and a PiLas IR sensor directed at the opening in the metallization on the surface of the channel connected to the input of the FCFDv0. The output of the comparator was sent to one of the channels of the Lecroy Waverunner 8208HD oscilloscope, and the output of the trigger channel of the PiLas laser to the other channel. The difference between the time of arrival of two signals was then

histogrammed, and the width of the distribution is extracted to evaluate time resolution of the LGAD+FCFDv0 system. The resulting dependance on the bias voltage applied to the LGAD is shown in Fig 2, demonstrating that we achieve around 30 ps time resolution in a system containing real signals from LGADs, consistent with expectations for this LGAD sensor [7]. Measurements with test beam will be performed during Fall 2022 at FTBF, when the beam operations resume.

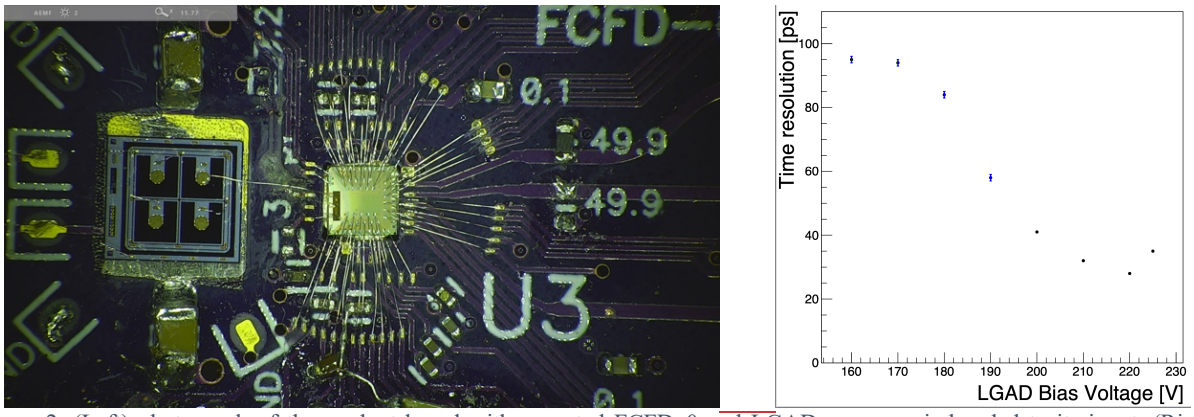

Figure 2: (Left) photograph of the readout board with mounted FCFDv0 and LGAD sensors wirebonded to its input. (Right) Measured time resolution using FCFDv0 with LGAD signals that detect signals from an IR laser, as shown on the left image.

The PI proposes to develop the next generation of the FCFD chip, a specialized low-power and multi-channel ASIC designed to read out signals from either LGADs or MCP-PMTs (such as LAPPD). This next stage of the development program (FCFDv1) will reuse the main components of the analog part of FCFDv0, such as the preamplifier and discriminator, but will target the addition of charge measurement needed for position reconstruction in sensors such as AC-LGAD or LAPPDs. The multi-channel ASIC would allow the PI and his collaborators to build a large-area demonstrator of the technology that would be able to perform simultaneous measurements of position and timing of the passage of charged particles. The development of this version is expected to take the first half of BY1. After the successful demonstration of the system readout with a 10-channel system during BY1 and BY2, the next step, FCFDv2 would aim to build a full chip, including the digital readout, during the second half of BY2 and first half of BY3 (10-channel FCFDv2). The final, mixed-signal ASIC will be produced and tested during BY3, and its performance will be characterized using a single-layer AC-LGAD demonstrator at FTBF.

Performance characterization of the ASICs will be carried out at FTBF. Our group has performed detailed studies of AC-LGADs using our test-stand at FTBF, shown in Fig. 3. The FTBF provides a 120 GeV proton beam from the Fermilab Main Injector accelerator. The AC-LGAD are wire-bonded to a 16-channel readout board, designed at Fermilab. The 16-channel board is designed to test sensors with sizes as large as 8.5×8.5 mm^2 at voltages up to 1 kV. Up to sixteen sensor outputs can be wire-bonded to the input pads of 2-stage amplifier chains based on the Mini-Circuits GALI-66+ integrated circuit. In this configuration amplifiers used a 25 Ω input impedance, an approximately 5 kΩ total transimpedance, and a bandwidth of 1 GHz. The FTBF is equipped with a silicon tracking telescope to measure the position of each incident proton. The position resolution of the proton track is in the range of 5–10 μm, which is comparable to the expected resolution of the AC-LGAD sensors. A Photek 240 micro-channel plate (MCP-PMT) detector, placed inside the environmental chamber downstream from the AC-LGAD provided a precise reference timestamp

that was measured to be smaller than 10 ps. The AC-LGAD and MCP-PMT waveforms were acquired using an 8-channel Lecroy Waverunner 8208HD oscilloscope. This oscilloscope features eight readout channels with a bandwidth of 2 GHz and a sampling rate of 10 GS/s per channel.

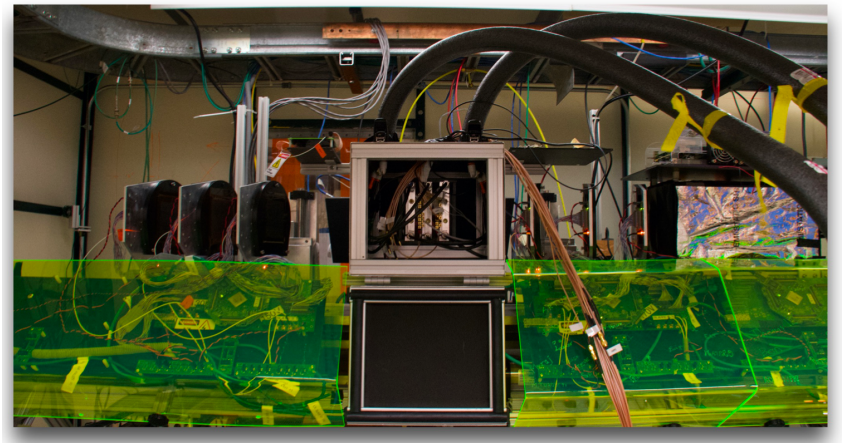

Figure 3: A photograph of the environmental chamber placed within the FTBF silicon telescope.

Using AC-LGAD sensors produced by our collaborators at Brookhaven National Laboratory (BNL), we performed detailed studies to extract the specifications needed for the FCFDv1 ASIC, such as the required precision in the extraction of the signal amplitude, the dynamic range of signals to with optimized timing resolution. The capacitance of the input sensors needs to be optimized depending on the sensors to be used with the ASIC, but we will select a specific set of sensors for the development of the demonstrator ASICs such that it is suitable for potential applications at EIC.

Candidate specifications for the next version of the ASIC were derived using a sensor produced by BNL in 2020 with strip widths of 80 μm and pitch of 100 μm [8]. Due to the design of AC-LGAD sensors, the signals are shared with the neighboring channels. The sharing is smallest when a particle passes through the center of the metalized strip, and largest when particles pass in the gap between the strips. The distributions of collected signal amplitudes shown in Fig. 4 show that the minimal signals that the ADC needs to be sensitive to correspond to about 2 fC, and maximum signals are about 64 fC.

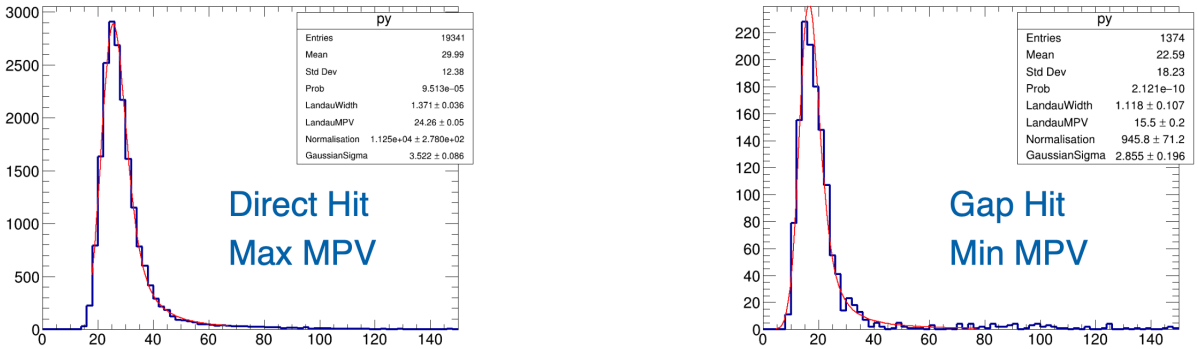

Figure 4: The distribution of the amplitude of the signals collected when particles pass through the center of the strip (left) and through the gap between strips (right). The X-axis shows the amplitude of signals in mV. Conversion to collected charge can be approximated by signal MPV/5.

The estimation of the required precision of the signal amplitude ADC is estimated as follows. The effect of ADC binning on the measurements of the signal size can be approximated by introducing an artificial smearing on the measured amplitude. We multiplied each channel's amplitude by a random number from a Gaussian distribution, with mean 1.0 and varying its sigma. Results are presented in the Fig. 5 and demonstrate that a 1-2 fC upper limit on needed amplitude resolution is sufficient.

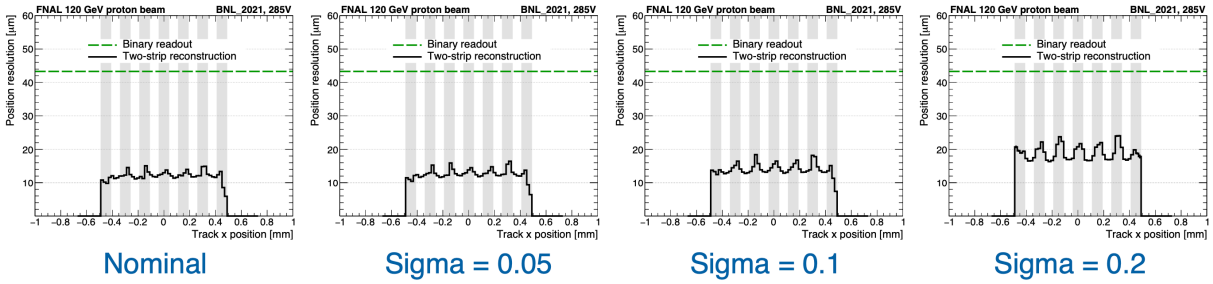

Figure 5: Position resolution for several options for signal smearing.

Detailed Timeline

A year-by-year timeline with proposed milestones and deliverables are described in the following subsections, and the timeline is shown in the schematic diagram in Tab. 1.

Table 1: Year-by-year timeline of the project

Activity	BY1	BY2	BY3
Development of FCFDv1, production, and start testing			
Characterization of FCFDv1 in beams, design of FCFDv2			
Production of FCFDv2 and testing in beams			

Budget Year 1 (BY1)

In BY1 the PI will lead the study to finalize the specifications for the 10-channel FCFDv1 ASIC such that it is optimized for sensors suited for applications in EIC experiments, such as AC-LGADs with 500 μm pitch and 1.0 cm length of strips, and MCP-PMT. The signal size of both detectors is comparable within a factor of 10, and simple modifications to the ASIC would allow the same electronics to be used for both detectors. Upon the completion of this study, the PI and his co-I will lead the development of the ASIC and its submission to TSMC to manufacture a set of prototypes. Testing on the bench by the lead engineer will be performed first to validate the basic performance, followed by testing with the ASIC connected to an AC-LGAD and MCP-PMT in test beams.

Deliverable #1: Specifications for the FCFDv1, and selection of the sensors for demonstrator.
Deliverable #2: Design, submission, and initial testing of 10-channel FCFDv1.

Budget Year 2 (BY2)

In BY2 the team will focus on detailed characterization of the FCFDv1 chip, using laser, beta source, and FTBF test beams. Performance will be compared to simulations, and measurements of timing and position resolutions will be studied in detail. Results will be summarized in a publication. The design of the mixed-signal, final FCFDv2 will commence in the middle of BY2, once the initial set of results is already available and can guide the further developments of the ASIC. The digital part of the ASIC will be largely followed from similar ASIC developed by the Fermilab team for the CMS experiment [9] and will integrate the analog front-end developed in BY1.

Deliverable #3: Detailed characterization of the FCFDv1 performance summarized in a publication.
Deliverable #4: Design of the mixed-signal final 10-channel FCFDv2 ASIC for the demonstrator.

Budget Year 3 (BY3)

In BY3 the team will submit the final version of FCFDv2 for production at TSMC. A full system for DAQ and reconstruction will be developed while waiting for the return of the ASIC from the foundry, and tests will be carried out at the FTBF facility. Several large-area modules of AC-LGAD wire-bonded to the FCFDv2 will be assembled and inserted into a telescope for test-beam studies at the FTBF, which will be followed by detailed data analysis and publication.

Deliverable #5: Completed technology demonstrator, detailed studies of its performance and publication.

Funding requests and budget for Budget Year 1

In this proposal the PI requests funding only for the first year: **BY1**. We intend to continue this research program towards completion in BY2 and BY3 upon the successful completion of BY1.

To carry out the outlined research program, the PI is requesting funding to support an ASIC design engineer at 0.5 FTE at Fermilab ($150k), production cost of the ASIC submission ($25k), and 2 months of electronics engineer at UIC to design a dedicated readout board for mounting and readout of FCFDv1 ($30k). The ASIC design will be carried out by FNAL engineer Tom Zimmerman, who has decades of experience in designing ASICs for particle physics experiments, such as the QIE used in CMS experiment at the LHC [10], and FLORA for X-ray experiments at LCLS-II [11]. T. Zimmerman is not involved in any other projects and is fully committed to the development of FCFD ASIC in the coming years.

We studied three budget scenarios and the impact on the project deliverables, and present our findings below:

- a realistic nominal budget (baseline budget)
    - Deliverables for this budget are presented in the project narrative above
- a nominal budget minus 20%
    - The impact of 20% budget reduction would result in a reduced amount of ASIC design verification before submission. In case of such a reduction, the PI will focus the design on a reduced channel ASIC, e.g. 5-channel ASIC instead of originally planned 10-channels, to simplify the design verification stage.
    - **Deliverable #1:** *would be fully accomplished*
    - **Deliverable #2:** *would be a reduced 5-channel FCFDv1*
- a nominal budget minus 40%.
    - The impact of a 40% budget reduction would result in a significantly reduced amount of ASIC engineer effort. In case of such a reduction, in addition to the strategy outlined for the 20% reduction, the PI will also direct the ASIC engineer to not focus on power consumption optimizations for FCFDv1
    - **Deliverable #1:** *would be fully accomplished*
    - **Deliverable #2:** *would be a reduced 5-channel FCFDv1, without power optimization.*

Research Team

To carry out his research program the PI is requesting funding to support an ASIC engineer (T. Zimmerman, Fermilab), and electronics engineer at UIC. During the research project, the PI and co-I will focus on providing close support to team and engineers to maximize the group's achievements. The group will include a postdoc (C. Madrid) and a graduate student (S. Nanda) working with the PI and co-I on the development of precision timing detectors. The postdoc is funded by co-I Early Career Award. The PI and co-I will also collaborate with FNAL scientists S. Xie and C. Peña on the design and characterization of the FCFDv1 chip. The team also includes postdocs and graduate students from collaborating institutes (Caltech, BNL, UCSC, University of Santa Maria Chile).

Throughout BY1, the FNAL and UIC engineers will design the FCFD ASIC, and readout boards for testing with AC-LGAD sensors. The UIC and FNAL postdocs and students will develop the ASIC specifications based on detailed studies of test-beam data from AC-LGAD sensors, develop the DAQ, and perform the characterization of sensors in test-beams. A detailed Money Matrix is presented in Tab. 2. Subprojects associated with the efforts of postdocs and students do not require funding from this award.

Table 2: Money Matrix

	Development of specifications	Design of the ASIC	ASIC production	Test board design	Travel	Total
Fermilab		$150k	$25k			$175k
UIC				$30k	$5k	$35k
Total		$150k	$25k	$30k	$5k	$210k

Cost Effectiveness

In all cases, priority will be given to domestic manufacturers when available. The AC-LGAD sensors are produced domestically. The program will leverage on the facilities and equipment that already exist at Fermilab and UIC for testing and characterization of the prototype detectors, thus significantly reducing the overall cost of the project. Teleconference meetings will be held instead of in-person meetings whenever possible to reduce the carbon footprint. The project has minimal exposure to supply chain challenges due to its reliance on already existing equipment and facilities.

Diversity, Equity, and Inclusion

The PI is committed to excellence in mentorship and advancing the careers of junior researchers, including students and postdocs. The PI is committed to fostering a collaborative culture with diversion, inclusion and equity.

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