Implementation of a gain layer in Monolithic Active Pixel Sensor (MAPS) for high resolution timing application

A. Camsonne*,[1] Y. Degerli,[2] F. Guilloux,[2] J.P. Meyer,[2] P. Schwemling †,[2] and H.S. Jo+[3]

[1] *Thomas Jefferson Laboratory, Virginia, USA*
[2] *CEA IRFU Saclay, France*
[3] *Kyungpook National University, Daegu, Republic of Korea*

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Abstract

Monolithic Active Pixels Sensors (MAPS) have been very successfully used as trackers. The integrated electronics allows for thin sensors and high degree of pixellization, giving them excellent position resolution with low material budget and excellent signal to noise ratio. On the other hand most MAPS have a fairly moderate timing resolution, but the technology has enough flexibility to optimize it for time measurement. We are proposing to create DMAPs optimized for timing by creating a gain layer. We expect timing resolution to be improved with the end goal to reach performance as good as LGAD or SiGe technologies but with the lower power consumption of DMAPs.

† PI and contact :Philippe.Schwemling@cea.fr
+CoPI : hyonsuk@knu.ac.kr
*CoPI : camsonne@jlab.org

I. INTRODUCTION

Monolithic Active Pixels Sensors (MAPS) consist of a silicon detector will built-in readout electronics in the same silicon substrate.

This gives several advantages :

- The front-end readout electronics is as close as possible to the sensor giving the best signal to noise ratio.
- Since amplification can be implemented on the same substrate as the sensor, a thinner sensor can be used, giving it the best material budget.
- This technology significantly reduces the amount of electronics, driving the costs down and simplifying the deployment of the detector compared to hybrid solutions.

An example of this technology is a Deep Nwell MAPS as shown in Fig. I.

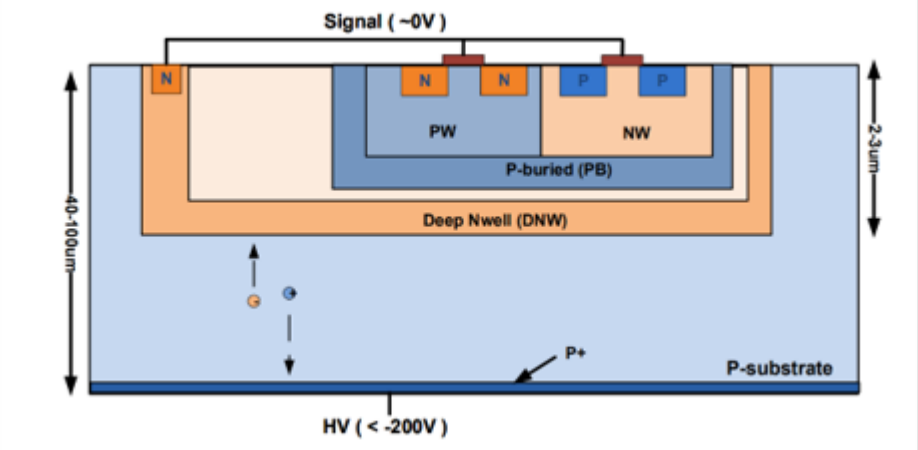

FIG. 1. A cross-section of a DMAPS pixel. Pixel readout electronics is enclosed in a Deep Nwell structure.

Such detectors have been very successfully used for tracking purpose. The baseline vertex tracker is based on ALICE ITS3 MAPS technology, but timing resolution has been a bit lagging since in most MAPS application the device is optimized for amplitude and position rather than timing. Most existing MAPS have timing resolution above 100 ps. Currently layers of Low Gain Avalanche Diode (LGAD) are considered for timing purpose, they provide down to 25 ps level but the implementation is slightly less straightforward than MAPS due to coupling to the readout ASIC via bump bonding and cooling requirements. A timing MAPS layer would give the same ease of integration as the ITS3 MAPS tracker, greatly simplifying installation and integration of services for the detector.

Suitability of Depleted Monolithic Active pixel Sensors (DMAPS) devices as radiation–tolerant detectors for tracking and timing has already been largely demonstrated [1] [2] [3] [4] [5], [6]. Building on this experience we explore the possibility of using high voltage, high resistivity CMOS pixel sensors as a low cost, high performance, radiation hard alternative to the LGAD (Low Gain Avalanche Detector) concept. We focus on the LFoundry LF15A technology, since we have experience with this process from past developments of several successful tracking and timing-oriented sensors. Other comparable technologies, like AMS180/TSI180 or TJ180 are also a possibility, if LF15A turns out not to be accessible in the medium/long term. Several iterations of a sub 100 ps timing sensor have been developed and tested at Irfu, in collaboration with Bonn. Test beam data taken in October 2021 at CERN with the RD-51 team show a time resolution of 90 ps [7] on Minimum Ionizing Particles for a 0.5 mm $\times$ 1 mm pixel, implemented on a wafer thinned down to 200 µm. Further optimisation of the front-end settings and increasing the high voltage from 280 V to 400 V on the same sensor has pushed down to 65 ps [8].

II. RELEVANCE TO EIC DETECTOR 1 AND DETECTOR 2

Such technology could be applied wherever MAPS or LGADs are being used i.e. for the vertex tracker as shown in Fig.3 or timing layers (Fig. 3) found in the Yellow report [9] generic detector design or the ECCE detector which was chosen as the reference detector where ToF is used for PID at low momentum 4.

It could also be a possible readout for the ATHENA imaging calorimeter which could be considered an upgrade of detector 1 or for detector 2.

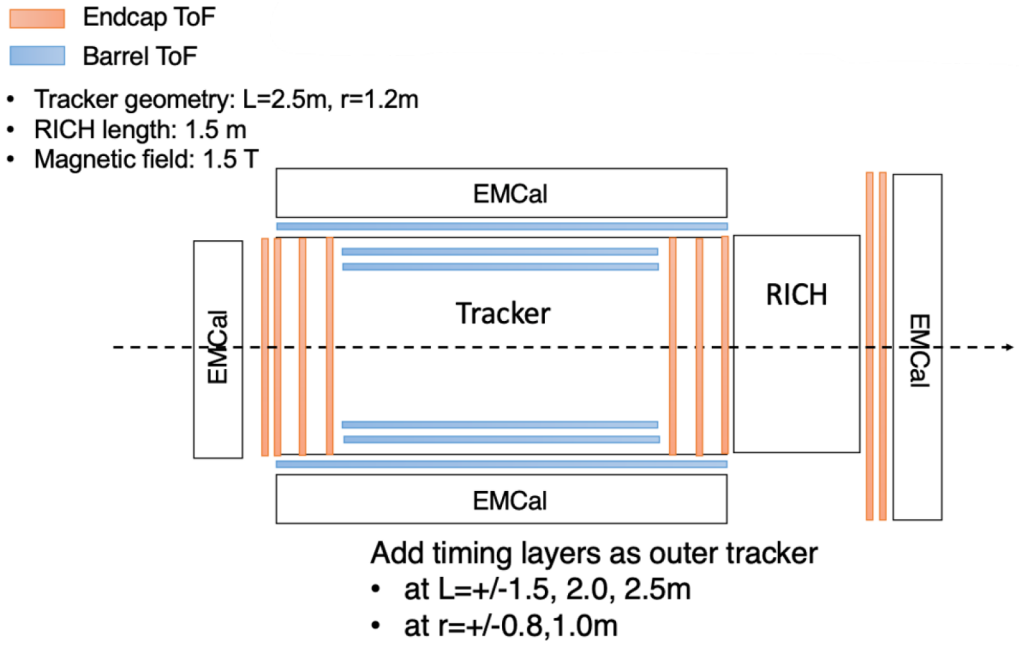

FIG. 2. Time of flight layers for Yellow Report generic detector

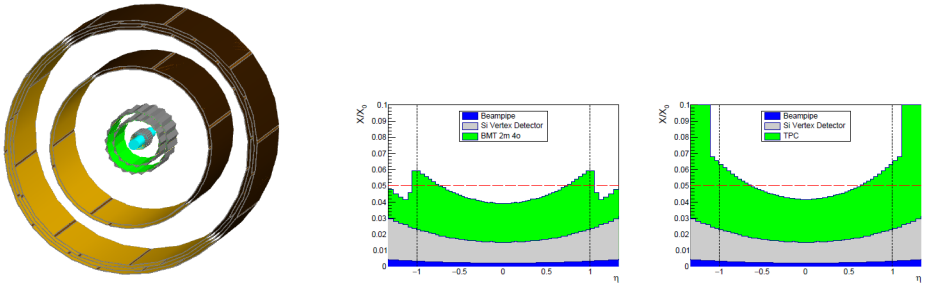

Figure 11.30: (left) A possible configuration of the cylindrical MPGD tracker with two pairs of layers at mid way between the SVT and the four outer detector layers. The material budget of the hybrid detector with MPGD layers (center) is comparable with the TPC solution (right). In the stack plots, the contribution of the beam pipe in blue, in gray the one of the silicon vertex detector and in green the MPGD tracker (or TPC) contribution.

FIG. 3. Hybrid Silicon Vertex and MGPD tracking solution for YR generic detector

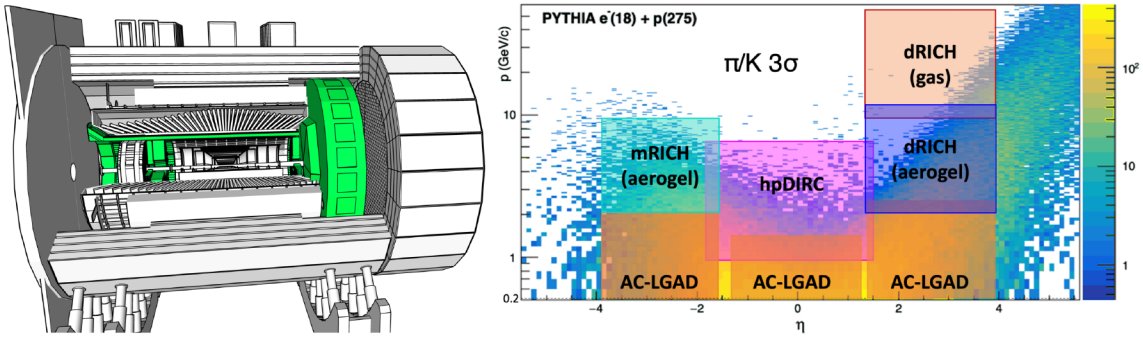

FIG. 4. ECCE PID detectors momentum range

1. *Current state*

From table in Fig. 5 the presentation done by N. Cartiglia , 4 D Tracking, LGAD and Fast Timing Detectors, at VCI2022, we can summarize the different solid state technologies available with a few key parameters.

Name	Sensor	node	Pixel size	Temporal precision [ps]	Power [W/cm²]
ETROC	LGAD	65	1.3 x 1.3 mm²	~ 40	0.3
ALTIROC	LGAD	130	1.3 x 1.3 mm²	~ 40	0.4
TDCpic	PiN	130	300 x 300 µm²	~ 120	0.45 (matrix) + 2 (periphery
TIMEPIX4	PIN, 3D	65	55 x 55 µm²	~ 200	0.8
TimeSpot1	3D	28	55 x 55 µm²	~ 30 ps	5-10
FASTPIX	monolithic	180	20 x 20 µm²	~ 130	40
miniCACTUS	monolithic	150	0.5 x 1 mm²	~ 90	0.15 – 0.3
MonPicoAD	monolithic	130 SiGe	25 x 25 µm²	~ 36	40
Monolith	LGAD monolithic	130 SiGe	25 x 25 µm²	~ 25	40

FIG. 5. Summary of silicon technologies and parameters

One can see that hybrid solution give good timing resolution with reasonable power consumption. Monolithic sensors can have very good timing resolution using SiGe technology but at the cost of high power consumption. The miniCACTUS has the lowest power density consumption and actually reached 65 ps in a later test making it a promising candidate. We are proposing a novel processing to further improve the miniCACTUS timing resolution.

2. Implementation of gain layer

In order to improve the timing performance of DMAPS, we plan to investigate adding a charge carrier multiplication layer to the sensors, in a sense combining the principle of LGADs with the architecture of a DMAPS. The motivation

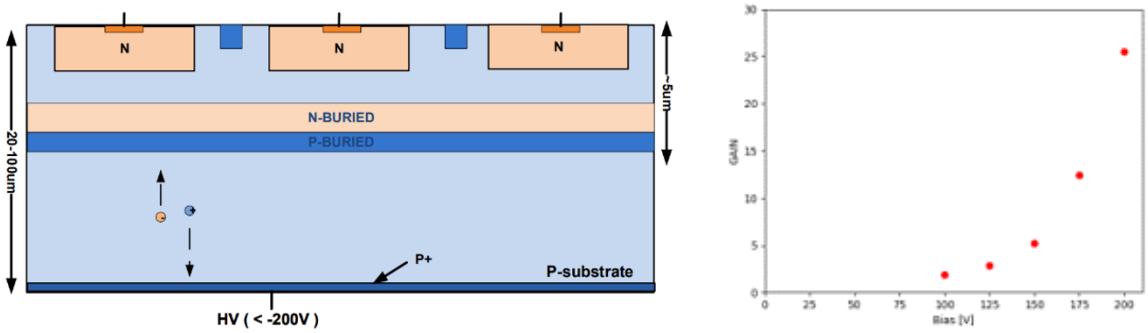

FIG. 6. Cross-section of a DMAPS sensors with a signal gain layer (left) and an initial TCAD simulation of signal gain as a function of bias

to do that is to increase the signal-to-noise ratio, which is a crucial contribution to the overall timing resolution of the sensor. A possible way to do that would be to integrate this layer directly in the technology design. The performance of such post processed sensors, with a layer of carrier amplification, will be evaluated using the same equipment and test procedures as for non-amplified sensors, with which we have long lasting expertise. The potential advantages of this technology are its low cost, its potential ease of operation, and the possibility to easily produce large surfaces of sensors (several hundreds of square meters for future high energy physics projects). Adding an optional charge multiplication layer directly below the very deep N-well improving the Signal to Noise Ratio will be investigated. This scheme allows for very high active detection area (fill factors close to 100%) and complex in-pixel electronics at the same time, with very fast charge collection times. This would be a significant improvement in comparison to state-of-the-art sensors like SPAD, APD and PIN sensors. A possible way to add the gain layer is to use a high-energy implant below the collecting electrodes. Since the SNR is crucial to get the best time resolution from the sensor, the idea here is to increase the signal height without increasing electronics readout noise. This can be done by adding a gain layer as part of the structure of the pixel. This is shown in Figure 2. The basic concept is very similar to LGADs, except that the sensor is not produced using a specially tuned process with the amplifier layer built in, but the amplifying layer is added on top of a standard industry process. Preliminary TCAD simulations show that a gain of 10 for a sensor bias of 200 V is possible. Such a gain is comparable to what is obtained with LGADs. In practice, the implantation of the gain layer will be done at the post-processing stage (thinning, backside ion implant, annealing) of the wafers. Some identified companies having the expertise to do wafer post-processing have the adequate (high energy) ion implant material to introduce the adequately doped layer on already produced sensors : the company that did the post-processing operations on the MiniCactus sensors (Ion Beam Services, `https://www.ion-beam-services.com/`, located in France) has the required knowledge and equipments. The plan is to go through this company for the implementation of the gain layer. Existing wafers including the MiniCactus design, that has already been thoroughly characterized, will be used to test the concept of gain layer implementation. The cost of a processing run of three wafers, to be able test different process parameters, can be evaluated to 75 k$, based on past post-processing operations that we have done successfully.

III. DELIVERABLES

We are proposing to use an existing mini-CACTUS prototype (designed by Irfu) to test the creation of a gain layer, do a post processing of the detector with ion implantation. The prototype will be characterized the same way as the MiniCactus, with the same equipment, allowing to compare in detail signal shapes, amplitudes, charge collection and time resolution.

IV. TIMELINE / MILESTONES

Task	Start date	End date	Milestones
Hiring for simulation	October 1st	November 1st 2022	
TCAD Simulation implantation	November 1st 2022	April 1st 2023	Optimized design
Wafer processing	April 1st 2023	May 1st 2023	Prototype ready
Characterization with source and laser	May 1st 2023	June 1st 2023	Signal to Noise, timing resolution
Test in beam	June 1st 2023	July 1st 2023	data for MIP
Data analysis	July 1st 2023	September 31st 2023	timing resolution, amplitude and efficiency for MIP

V. BUDGET

Kyungpook National University	140 K$
CEA Saclay	140 K$
Contract implantation	75 K$
Total	365 K$

A. Detailed budget full funding

Kyungpook National University	Graduate student 12 months	60 K$
Kyungpook National University	Test bench	50 K$
Kyungpook National University	Travel France	30 K$
CEA Saclay	Supplies MiniCactus	55 K$
CEA Saclay	High resolution Scope	25 K$
CEA Saclay	Contractor	30 K$
CEA Saclay	Travel beam test	30K$
Contract implantation	Wafer processing	75 K$
Total		355 K$

55 K$ upplies Minicactus includes 3 wafers and carrier PCB boards

High timing resolution scope is needed for bench test to capture the faster signals from sensors.

Contractor will carry out initial TCAD simulation and work with the graduate student for 3 months so he/she can run simulations later.

Graduate student will take part to simulation and testing of the detector on bench and in beam in France and will setup a copy of the test bench in Kyungpook University to be able to characterize detectors

2 Beam tests at CERN and 1 at Fermilab with 3 staffs will be planned to study response to minimum ionizing for proton, electrons and pion

The implantation of ions in the MAPS will be contracted with a private company for 75 K$

B. Budget in 80% case

Kyungpook National University	Graduate student 12 months	60 K$
CEA Saclay	Supplies MiniCactus	55 K$
CEA Saclay	High resolution Scope	25 K$
CEA Saclay	Contractor	30 K$
CEA Saclay	Travel beam test	30 K$
Contract implantation		75 K$
Total		275 K$

In this scenario travel funds for the student and test bench would be cut, the student would stay in Korea and focus on simulation and analysis of data collected in France.

C. Budget in 60% case

Kyungpook National University	Graduate student 6 months	30 K$
CEA Saclay	Supplies MiniCactus	55 K$
CEA Saclay	High resolution Scope	25 K$
CEA Saclay	Contractor	30 K$
Contract implantation		75 K$
Total		215 K$

In the 60% budget scenario, beam test would be cut which would only give signal to noise and timing resolution with radioactive source and laser. A request for a beam test to measure timing resolution for MIP particles would very likely be requested the following year to fully characterize the prototype.

VI. MANPOWER

The graduate student will be based in Kyungpook National University and supervised by the CoPI Pr. Hyon-Suk Jo. If funding allows, the student will be sent to France to participate with simulation work and testing of the prototype on the bench and in beam. He/she would also set up a test bench at Kyungpook National University to speed up testing of the prototype devices from each wafers. The student would be supervised by the PI when in France.

The CEA Saclay contractor will be based in Saclay and hired for 3 months to conduct the preliminary simulation. If proposal is approved we will seek additional funding to possibly turn this position in a one or two year postdoc which would be ideal to retain expertise, but we estimated that a 3 months contract will be sufficient in any case to carry out the required simulation work. The contractor or postdoc will be supervised by the PI.

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