Continued Development and Evaluation of a Low-Power High-Density High Timing Precision Readout ASIC for AC-LGADs (HPSoC)

25 July 2022

Bruce Schumm[1], Abraham Seiden, Hartmut Sadrozinski, Simone Mazza, Jennifer Ott, Taylor Shin, Forest Martinez-McKinney, Max Wilder
(University of California, Santa Cruz; Santa Cruz Institute for Particle Physics)

Luca Macchiarulo[2], Greg Uehara, John Stahoviak, Christopher Chock
(Nalu Scientific LLC)

Abstract

The HPSoC (High Timing Precision System on Chip) is a multi-channel waveform digitizing and processing ASIC being developed to read out ultra-fast, high-density sensor arrays such as AC-LGADs. The chip will ultimately be able to service up to ~100 channels, operate with 10 GSa/s waveform digitization, and use autonomous triggering, feature extraction and multichannel data fusion while providing timing precision <10 ps. To date, we have developed the chip architecture design, and have designed, fabricated and tested a four-channel prototype "chiplet" with the goal of optimizing and validating the front-end components on the chip. Funding is sought to continue development and testing of the HPSoC, both in isolation as well as in combination with EIC-specific AC-LGAD sensor prototype(s). The compelling need for high-timing precision subdetectors to fully leverage the EIC machine and optimize physics sensitivity is discussed in detail in the EIC Yellow Report. AC-LGAD based subdetectors are included in each of the ECCE, ATHENA and CORE detector designs, and would also likely be part of the design of any second EIC detector.

[1] Contact PI: baschumm@ucsc.edu
[2] Contact PI: luca@naluscientific.com

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1. Introduction, Motivation

Over the past several years, the introduction of Low Gain Avalanche detectors (LGADs) [1] photodetectors with low pitch and very high timing accuracy has enabled high-density designs for high energy and nuclear physics detectors offering excellent spatial and timing precision, including the EIC. Their use, however, is currently limited by the capabilities of existing readout electronics. Time-to-Digital Converter (TDC) and time-over-threshold solutions permit only an indirect estimate of integrated charge, cannot easily provide sub-pixel spatial resolution or correct for pile-up, sensor aging, radiation and other environmental effects, and suffer from a variety of effects contributing to timing imprecision such as e.g. timewalk, baseline wander, and waveform shape variations.

In order to address the limitations of time-based approaches such as TDCs, Nalu Scientific has designed a compact 1.0x1.3mm^2 low-power readout ASIC, the High Timing Precision System on Chip (HPSoC), that implements full waveform digitization, programmable feature extraction and data fusion capabilities based on our previous experience with such readout chips [2, 3, 4]. To date, an initial four-channel HPSoC prototype “chiplet” has been designed and fabricated to examine the relative performance of several analog front-end variants; it is currently being tested. Support is requested here to design, fabricate and evaluate a new four-channel prototype chip implementing (a) an optimized front-end design informed by the initial prototype chiplet testing results, (b) a full digitizer and (c) capable of autonomous self-triggering, along with a test board(s) which will interface the chip with EIC-specific prototype LGADs sensor(s). The project goal in FY23 is to fabricate and test this chip. Subsequent to that, we plan to continue development of the HPSoC with a nine-channel 3x3 “mini-HPSoC” chip and then the full HPSoC, a 3x3 array of mini-HPSoC chips leading to a total of 3^4 = 81 channels for the full chip. Evaluation of performance for EIC TOF systems for each of these HPSoC development stages is planned.

The target specifications of the fully developed HPSoC ASIC which is expected following the overall multi-year development process are given in Table 1, below. This is followed by a brief overview of the envisioned full chip architecture and testing results from the initial prototype chiplet which has been fabricated. Following that, we present our proposed FY23 objectives, along with a plan of work and the respective responsibilities of both institutional proponents. We subsequently briefly discuss participating personnel, including each institutional proponent’s efforts in advancing diversity, equity, and inclusion, and the areas of responsibility of each person for whom support is sought. We conclude with effort and funding tables summarizing the proposed overall FY23 project.

1.1. LGADs based detectors at EIC

The EIC has a rich scientific program whose possible physics reach has been surveyed and summarized in the EIC Yellow Report [5], where LGADs based detectors were singled out as a technology of choice for far forward Roman Pots and Time of Flight (TOF) detectors. The spatial and timing precision possible with LGAD-based detectors directly correlates with fundamental detector properties such as e.g. charged particle identification performance. There is a critical need for a readout which can both meet the stringent limits on size and power for

readout of the high-density LGAD arrays typical in large NP/HEP detectors while providing the ps-level timing precision required to fully leverage the capabilities of the sensor.

Existing EIC LGADs detector and generic R&D (eRD) efforts are on-going and one of the proponents here (UCSC) has been an ongoing participant in those efforts. Nalu Scientific has joined this effort more recently but has already been substantively participating in EIC for the past few years with the University of Hawai'i in the design and development of the baseline readout chip (HDSoC) for the hpDIRC.

Parameter	**Specification**
Channel no.	Prototype chip (this proposal): 4 Full chip (post FY23): ~100+ (pitch ~300µm)
Process	65nm CMOS
Sample rate	10 GSa/s
Bandwidth	2 GHz
No. bits	10
Supply Voltage	1.0V (2.5V for digital I/O)
Timing accuracy	5 ps
Front-End stage	Embedded TIA
Buffer length/channel	256 samples
Power/channel	<2mW
On-chip integration	Prototype chip (this proposal): Sampling, Digitization Full chip (post FY23) adds: Calibration, Feature Extraction, Data Fusion, Streaming

Table 1. Target HPSoC specifications.

2. HPSoC Architecture Design and Current Status

Channel Architecture: The overall structure of the HPSoC channel design is composed of three partitions, as shown in Figure 1. The main purpose of the current HPSoC chiplet was to examine several front-end variants and the funding requested here would allow design, fabrication and testing of an enhanced four-channel prototype chip including a front-end down-selected from among the variants studied with the current chiplet and additionally including digitization and autonomous triggering.

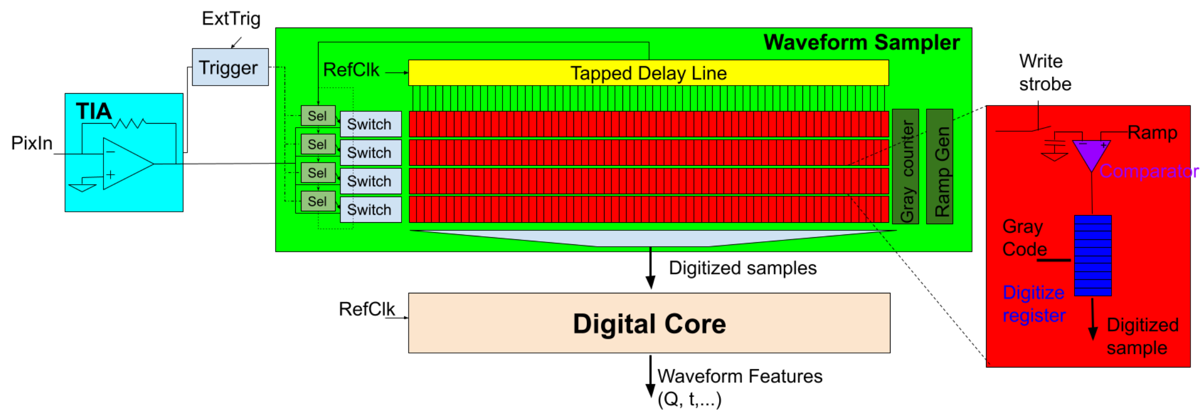

Figure 1. Overall channel architecture for the HPSoC chip, from left to right: transimpedance amplifier (TIA, blue), waveform sampler (green), and the digital partition (red).

Front-end amplifier: The front end interface of each channel has been designed to satisfy the requirements of low power, adequate transimpedance gain to produce measurable voltage pulses, and capability of capacitive drive consistent with the load of the sampling array and signal to noise ratio targets. In simulation, the TIA preserves the edge of an input current signal with ~200 ps rise time and a load of up to 2 pF, which is consistent with expected sensor specifications.

Waveform Sampler: This component will perform data sampling, analog storage, digitization and readout. It consists of a switched-capacitor array in which many samples can be converted to digital format in parallel. A hardwired mechanism is used to coordinate between (continuous) sampling and (on-demand) digitization, permitting simultaneous operation. Digitization will be able to be self-triggered via internal discriminator for autonomous operation.

Digital partition: The digital partition will handle the readout of the digitized signal, together with calibration and feature extraction. For every triggered acquisition, the feature extraction module will identify the number of individual hits occurring on the pixel and the precise time and charge deposited. Feature extracted data will consist of time of arrival and charge estimates.

All three components have been designed to permit area and power estimation and the layouts are shown in Figure 2, where the size of the digital component fits the long channel profile. This permits the layout of the complete channel tile within a small elongated area as a basic building block of the full system.

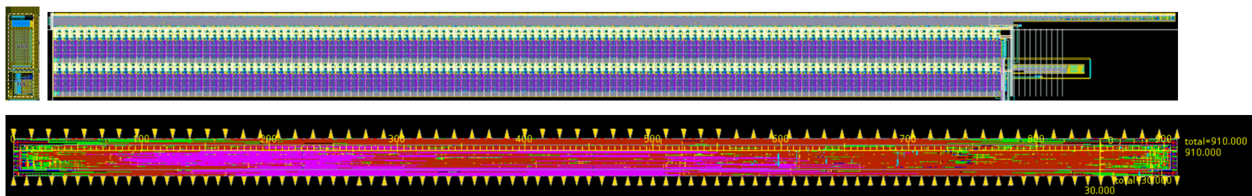

Figure 2. (Top) Front end amplifier and channel layout - approximate size: 900um x 80um for 256 samples. (Bottom) Fully placed and routed channel control - dimensions are 900x30um^2, including power rails.

Full chip architecture and floorplanning (Figure 3): The HPSoC will be modularly built as an array of channels, or "tiles", each capable of independently gathering data from the corresponding pixel. Each channel/tile will perform the operations detailed above and convert the signals from the sensor into timing and amplitude (charge). In the example in Figure 3, the four "hit" tiles respond with charge/timing pairs that encode the information of the hit. The time and charge information is then transferred to a data concentrator that can perform data fusion between neighboring channels to calculate an accurate estimation of the arrival position with sub-pixel accuracy and a sub-sampling time estimate of the event arrival.

The design of the digital and analog channel will permit the layout of the tile within a small area that can be further arranged in groups of nine pixels in a square configuration (a "super-tile"), as shown in Figure 4 (left). Using this concept, a possible floorplanning for a complete chip is shown in Figure 4 (right), where it can be seen that a final die of only 3x3 mm^2 could allow readout of a 9x9 array of pixels at ~350μm pitch or less. This takes into account the space which will be needed for common mixed signal logic (timing generation, in yellow in Figure 4, right), that we estimate is sufficient for the back-end logic to perform the data fusion operation.

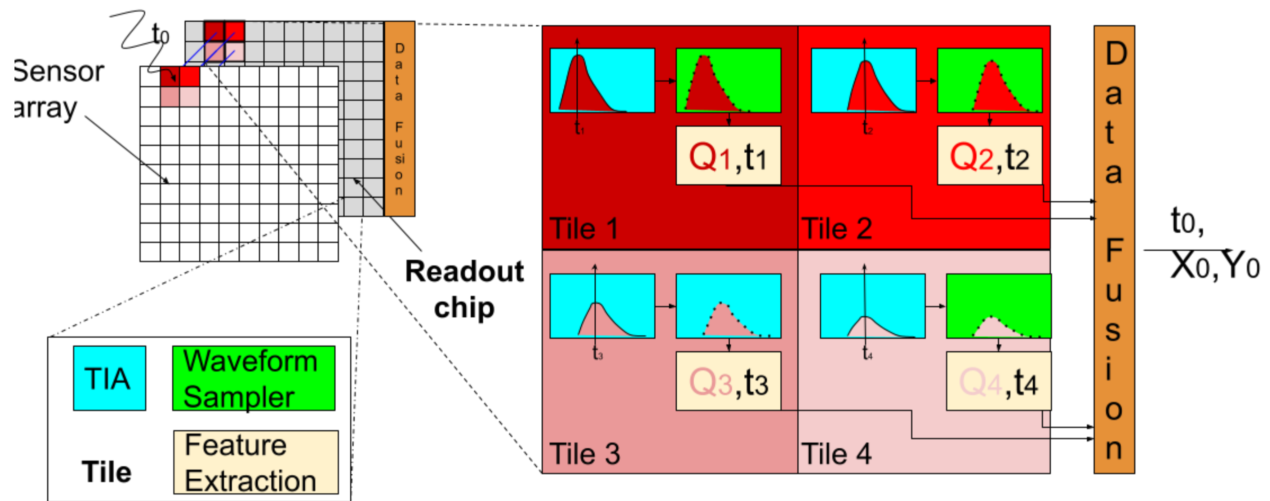

Figure 3. Conceptual operation of HPSoC-based sensor array readout.

2.1. Prototype HPSoC chiplet

In order to validate the HPSoC architecture design, a subset of the required components has been fabricated in a small 1.5x1.0 mm^2 chiplet, shown in Figure 5 (left), which contains:

- Four TIAs, with and without an extra gain stage;
- Four separate readout channels, with three different sampling cells and direct connection to the input to separately validate channel performance; and
- One channel connected to a TIA+gain stage to validate the overall signal chain from sensor output to digitized waveform.

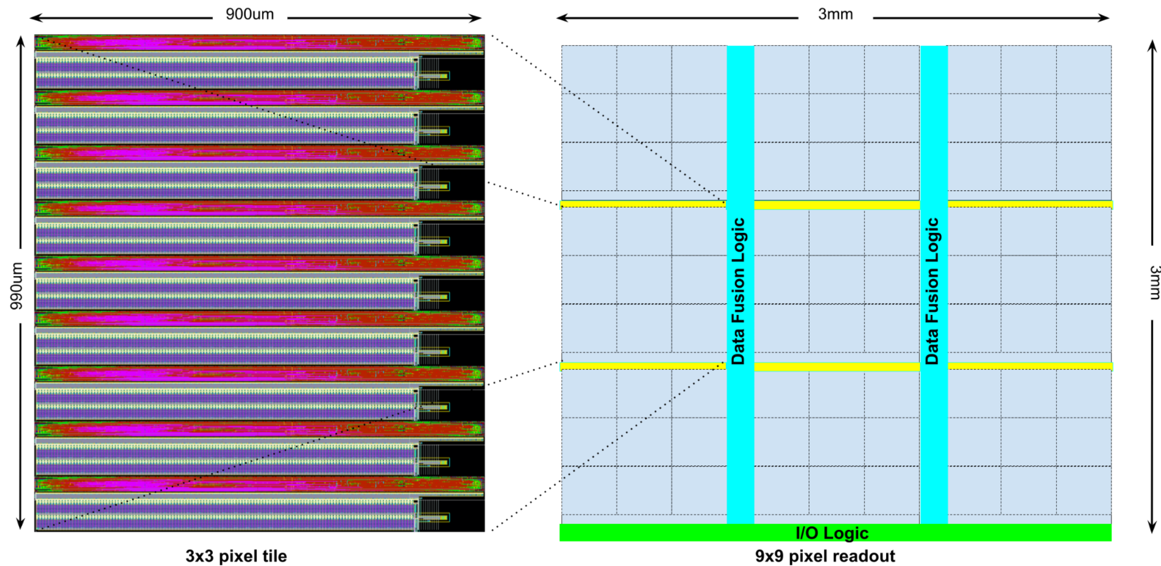

Figure 4. "Super-tile" floorplanning for 9 input channels, and conceptual floorplanning for a 9x9 channel HPSoC.

Figure 5 (right) shows the chiplet test board; in the figure, the large yellow rectangular space is a fixture for incorporation of various sensor array configurations, the small square at the right of the rectangle is the housing of the fabricated die, and the components at the bottom permit calibration testing. Figure 6 shows close-ups of (left) a wire-bonded die connected to the calibration traces rather than a sensor, and (right) a chiplet wire bonded to an AC-LGAD sensor (here, FBK - RSD1 production 500um pitch, 200um pads). Test results to date, both with calibration inputs and connected to an AC-LGAD sensor, are presented below.

2.2. Prototype HPSoC chip test results

The chiplet has been tested using both calibration inputs as well as with an AC-LGAD sensor. The sensor used was a 3x3 array FBK AC-LGAD [LGAD-Test] from RSD1 production 3x3, 500 um pitch, 200 um pads. This was connected to the 4 chiplet inputs using 3 sensor pads in a row to 3 chiplet inputs, N+ connection to input, GR + other pads to ground. A Sr90 source aligned with back of the sensor was used for testing, however, the low <1Hz data-taking rate limited the size of the collected dataset, which amounted to ~150 events on one channel and ~40 events on a second channel, and further testing with a IR laser is planned. Analogous sensor testing results were obtained from both channels. Only two of the chip channels produced usable data; issues in bonding with the other two channels precluded data-taking with them. The calibration dataset, which is for all four channels, was generated by feeding a voltage signal with a fast rise time (300ps 20-80%) from a function generator to an input network consisting of a termination resistance and a series small capacitor (0.1pF) into the chip input.

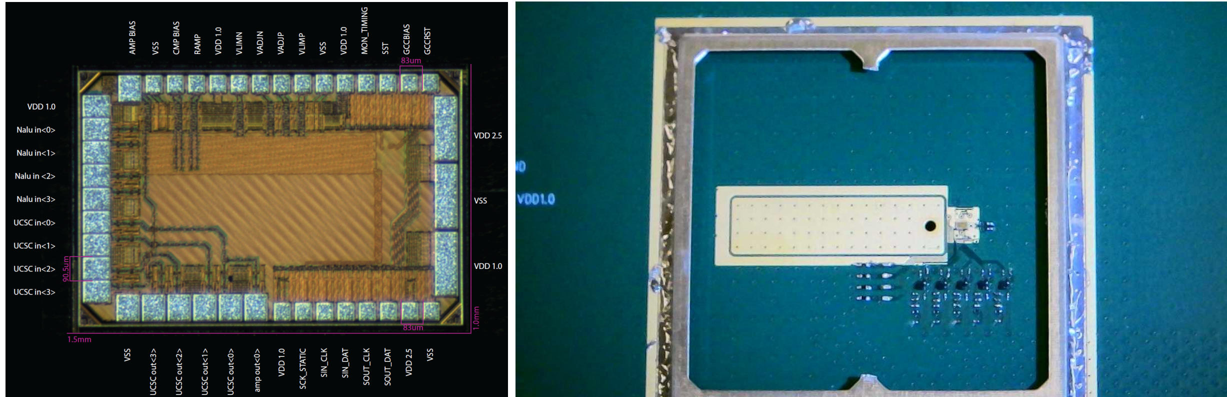

Figure 5. (left) Micrograph of fabricated HPSoC prototype chip; (right) chiplet test board, the large yellow rectangular space is the fixture for incorporation of various sensor array configurations, the small square at the right of the rectangle is the housing of the fabricated die, the components at the bottom permit calibration testing.

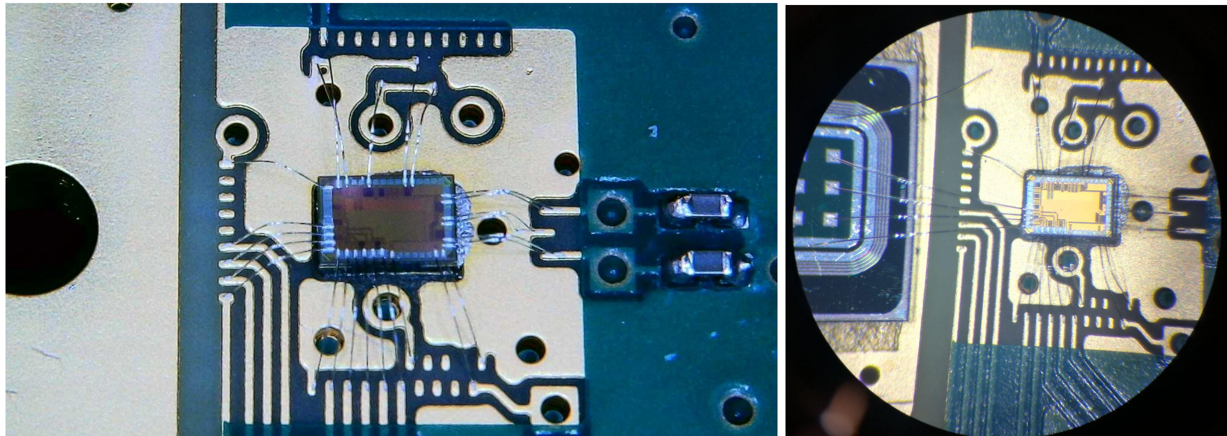

Figure 6. (left) Close-up of a mounted chiplet showing the wire bonded die connected to the calibration traces on the test board, it is used without a sensor array; (right) Chiplet wire bonded to an AC-LGAD sensor (here, FBK - RSD1 production 500um pitch, 200um pads).

Using calibration inputs at different levels, we performed linearity measurements as shown in Figure 7. As shown in the left sub-figure, output relative to the input step is reasonably linear with a slope ~0.1, for channels 1,2,3. When a full model of the input stage is considered, this translates into a transimpedance gain of ~1.4Kohm, as expected from our simulations. Channel 0 is followed in the chip by a voltage gain stage, and the lower response of channel 0 relative to the other channels is expected, as it arises from the added loaded capacitance associated with the output of the stage. An analogous measurement performed on the cascade of TIA+extra gain stage is compared with the pure TIA output in Figure 7 (right), which shows the linearity of the response as well as an effective gain increase by more than a factor of 4.

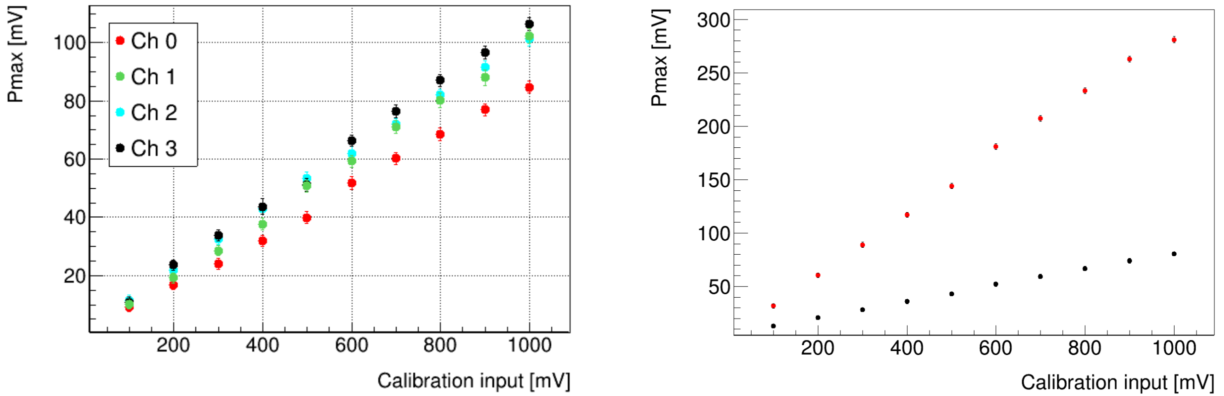

Figure 7. (left) TIA gain measurement. Comparisons of TIA and TIA+VGS on the same input channel - effect of gain stage.

Sideband data from the calibration dataset was used to estimate the noise from the amplifier stage. Figure 8 (left) shows an example of noise measurements corresponding to different impulse levels. The mean values are reproducible and independent of the input, as expected for a pure amplifier noise (as opposed to other types of crosstalk or feedthrough). The RMS value, around 2.6mV, should have the value obtained by measuring the probe and scope by themselves, which is approximately 1.7mV, subtracted in quadrature. This yields a noise level of ~1.7mV, which is higher than expected from simulations but, as will be discussed, below, still allows for timing precision well within the performance specifications of the EIC TOF system. The rise time (20-80%) of the output signal was evaluated at different input levels (Figure 8, right) and is largely independent of input level at ~500-600 ps, consistent with simulation.

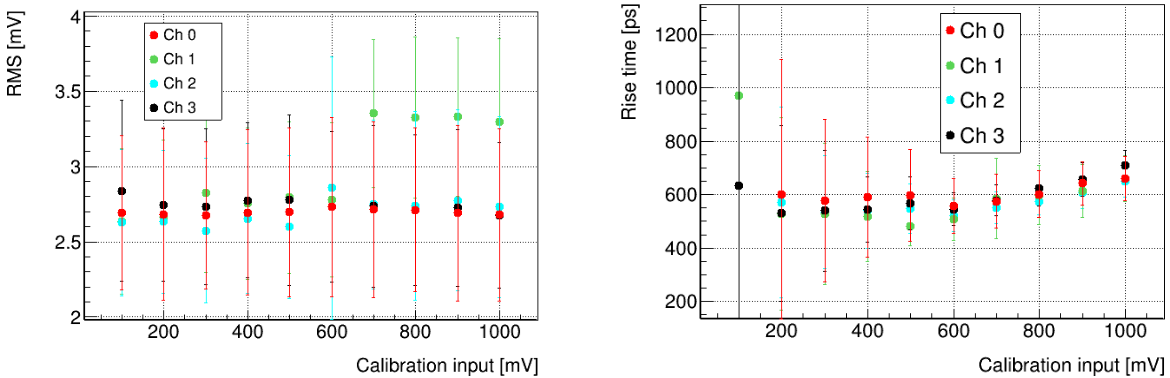

Figure 8. Calibration dataset measurements of (left) TIA noise, and (right) TIA rise time.

Figure 9 (left) shows a typical waveform with a reasonably high voltage peak ~60 mV over baseline acquired using the Sr90 source to excite a minimum-ionizing signal in an FBK AC-LGAD sensor. This would already be sufficient for the HPSoC to identify the deposition and provide precise timing even without the help of a gain stage which can increase the gain by a factor of ~4-5. However, such a gain stage will likely be a necessity for smaller pitch sensors. Figure 9 (right) shows the distribution of voltage peak amplitudes for the smaller of the two Sr90

datasets. Figure 10 (left) shows the distribution of rise times from the “large” Sr90 dataset with a mean of ~540 ps, which is consistent with the expected response of the sensor used. Estimating the time jitter using the ratio between the RMS of the noise and the slope of the rising edge (slew rate), we found a resolution of 1.7mV/(74/546 mV/ps) or ~12.5ps, which is quite encouraging and in line with estimates from simulation for a full input capacitance of 0.4pF.

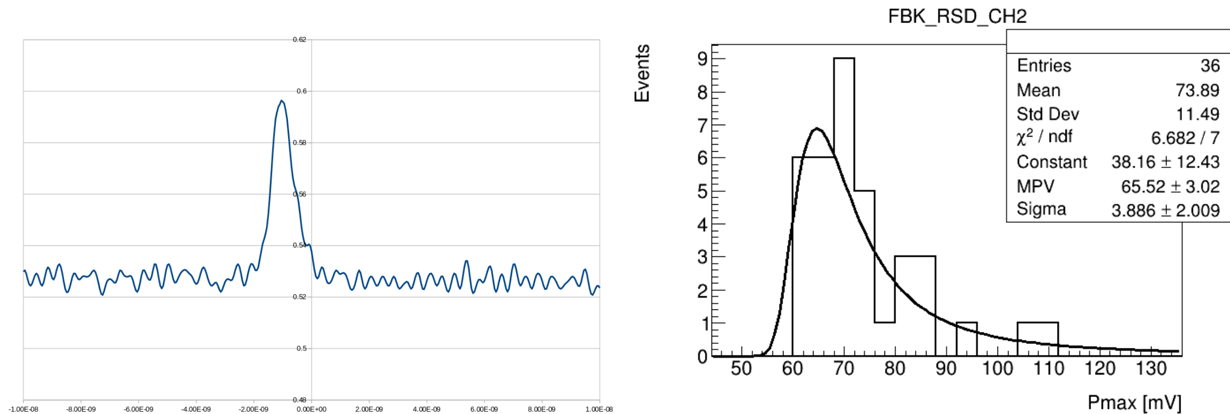

Figure 9. (left) Typical TIA output response (rise time ~540ps); (right) Sr90 AC-LGAD “small” dataset distribution of peak waveform amplitudes.

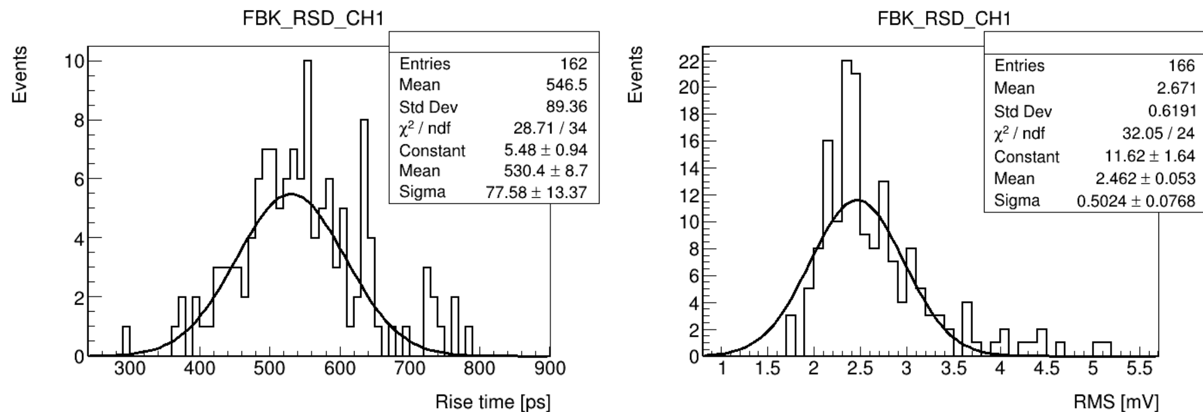

Figure 10. Sr90 AC-LGAD “large” waveform dataset distributions: (left) rise time (~540ps); (right) sideband noise.

2.3. Current HPSoC status

HPSoC design and development was initiated under a DOE-HEP SBIR Phase I award. As discussed in detail below, support is requested here to continue HPSoC development and perform testing of the next iteration of the HPSoC chip using EIC-specific prototype sensors. The main findings and results of the Phase I DOE-HEP project were:

- **Architecture exploration:** a feasible HPSoC architecture, described above, was defined based on the target specifications**.**

- **Process exploration:** completing design of full analog, mixed signal and digital submodules in 65nm proved the process sufficient for both analog and digital performance.
- **Feasibility and achievable pitch:** it was found that area tiling permits an achievable pitch down to <~300 um.
- **Performance evaluation of front end:** using simulations after post-layout parasitic extraction of a selected design for TIA and gain stage, a gain stage capable of reaching the agreed-upon SNR necessary to achieve the desired timing performance for the whole system (<10ps) was designed. Using the output of a TIA stage, and estimating time jitter as the ratio between the RMS of the noise and the slope of the rising edge we obtain an estimated resolution of ~12.5ps, which is in line with estimates from simulation for a full input capacitance of 0.4pF.
- **Performance evaluation of mixed signal:** simulation taking into account device variability has shown the feasibility of a waveform sampling within the desired resolution. It is expected that up to 4 individual groups of 64 samples can be operated in parallel, providing sufficient depth for deadtime-free operation at a maximum rate of ~1 MHz rate per pixel.
- **Preliminary design of digital channel component and architectural design of back end:** a full implementation of the channel digital component was completed and shown to fit within the area required to reach the pitch target. The digital component performs signal calibrations and simple feature extraction. The back end digital design to perform data gathering and fusion has also been analyzed and is expected to fit within the overall available area.

3. Objectives; institutional areas of responsibility

The overall goal of the multi-year HPSoC project is to design and fabricate a readout chip meeting the specifications given in Table 1, above, and which has been synergistically developed and optimized for use with EIC-specific sensors. The more immediate FY23 goal for which support is sought is to design, fabricate, test and evaluate a second iteration of the four-channel prototype HPSoC chip additionally implementing (a) an optimized front-end design informed by the initial prototype chiplet testing results, (b) a full digitizer and (c) capable of autonomous self-triggering, along with (d) design and fabrication of an evaluation test board(s) which will interface the chip with EIC-specific prototype LGADs sensor(s) as well as calibration signals. The final FY23 goal is to fully test the new chip integrated with EIC-specific sensor(s) on both the bench and, assuming availability, with beam testing.

Nalu Scientific will be primarily responsible for all chip and board design as well as chip fabrication, including, in particular:

- Based on a down-select among the four different front variants in the initial prototype chiplet, design a front-end for the second iteration of the HPSoC prototype optimized for use with EIC-specific sensor(s);
- Design a simple digitizer stage for use with the prototype based on the already-accomplished preliminary design of the digital channel component and additionally leveraging existing Nalu designs;

- Add on-chip capability for self-triggering based on modification of existing Nalu designs;
- Fabricate the second prototype chip iteration;
- Participate in the design of the evaluation test board to accommodate the second prototype chip's use in both calibration input and sensor-based testing;
- Design and implementation of all firmware.

UCSC/SCIPP will be responsible for sensor selection/mounting and testing, including, in particular:

- Guidance on the design of the second iteration of the HPSoC prototype chip as it relates to its application to the Electron-Ion-Collider detector Time-of-Flight system;
- Participate in the design of the evaluation test board to accommodate use with EIC-specific sensor(s);
- Loading and verification of the modified evaluation test board;
- Characterization of the new HPSoC prototype chip using calibration and sensor data collected through both bench and beam testing, including
    - Confirmation of basic functionality,
    - Analog gain and noise performance,
    - Analog dynamic range studies,
    - Assessment of the performance of the initial on-board digitization feature, as it relates to gain, noise and dynamic range,
    - Analysis of characterization data as it relates to physics performance.

3.1. Work plan

The work plan for FY23 will allow achieving the objectives outlined above to design, fabricate, test and evaluate a second iteration of the four-channel prototype HPSoC chip with EIC-specific prototype LGADs sensor(s). ***Many elements in the WBS below will inherit from the existing HPSoC effort, however, each will be reviewed to verify whether any changes and/or modifications are needed in order to best support the addition of the new/enhanced functionality which is the focus of this request.***

WBS 1. Design of the second iteration of the prototype chip: Based on a down-select among the four different front variants in the initial prototype chiplet, an optimized four-channel front-end will be designed and implemented. The following additional elements will be designed for the new prototype chip iteration:

- A simple digitizer stage for use with the prototype based on existing Nalu design(s);
- On-chip self-triggering based on existing Nalu design(s);

The existing mixed signal architecture design will be modified to accommodate the self-triggering scheme. These elements will be added to the existing design and validated using the existing chip simulation updated for the new elements above. The current design choices for the following will be reviewed and validated, with modification as needed to accommodate the additional new features in the second prototype chip:

- Timing generation and distribution: minimization of timing skew and jitter
- Sampling cell design: reduction of sampling errors and leakage

- Digitization components design: ramp, fast counter design, compaction of digitize register
- Full channel structure evaluation.

Only the minimal digital components required to control the analog channel will be incorporated, including:

- Single channel control: overall slow control for settable parameters, operation modes and management of self-triggering
- External Interface design: data packetization and serialization
- In the interests of economy, single channel data flow and extraction, i.e. simple DSP features and feature extraction which would typically be implemented on-chip, is proposed to be implemented and tested in FPGA:

WBS 2: Integration of test chip, verification and foundry submission

- Test chip definition: Final selection of components and test structures to be submitted. Test Channel assembly, exposed test points and integration with I/O pads
- Functional verification - analog functional model: Analog subsystems in the ASIC are designed and verified with transistor level simulators. Their functions are then represented in chip level simulations with combined structural and HDL (hardware description language) models which are used for whole chip simulations.
- Combined testbench for each chip subsystem: Final simulation verification of the test chip will test the combined analog and digital models' netlists. The simulation is done to ensure proper connections and signal interpretation between the digital and analog domains. This step ensures that each subsystem of the ASIC functions together as intended.
- Full chip layout vs. schematic: The assembly of the test ASIC will require the placement and interconnection of the digital and analog cores' physical layouts and with the IO pads. The entire physical layout will undergo DRC (Design Rules Checking for manufacturability) and LVS (Layout Versus Schematic) to ensure matching of desired netlist structures with silicon devices. DRC and LVS will use commercial tools (such as Cadence PVS) and foundry provided rules files. This phase concludes with tape-out to the IC foundry fabrication facility.

WBS 3: Evaluation PCB test board design, fabrication and chip testing:

- Chip packaging and footprint: After the chip is submitted for fabrication, it is possible to proceed with the choice of package, allowing definition of the chip footprint for the PCB layout. Some fabricated dies will be left unpackaged to allow for direct bonding to LGAD sensors. No substantive changes with respect to what was done with the existing initial prototype chiplet are foreseen.
- Evaluation PCB test board design: The existing board design allows testing of the individual subcomponents of the chip on the analog front end (amplifiers, buffers, digitizer), or on the digital front end (power, timing performance). As needed, the existing board design will be modified to accommodate the new prototype chip and/or EIC-specific prototype sensor(s).

- Front-End testing: Two different types of testing are planned: (a) benchtop testing of the packaged chip will take advantage of the PCB for interfacing with the measurement equipment, and (b) a test of a device(s) coupled with LGADs to probe its effective response to the expected operational environment and input characteristics. The latter test will be performed with a bare die directly bonded to the sensor. Both sets of tests will be performed by the UCSC collaborators and will, if possible, include beam testing in addition to lab bench tests.
- Mixed signal testing: individual components and full channel functionality and performance will be probed.

All results of testing will be reported in the relevant EIC eRD and detector group(s), and we will additionally report results at conference and/or in instrumentation papers and other documents, such as internal notes and programmatic documents i.e. internal reports, TDRs, etc.

WBS 4: **Firmware Design:** Firmware implemented in an FPGA on the evaluation test board will be required to e.g. configure the chip, start/stop sampling, start digitization, export data, clear/reset and repeat. In addition, part of the scope reduction required to meet the 80% baseline request would include moving to FW much of the implementation of autonomous self-triggering planned to be on-chip in the 100% baseline request.

3.2. Personnel, performance schedule; support request, deliverables

The Nalu Scientific team will be led by PI Dr. Luca Macchiarulo, Nalu's Senior IC Designer, with additional effort from other staff members with relevant specialized skills, including Sr. Firmware Designer John Stahoviak, Sr. Design Engineer Dr. Greg Uehara, Integration Engineer Chris Chock, Senior Scientist Dr. Kevin Flood and CEO Dr. Isar Mostafanezhad. (No support is being requested for Drs. Flood and Mostafanezhad.)

The UCSC/SCIPP team will include the PI Prof. Bruce Schumm, recalled faculty Abraham Seiden and Hartmut Sadrozinski, postdoctoral researchers Simone Mazza and Jennifer Ott, and the three technical staff members for whom support is requested here: electro-mechanical technician Forest Martinez-McKinney, and electronic design specialists Max Wilder and Taylor Shin.

Table 2 summarizes the start and duration for completing the major elements of the WBS. Table 3 summarizes the 100% baseline level of effort, the particular scope addressed and the accompanying resource request for each individual seeking support here. The relative apportionment of funding and effort proposed between Nalu and UCSC/SCIPP is ~75%, 25%, respectively.

Beyond personnel, support is additionally sought for fabrication of the new chip prototype ($10k) and the modified evaluation test board plus procurement of parts required for the board ($10k), along with a small amount of M&S for miscellaneous expenses and travel. UCSC indirect costs are 54% of direct costs, Nalu's effective indirect rate is ~40%. All numbers provided in Tables 3 and 4 include fringe and are fully loaded.

Table 2. Objectives and schedule for FY23, by months 1-12 (F=Fabrication).

FY23 Month Objective	1	2	3	4	5	6	7	8	9	10	11	12	Principle Responsible Part(ies)
WBS 1.Update of prototype chip design, addition of new features	X	X	X										Nalu
WBS 2. Integration of test chip, verification and submission			X	XF	F	F							Nalu
WBS 3. Evaluation test board design, fabrication					X	X	X						Nalu, UCSC
WBS 3. Testing, reporting of results							X	X	X	X	X	X	UCSC, Nalu
WBS 4. Firmware design, implementation						X	X						Nalu

Table 3. Level of Effort, Scope Addressed, Resource Request for each person

	100% Baseline		
Team Member, Institution	**FTE months**	**Request ($k)**	**Function, Scope**
Dr. Luca Macchiarulo, Nalu	1.2	30	Principal chip designer, lead PI
Dr. Greg Uehara, Nalu	1.0	25	Design, implement on-chip self-triggering
John Stahoviak, Nalu	0.8	20	Design, implement firmware
Chris Chock, Nalu	1.1	20	PCB board design and implementation; chip layout, integration
Taylor Shin, UCSC	1.5	17	Electronic design specialist; PCB board design and implementation
Max Wilder, UCSC	0.86	10	Electronic design specialist; PCB board design and implementation
Forest Martinez-McKinney	0.4	5	Electro-mechanical technician; PCB board implementation
Total:	5.5	127	

Table 4 provides a line item budget summarizing the total 100% baseline request of 150k in FY23, along with the requested ~80% and ~60% reductions. However, given that a true 40% reduction in the budget would not allow successfully addressing the minimal scope of fabricating and testing any version of a next iteration of the HPSoC chip, a 72% baseline budget is given. Most of the reduction from baseline to 80% is accomplished by moving much of the autonomous self-triggering implementation from on-chip to firmware running on an FPGA on the evaluation test board. This will significantly reduce Dr. Uehara's effort and, to a lesser extent, that of both Mr. Stahoviak and the PI Dr. Macchiarulo. The "60% baseline" budget, which is actually ~72% here, descopes the autonomous trigger and other FPGA functionality to the bare minimum required to acquire and digitize AC-LGAD waveforms with an external trigger.

Table 4. Line item budget

Item	100% Baseline Request ($k)	80% Baseline	"60% Baseline"
Chip fabrication	10	10	10
Board fabrication, parts	10	10	10
Nalu personnel	95	76	65
UCSC personnel	32	26	23
M&S, travel (trvl only at 100%)	3	1	1
Total:	150	123	109

The main deliverable for the FY23 effort will be the second iteration, along with calibration and sensor test results, of the four-channel prototype HPSoC chip, which will implement (a) an optimized front-end design informed by the testing results from the initial prototype chiplet, (b) a full digitizer and (c) on-chip autonomous self-triggering, along with (d) design and fabrication of an evaluation test board(s) based on the existing board design which will interface the chip with EIC-specific prototype LGADs sensor(s) as well as calibration signals. Test results based on the prototype chip will be presented and shared with the relevant EIC AC-LGADs detector and other working groups such as e.g. eRD112. A copy of this proposal has been provided to the eRD112/LGADs conveners[3] for their review and was discussed with one of the conveners, Zhenyu Ye who is fully supportive, prior to submission.

Subsequent to FY23, a nine-channel HPSoC 3x3 "mini-chip" is planned as an intermediate step towards an ultimate 81-channel full chip composed of a 3x3 array of mini-chips, as shown in Figure 11, which could be available in FY25.

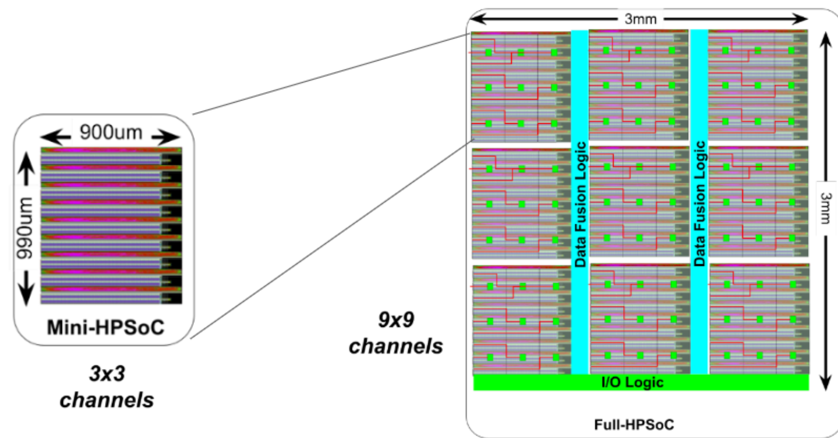

Figure 11. Planned scaling to higher channel count chips in successive HPSoC iterations after FY23.

3.3. Diversity, Equity, and Inclusion

Both Nalu Scientific and UCSC strongly support the goal of advancing diversity, equity and inclusion. UCSC/SCIPP PI Prof. Schumm is the Director of UC Operations for the inter-segmental Cal-Bridge Program (https://www.cpp.edu/calbridge/index.shtml), currently funded at $5M per year by the California Legislature, that mines the diverse talent of the California State University undergraduate student body, bringing competitively-selected students into close mentoring relationships with UC faculty and cultivating them for admission to graduate school. As a result, SCIPP has access to a significant pool of talented graduate students from historically under-represented backgrounds. Two such students (fourth-year Rene Mora Padilla and second-year Miguel Escobar Godoy) are currently active in the Fast Sensors group that will host the UCSC portion of the proposed work, which would provide significant additional opportunity for their education and professional development.

[3] Constantin Loizides <constantin.loizides@cern.ch>, Frank Geurts <geurts@rice.edu>, Wei Li <wl33@rice.edu>, Zhenyu Ye <yezhenyu@uic.edu>

Nalu is currently hosting as a summer intern a University of Hawai'i EE grad student through a DOE-NP SBIR Phase II diversity supplemental grant program designed to foster diversity by engaging students from groups shown to be underrepresented in science and engineering. Nalu's close partnership with the University of Hawai'i since the inception of the company has afforded it similar opportunities in the past and undoubtedly will in the future. Reflecting the State of Hawaii's underlying "majority-minority" demographic make-up, Nalu's workforce has developed naturally over the past several years to reflect its naturally diverse environment. In turn, Nalu has the opportunity to provide high-tech mentoring and professional development to local graduate students participating in UH research groups collaborating with Nalu as well as students from further afield, including both the U.S. and internationally.

3.4. Cost effectiveness

Through its localization of the digitization of fast-timing signals from advanced solid-state detectors onto the primary readout ASIC, the successful development of the HPSoC ASIC will significantly reduce the per-channel cost of digitizing and processing information from fast timing sensors. In addition, the development of an ASIC to replace conventional digitization and communication chipsets will reduce reliance on supply-chain disruptions, placing the production and procurement of critical electronics in much tighter control of the scientists and engineers developing and working with fast timing systems.

[1] H. F. W. Sadrozinski et al., Ultra-fast silicon detectors, NIM-A 730 (2013) 226-231.
[2] L. Macchiarulo et al., "Design improvements and first results for the revision 3 of AARDVARC Waveform Sampling System On Chip," IEEE NSS-MIC 2021, Virtual Presentation (Oct 2021).
[3] L. Macchiarulo et al, "Design and Measurement Results for the High Density Digitizer System on Chip (HDSoC): A 64 Channel 1 GSa/s Waveform Digitizer for High Density Detectors", IEEE NSS 2020 (Nov 2020).
[4] M. Mishra et al., "Application of High Density Digitizer System-on-Chip (HDSoC) prototype for acquiring fast silicon photomultiplier signals", accepted by IEEE NSS 2022 (Nov 2022).
[5] R. A. Khalek et al. "Science requirements and detector concepts for the electron-ion collider: EIC yellow report." arXiv:2103.05419 (2021).