Large-Area Monolithic Active Pixel Sensors Combining High Spatial and Temporal Resolution

EIC Generic R&D for FY24

Dominik Górni[1,*], Elke Aschenauer[2], Gabriella A. Carini[1], Grzegorz W. Deptuch[1], Soumyajit Mandal[1], and Giovanni Pinaroli[1]

EIC Silicon Consortium

[1]Brookhaven National Laboratory, Instrumentation Division
[2]Brookhaven National Laboratory, Electron-Ion Collider Directorate
[*]Contact Person, dgorni@bnl.gov

July 14, 2023

Abstract

This document proposes development of Monolithic Active Pixels Sensors, targeting high spatial resolution, on the order of that offered by ALICE - ITS3 sensors, but yielding simultaneously sub-microsecond timing resolution in response to the call for generic R&D proposal for the EIC. The follow-up on the results of this proposal will the future development of a complete circuit solution, aiming at the Large Area Sensors for the EIC tracking and vertexing layers with emphasis on the outer, sagitta layers and the disks in the hadron and electron directions. The current plan for the ePIC SVT layers is to directly employ the ALICE-ITS3 sensors for the innermost barrel layers, whereas the sagitta layers and end-cap wheels are to be conceptually evolved from the mentioned ALICE-ITS3 sensors, despite the fact that their properties are not fully satisfactory for the ePIC SVT detector. The baseline solution for the EIC specific sensors to be forked off the ALICE-ITS3 sensors endorses only minimal changes to the sensors design due to, primarily, the risk of undertaking a completely new design in the light of the need of delivering operational sensors in the restricted timeline for the construction of the EIC and its detectors. This proposal brings an idea of developing entirely new Repeated Sensors Units, capable of delivering simultaneously high spatial and temporal resolution at low power consumption for the upgrades of the EIC vertex and tracking layers that can be used to substitute the original Repeated Sensors Units in the ALICE - ITS3 sensors. The Repeated Sensors Unite constitutes the basic building block of the ALICE-ITS3 sensors and is operatively connected to the frame of a sensors slab made of the stitched reticles. The outcome of the R&D efforts will be results of the analysis of the feasibility of the idea for substitutive arrangements of the new Repeated Sensors Units in the ALICE-ITS3 design and an early stage of the design of the new Repeated Sensors Units in the TPSCo 65 nm process. The proposed work is entailed by the R&D, focused on event-driven readout architectures and optimized front-ends.

Contents

1 EIC Vertex & Tracking Detectors Considerations - Introduction

1.1 Synopsis of the R&D Proposal

The requirements for an EIC detector as ePIC are hermeticity and a large rapidity $\eta \in (-4, 4)$ coverage, as well as excellent momentum resolution are required for reconstructing event kinematics, for jet reconstruction, jet correlations, and jet substructure studies, and others [1]. The requirements on the vertex resolution are driven by the heavy flavor reconstruction, where the reduction of the background relies strongly on analyzes-related selections performed in different combinations of the primary scattering vertex and the secondary vertex of the decaying heavy meson. All these requirements are currently possible to be fulfilled only by a tracker system utilizing highly granular, lightweight and capable of providing sub-microsecond timing resolution detectors. Best, even the timing resolution on the order of $\sim 100\,\text{ns}$ would be advantageous.

The EIC background overlaid on the physics is dominated by electron and hadron beam gas scattering in the electron and hadron direction, respectively, electrons curling in the magnetic field, and X-rays generated by electrons in the bremsstrahlung process. This translates to the requirement the timing resolution being equally important as the spatial resolution and the total material budget of the vertex and tracking layers organized in a form of the barrel layers and of the hadron and electron direction disks. The vertex and tracking system with the Electromagnetic Calorimeter (EmCal) and Particle Identification (PID) form the central part of the detector. This part plays a crucial role in exploiting the Deep-Inelastic Scattering (DIC) process, which is the basic process at the EIC, because of its unmatched precision in studying the inner structure of nuclear matter.

The total material budget located before the PWO-like EmCal and the PID detector such as Detector of Internally Reflected Cherenkov Light (DIRC) represent important challenges. On the one hand, it is desired, by the PID, to have better than 1 mrad angular resolution into the PID subsystems. On the other hand, assuring the 5% electrons efficiency loss, the tolerable amount of material in front for the high resolution EmCal is only $\sim 5\%$ of the radiation length X_0 assuming certain distance of the material from the interaction point and the reconstruction method. The DIRC, in particular, appears to expect 0.5 mrad of the angular resolution or even better. In part the resolution is assured by the granularity of the detector, but from multiple scattering arguments, in the interesting for the physics, sub $\sim 5\,\text{GeV}$ momentum range, such a resolution level is hard to achieve with inactive material directly in front of the PID, unless that inactive material is pushed down into the total not exceeding a few percent percent level of X_0. Even if the latter is achieved, a significant problem of production of X-rays, resulting from the bremsstrahlung process, needs to be addressed. On the one hand, it can be handled by using extremely thin detector layers and using such detectors that can provide improved timing resolution to improve full reconstruction of the event with high suppression of the background. But this can be not enough, and further reduction of the material may be needed. Here the best target is seeking alternatives for any high-Z elements that even if present is small quantities may add to the percentage of X_0. A significant gain, assuming that the vertex and tracking detector layers are made of Silicon sensor slabs that are either self-supporting or laid out on a lightweight Carbon Fiber (CF) frame can be expected should delivery of resources, i.e., power supplies, biases, down- and up- links for data transfer, are realized in an optimal way. These resources are typically driven-in using variants of Copper cables. Most dominantly, flex substrates with Cu traces are used. Therefore, serial powering, proposed for the ePIC SVT detector, offers the first step towards the desired improvement in having less material in which electrons can generate X-rays. The next step would be to explore elimination of the Cu cables by resorting to handling the delivery of resources by light, i.e. through fibers. Fibers represent only negligible addition to the material budget as their diameters are extremely small and their material budget cost is equivalent to that of Si. Optical data and power links carry in and additional positive side effect by establishing Galvanically isolated connections from any chosen detector subsystem to the Data Acquisition (DAQ). Elimination of ground loops and removing the concern of equalizing voltage levels when signals between subsystems are exchanged, and increasing immunity to failures because, unlikely to serial powering, each detector subsystem is light -supplied and -serviced individually.

1.2 Basics of Monolithic Active Pixel Sensors

The material budget and spatial resolution requirements of the EIC program are fulfilled by a silicon based tracker system utilizing the Monolithic Active Pixel Sensors (MAPS) technology [2]. MAPS detectors integrate the sensor matrix and readout circuitry in one piece of silicon, as opposed to the hybrid approach where the sensor matrix and readout circuitry are implemented in two separate silicon pieces. This approach offers advantages in terms of eased detector assembly, thinning as needed, production cost, even when it comes to large sizes of megapixel arrays, individual pixel readout, radiation hardness, while operating at high speed, low power consumption, and operation from a low voltage supply source. The older-generation MAPS, such as those used in the Heavy Flavor Tracker (HFT) at STAR [3] used to be built on low-resistivity substrate, and operate in the analog mode. New inner trackers in Nuclear Physics (NP), such as the Inner Tracker System (ITS1/2 in the past and currently ITS3) for the ALICE experiment on the LHC, managed shifting to the increased resistivity of the Active Sensitive Volume (ASV) with the low detector capacitance [4] [5] and were shown thinned resulting in devices representing only a fraction of a percent of X_0 per layer [6].

There is only one caveat using a MAPS based tracking system. Currently, MAPS operate with a frame accumulation time from 5 to 10 µm [7] at the best. This accumulation time has an immediate negative impact due to the backgrounds on the tracking. To separate background hits from true DIS hits, enough hits from fast detectors are needed to form a "tracklet" with a good pointing resolution. In the ePIC detector, two Micro-Pattern Gas Detector (MPGD) barrel trackers have been added on top of the (AC-coupled Low Gain Avalanche Diode) (AC-LGAD) Time-of Flight (ToF) detector and two MPGD disks in each endcap have also been added. This will provide the additional information needed to efficiently reconstruct the tracks from the DIS event. These additional tracker do not only increase the cost of the detector significantly but, most importantly, reconstruction of the scattered electrons is impaired due to the increased material budget because of the additional trackers and service material. All of these negative impacts can be completely avoided if one has a MAPS-based tracker with a 100 ns or lower frame accumulation time.

1.3 Relation Between the ALICE-ITS3 and New EIC-Postulated MAPS

The design of the ALICE-ITS3 sensors, which are organized in almost 2 cm long slabs stitched along their width, is modular [7]. The sensors consist of the end caps that are used for services, i.e., delivery of power and I/Os, and the inner frame that provides voltage regulation, monitoring of internal functions, and transmission of data to the end caps within which the Repeated Stitched Units (RSU) are embedded. Such a scheme allows rotations of the original RSU by new blocks, assuming that pin-outs of such new blocks are compatible with the required electrical hook-ups of the inner frame. This opportunity is proposed by this proposal to be explored to offer a MAPS detector with new capabilities but at the minimized, economically and timeline-aware development efforts. The strong side of the proposal consist in the development of the MAPS, combining high spatial and temporal resolution carried out in the direction of an unit that can be pin-to-pin compatible with the ALICE ITS3 proposed RSU. The new RSU will feed the peripheral part of the ALICE-ITS3 sensors with the data but the pixels in the new RSU will be read out in the driven event-driven manner in contrast to the original frame-driven way. Looking in more detail in the concept of the ALICE-ITS3 sensors, the FIFO memory could be skipped in the original sensors, but the serializer and low-level signaling drivers can be preserved as the data can flow to the end-of-stave lpGBT concentrators agnostically whether the new (event-driven) or old (frame-driven) RSU is used. The in-periphery serializer speed of 160 MHz is compatible with the event-driven readout scheme, i.e., how portions of data can be fetched and bit words serialized. The development of the new MAPS, proposed in this document, combines a high spatial and temporal resolution capable readout protocol, called Event Driven with Access and Reset Decoder (EDWARD) [8], with the so-called 100 nW front-end concept. The latter is faster with respect to the solution developed for the ALICE-ITS3 sensors in order to alleviate the effect of the Time-Walk (TW) on the timing resolution. Both technology pieces were developed for the Electron-Microscopy Laboratory Directed Research and Development (LDRD) project at BNL and for X-ray science pixel detectors.

The timing resolution achievable with the ALICE - ITS3 sensors is limited by the readout of the registered hits based on the priority encoder [9] that requires snapping of the frames, *aka* strobing that is the legacy of the ALPIDE concept [10], and by the operation of the front-end amplifier - discriminator complex that is characterized by a significant TW. The latter is not correctable due to the simplicity of the concept forced

by the drastically limited $\sim 20\,\mu m$ footprint of the pixel. Pushed up the timing resolution on the side of the EIC with respect to the ALICE ITS3 upgrade requires investment in the new R&D. At this point, it is worth mentioning the power consumption, which cannot exceed several tens of miliWatts per cm^2 to be able to cope with the cooling requirements. The optimization, aimed at the substitutional RSUs, operatively arranged internally to yield the increased timing resolution, will need to be developed capping the total power consumption close to the ALICE-ITS3 sensors. On one hand EDWARD leads to powers savings, but also investigations will be going, supported by the physics analyzes, towards checking whether some of the SVT detector layers, most likely the outer, sagitta layers and further disks, may not be designed with pixel pitches larger, comparing with the ALICE-ITS3 sensors, leaving room for optimization of the power consumption. Should larger pixels be envisaged, their pitches will most likely be selected from 1.5, 2, 2.5 $\times$ the original pixel pitch to be able to still substitute RSUs without any changes made to the periphery of the sensors.

1.4 Signals and Background in the EIC SVT Detectors

The combination of the relatively low signal rate of the EIC collisions and the requirement for stringent systematic control for EIC measurements calls for low background and detector noise in an EIC experiment. Regarding the rate of the physics-related signal, it is expected to be on the order of $\sim 500\,kHz$ At a+p event at the center of mass $10\,GeV \times 275\,GeV$, assuming a nominal luminosity of $10^{34}\,cm^{-2}s^{-1}$. Translating this value into the event rate per cm^2 per second, a negligible value is obtained, outpaced by the background, representing a significant challenge for the detector system. The types and levels of backgrounds are one of the main considerations on the detector design, and it is a major consideration for the Interaction Region (IR) integration. The experience at earlier accelerator facilities, especially the previous HERA electron-proton collider, indicates the importance of background studies and any measure to suppress them experimentally. The main sources of background in the EIC SVT detector environment result from:

- Deep Inelastic Scattering (DIS).
- Synchrotron Radiation (SR).
- Electron Beam and Hadron Beam Gas
- Fake Hits and Radiation Doses

The latter is electronics related, but the three first are most dominant beam induced backgrounds that are briefly described in the following.

SR - Background: Various sources of SR could have an impact on the background level at the Interaction Point (IP). When the trajectory of a charged particle is bent, photons are emitted that are tangential to the path of the particle. Bending and focusing of the electron beam is the main cause of SR within the IR. It is important to place the IP far away from strong bending magnets in the arcs to minimize SR. The tracking detectors in the central detector as well as the calorimeter have to be properly shielded against SR, therefore a number of absorbers and masking must be applied along the electron beam direction. SR also deposits several kiloWatts of power into the beam pipe in the central detector region, which must then be cooled. Additionally, SR can degrade vacuum quality by causing material desorption from the walls of the vacuum chamber and/or heating residual gas. This can have a direct impact on the two other main beam-induced backgrounds.

Electron Beam and Hadron Beam Gas - Background: Beam-gas interactions occur when the electron or the proton/ion beam particles collide with residual gas. Ion beam interactions with gas cause beam particle losses and halo, which reach detectors. This is an important source of neutrons that thermalize within the detector hall. A crossing angle and a short section of the shared beam pipe in the EIC design minimize the beam-gas problem. Table 1.4 shows the deep-electron scattering (DIS) and beam background cross-sections and rates as function of center-of-mass energy and the respective rates.

The rates in the SVT detector from SR, after coating the beam pipe with a $5\,\mu m$-thick gold layer reach from several 10^4 Hz in the endcap trackers to $10^4\,Hz$ in the barrel trackers. For the electron beam gas events one has the rates of a couple of 10^7 Hz in the endcap and barrel tracking detectors and for the hadron beam

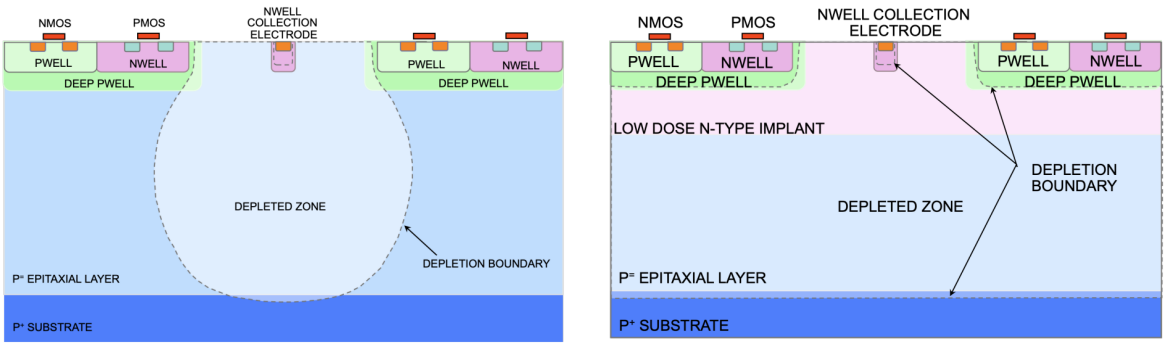
Table 1: Summary of cross-sections and rates for DIS and beam backgrounds as function of center-of-mass energy.

cross section	5×41 Gev	5×100 Gev	10×100 Gev	10×275 Gev	18×275 GeV
DIS ep (µb)	28.5	35	41	50	54
Proton beam gas (mb)	77.3	76.8	76.8	78.5	78.5
Electron beam gas (mb)	622.2	622.2	699.4	699.4	768.3
DIS ep (kHz)	12.5	129	184	500	83
Proton beam gas (kHz)	12.2	22	31.9	32.6	22.5
Electron beam gas (kHz)	2182	2826	3177	3177	317
Total rate	2207	2977	3392.9	3709.6	422.5

gas events one has 10^5 Hz in the barrel and electron endcap tracker and close to 10^6 Hz in the hadron endcap tracker. These numbers need to be compared to the rates from ep collisions of 5×10^5 Hz in the Barrel and electron endcap tracker and up to 10^7 Hz in the hadron endcap tracker. The most important conclusion from the quoted data referring to the rates of the physics-induced events and background is such that the expected event rate, calculated per cm^2 per second does not exceeds 1 MHz on the barrel and endcap layers. It is worth mentioning that the data rates were assumed to be 5.8 MHz per cm^2 per second when extracting benchmark performance of the ALICE-ITS3 sensors [7].

2 Description of ALICE-ITS3 MAPS Sensors

2.1 TPSCo 65nm Fabrication Process



(a) (b)

Figure 1: Structural cross-section of a pixel in a a) standard process b) modified process [6].

The TPSCo (Tower Partners Semiconductor Co.) 65 nm process is a state of the art CMOS process for image sensors. It is is a continuation of the TowerJazz 180 nm process, which was successfully used in development of all layers of the ALICE-ITS2. The inarguable advantage of this process family is that it offers a deep pwell that shields the readout analog and logic circuitry from the epitaxial layer. In this way, only the collecting nwell electrode is allowed to collect charge from the high-resistivity epitaxial layer. In

a result, the collecting electrode can have a small size, which results in a small input capacitance, which improves Signal-to-Noise Ratio (SNR) and also allows to build low-power Analog Front-End circuitry. Due to the pwell shielding, it is also possible to use the full CMOS process in the readout circuitry and build a complex circuit network in a pixel. Additionally, the pwell shielding suppresses the noise from the readout circuit to the sensor. The process allows modifications, such as an additional low-dose n-type implant, to obtain full depletion in the epitaxial layer which speeds up the charge collection and makes the sensor more radiation hard. The cross section of a single pixel is presented in Fig. 1. It should also be mentioned that in the TPSCo 65 nm process, it is possible to perform two-dimensional stitching of reticles on a single silicon wafer, resulting in a detector with a large surface area as shown in Fig. 2.

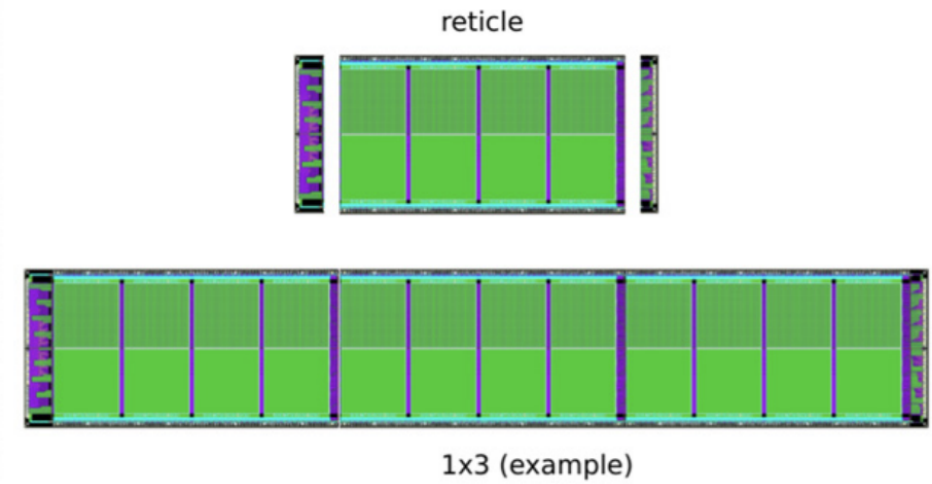


Figure 2: Example of creating of an object made of 3× stitched recticles [11].

2.2 Development of MAPS for the ALICE ITS3 Upgrade in TPSCo 65nm

The ALICE collaboration is developing the improved MAPS detector for the ITS3 upgrade to replace the three innermost layers of the current tracker during the Long Shutdown (LS3) of the LHC 2026-2028. During this R&D efforts, the MOnolithic Stitched Sensor (MOSS) prototype chip was developed [11]. It is a proof of concept for the stitched wafer sensor diced off 12-inch wafers.

3 Proposed Front-End Design and Readout Method, Resulting in Simultaneous High Spatial and Timing Resolution

The combination of solutions presented in this proposal is aimed at converting the original large are sensors into such that will be able to work with time resolution improved by more than an order of magnitude while maintaining other parameters, such as high spatial resolution and low power consumption. Also a strong point of the proposal is that the goal is not to start building these sensors from the proverbial "scratch", but to build on the already developed platform and focus strongly on cooperation with the ALICE-ITS3 team for which the results of the proposed R&D program may also be interesting, e.g., for a detector that ALICE-3 will require [12].

3.1 Event-Driven Readout vs. Time-Framed Readout

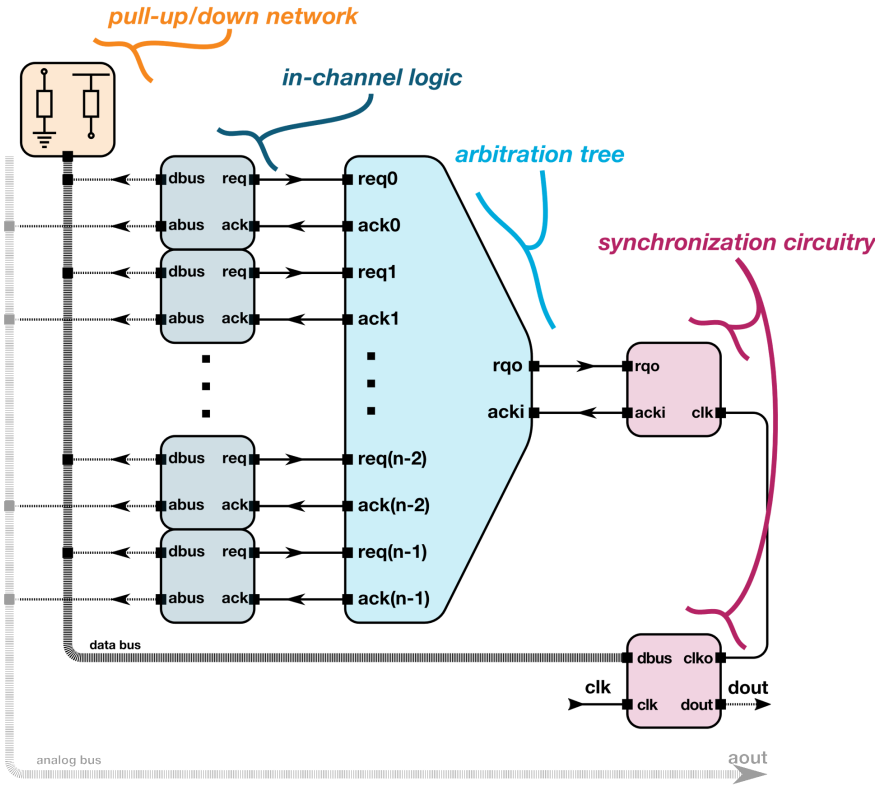


Figure 3: Block diagram of EDWARD readout architecture, in an exemplification suitable for handling combined analog an digital data.

In the recent years, at BNL, efficient readout methods, applicable to handling pixel arrays in radiation detectors, have been intensively investigated. The target has been to find the best, formalized for an efficient in-hardware implementation solution, allowing unambiguously scooping out positions of hit pixels, where the hit pixels are imprints of interaction of X-ray photons with the matter of silicon, pixelated sensors. In the targeted applications, such as for example full-field fluorescence X-ray imaging (soft X-rays) or satellite-born missions, such as NuSTAR (hard X-rays), X-ray photons arrive to a detector typically asynchronously and the impact positions are non *a priori* known. Only the readout that is tasked with this goal must be able to extract these positions and, in an undisturbed way by the simultaneous appearances of the new positions with hits, report them to an external processing and storing system by sending the addresses of the positions under which the interaction took place. It is important for the efficiency of the system supported by the implementation of the readout protocol not to group pixels with signals into time frames but to pump information to the output as it appears. At the same time, an important problem that must be solved is the arbitration of access to the transmission medium between the channels reporting the need for their reading service. The point is that there are no collisions and that none of the channels is privileged, which from the user's point of view means no loss of information, no false readings and no alteration of statistical distributions for the collected data. All these features, important for X-ray radiation detectors, are completely consistent with the needs of a detection instrument, which is a vertex and tracking detector in either an high-energy or nuclear physics experiment. The solution proposed to replace the time-framed readout, based on the priority encoder found so far in ALICE-ITS3 sensors, has been significantly advanced but has not yet been used in a full-scale pixel detector, which motivates its proposal under the generic R&D program for EIC.

As a result of the studies, a novel architecture, called Event-Driven With Access and Reset Decoder (EDWARD), has been developed [13] [8] and its block diagram is shown in Fig. 3. Its main advantage is

the ability for all pixels to send readout requests independently and exactly in the moment when an event occurs (e.g., when there was an interaction with a particle) and propagate these requests asynchronously over an arbitration tree. The tree is built on the basis of the arbitration structure described by C.L. Seitz [14] and stands in opposition to the currently widely used priority encoder-based arbitration. One example of a readout architecture that utilizes priority encoder is the Address-Encoder and Reset-Decoder (AERD) [9] architecture implemented for the ALPIDE chip - the MAPS detector used in construction of the ALICE-ITS2 tracking system [15]. The AERD architecture and its arbitration building block are shown in Fig. 4.

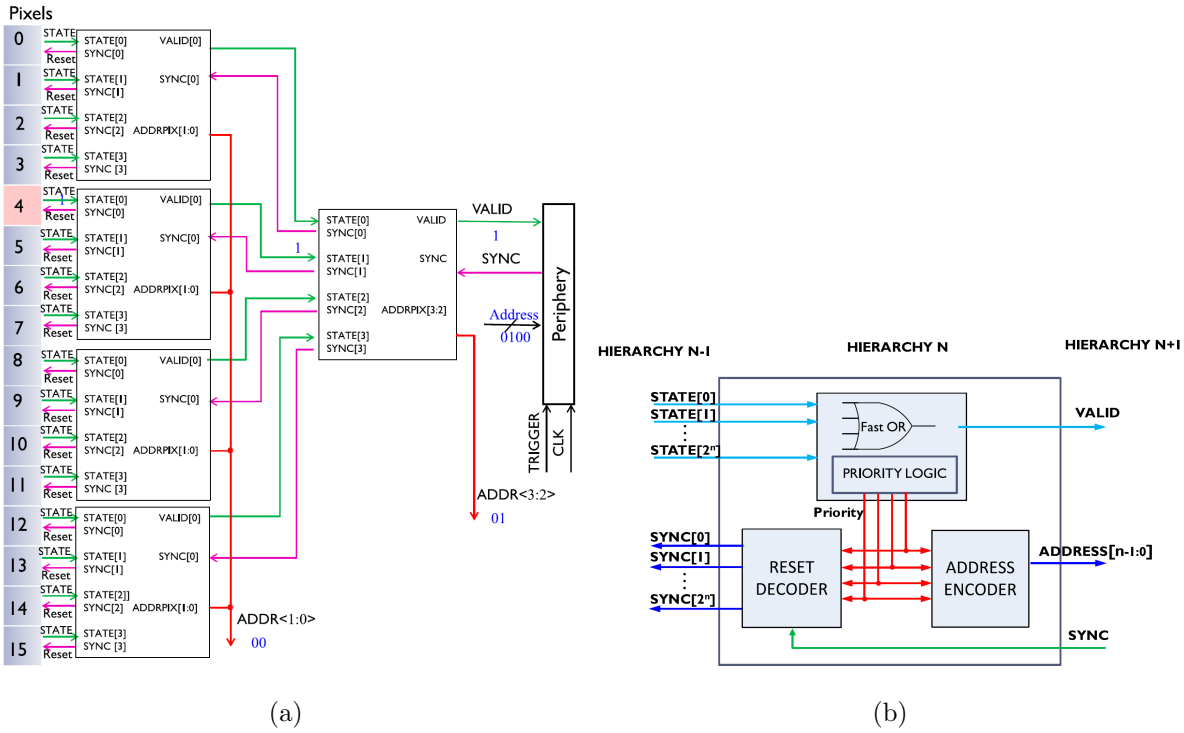


Figure 4: AERD readout architecture a) hierarchical structure b) structure of basic logic block [9].

The main feature that characterizes EDWARD and its arbitration method is that the EDWARD architecture has an arbiter cell that locally resolves the order of pixels to be read out based on the order of incoming requests and stores the result of this arbitration process until the request is withdrawn from the arbitration cell. The arbitration cell also does not allow an already started readout process to be interrupted until the pixel withdraws its readout request. Consequently, the EDWARD is devoid not only of built-in prioritization, but also of the need to snapshot the state of the matrix whenever it is read out. In this way, the architecture is free from dead time and does not accumulate pixel events while waiting for the frame clock (strobe). Instead of that, it allows continuous readout without polling the pixels for their state - it is the pixel itself that sends the readout request. The structure of the EDWARD arbitration tree is shown in Figure 5. Pixels are also armed with the mechanism that clears the readout requests after readout is done. This prevents repeated readout of the same event, as can happen when readout strobe is used, as shown in Figure 6.

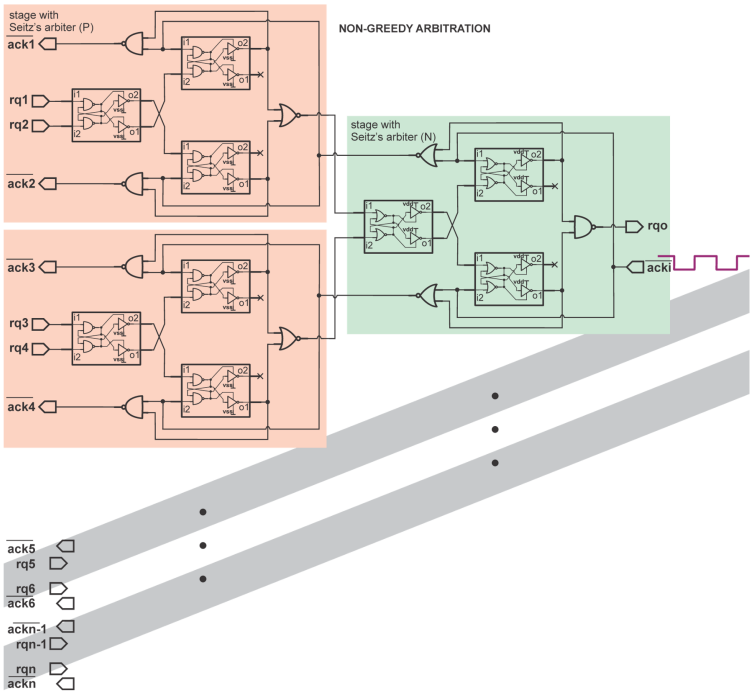


Figure 5: EDWARD arbitration tree structure with interconnected arbiters cells - simplified view.

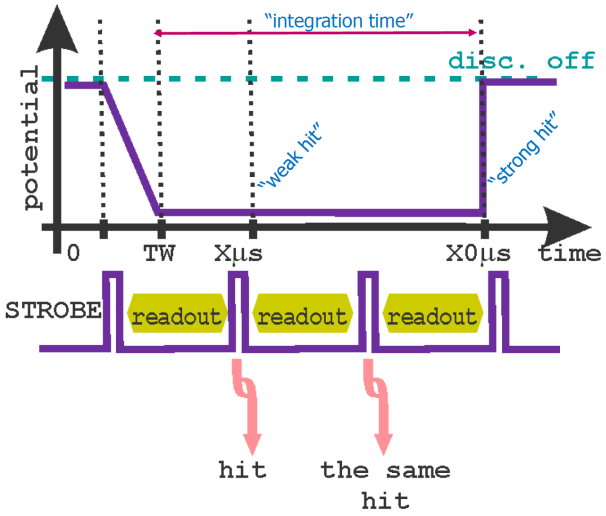


Figure 6: Risk of repeated readouts in the system with readout strobe when strobe frequency is higher than the integration time.

When it comes to DAQ systems, most of communication is synchronous in nature, often involving data serialization. Consequently, the compatibility between asynchronous readout requests and synchronous data forwarding needs to be guaranteed for seamless processing. EDWARD is not only equipped with such synchronization mechanism, but it also accomplishes synchronization in a nearly innate manner, as the concept revolves around generating readout acknowledge using the same clock that serves to latch data in the peripherals. In one cycle of this acknowledge clock, one, and only pixel can be serviced. Examples of responses to readout requests made at different times relative to the acknowledge clock are shown in Fig. 7. When a request is made during the active state of the acknowledgment clock, the readout can start

immediately. This is shown as the A and B cases in Fig. 7, respectively. When a request is made during the inactive state of the acknowledgment clock, it waits for the latter to change its state to active and only then the readout starts. This is shown as the C and D cases in in Fig. 7. Data in the periphery is always latched with the arrival of a new active state following the one in which the readout was initiated. This guarantees the minimum interaction time with the pixel and determines the minimum readout latency. Both are equal to the duration of the inactive state of the acknowledgment clock only. On the other hand, the maximum readout delay time in the case when only one pixel makes a readout request occurs when the request is sent just after the the acknowledge clock has transitioned to inactive. This time is equal to the sum of the duration of the inactive state and the entire period of the acknowledge clock.

By default, the duty cycle of the acknowledge is 50%, therefore the readout latency when only one request is made is in the range of ½ - ⅜ of the acknowledge clock period. In the actual system, the propagation time through the arbitration tree should also be taken into account, which should be added to the above-described range. However, it does not functionally affect the operation of the entire system. therefore, it is omitted for the purpose of further description for the sake of simplicity. It is also worth noting that the boundary case, when the readout request is made at the moment of transition of the active state to inactive, is devoid of the risk of any metastable state. Metastable states is one of the main problems in asynchronous circuits. A pixel in such a scenario may receive a residual acknowledge signal, but, if it is too short to switch a flip-flop that holds the read request, the readout will start with the next occurrence of the active acknowledge state in the pixel. The in-pixel interface logic for the EDWARD protocol is not discussed here, due to its obviousness.

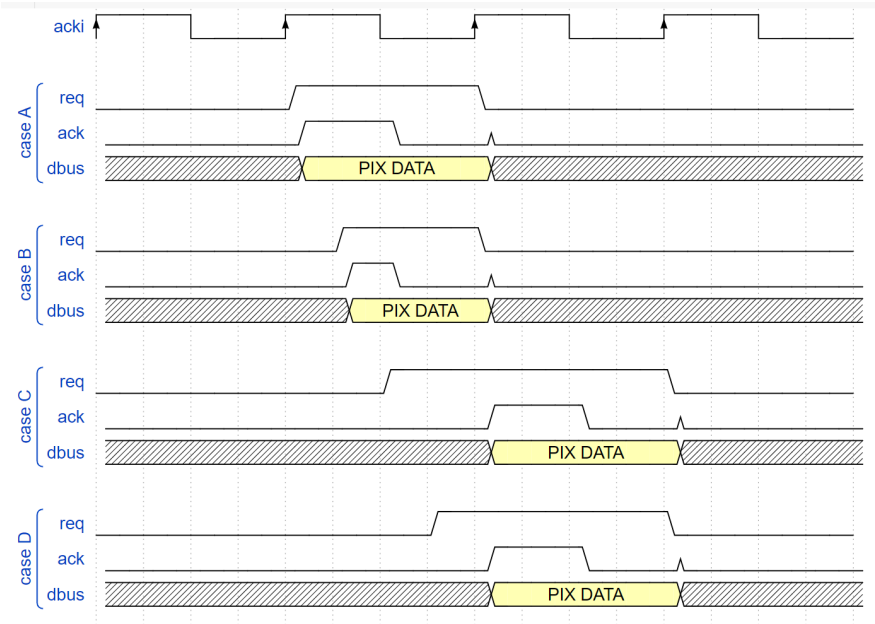
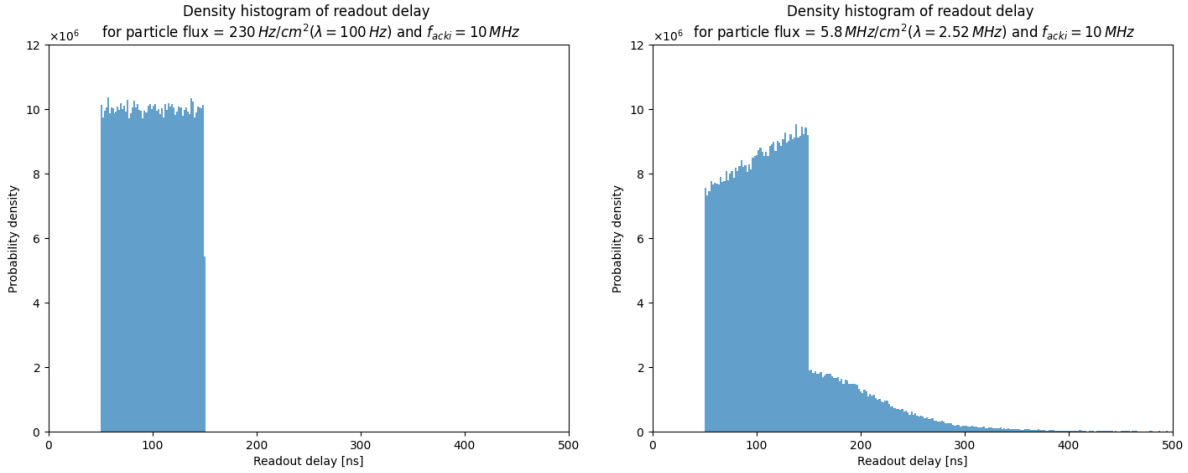


Figure 7: Illustration of response examples to readout requests sent at different times relative to the acknowledgement clock.

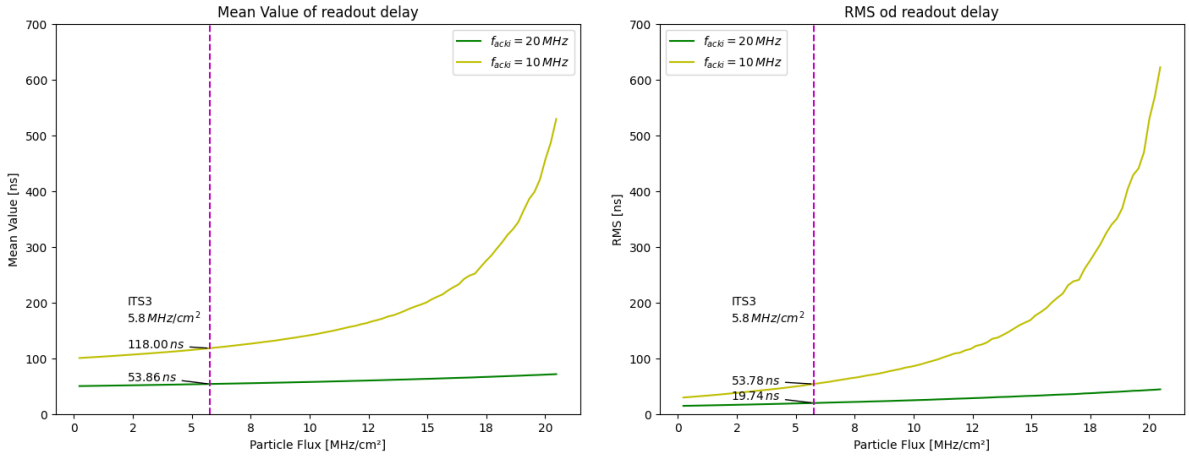
In regular operating conditions, readout requests from different pixels can stack, resulting in the longer readout latency, because it must also include the time needed for readout of other pixels. Fig. 8 depicts the variation in readout latency distribution based on a given, assumed particle flux. The readout latency in such a case depends strongly on the rate of generation of the events in the pixels and on the frequency of the acknowledge clock. In such conditions, the EDWARD architecture can be modeled using the queuing theory with the $M/G/1/k$ model [16], where M is the events generation process across the entire matrix with the rate strictly connected to the flux of particles, G represents the service time that follows a uniform distribution between ½ and ⅜ of the acknowledge clock period, $'1'$ signifies a common shared bus and periphery, and k is the number of pixels in the matrix, which caps at the maximum latency of the system. This makes the EDWARD architecture predictable. The benefits of replacements of the priority encoder based readout with the event-driven EDWARD architecture can be visualized on plots showing the mean readout delay and its

variability, given as rms, as shown in Fig. 9. The proposed two acknowledge clock frequencies (10 MHz or 20 MHz) are consistent with the assumed data width of 16 bits, following the ALICE-ITS3 architecture, and the available system clock frequency of 160 MHz in the ALICE-ITS3 sensors. The 20 MHz frequency utilizes the principle of Double Data Rate (DDR).



(a) (b)

Figure 8: Density histogram of the readout latency for a) low particle flux (almost no stacking of the readout requests) b) particle flux corresponding to the one assumed for the the ALICE-ITS3 case [7]. Calculation of the particle flux are made under the assumption of EDWARD system reading data from a ⅓ cm^2 (being the size of a region in the ALICE-ITS3 sensors) with an additional events generation factor resulting from the assumed charge sharing factor of 1.3.



(a) (b)

Figure 9: a) Mean Value and b) Root Mean Square (RMS) of readout delay as a function of particle flux

A close examination of the graphs in Fig. 9 clearly illustrates the advantages of the proposed solution over the onse used for the ALICE-ITS3 sensors in the environment of the EIC. Even assuming the minimum integration time of 2 µs, reported as possible in the ALICe-ITS3 sensors, the maximum possible timing resolution for the ALICE-ITS3 sensors is $^{2\,\mu s}/_{\sqrt{12}} = 577$ ns, while using EDWARD, it is is possible to descend to 20 ns, which is the 20-times improvement. Furthermore, the proposed solution not only offers better

timing resolution, but also brings the advantage of reducing power dissipation in the matrix, because it eliminates the distribution of the strobing signal, which for the ALICE-ITS3 sensors can consume 2 $^{mW}/_{cm^2}$ alone.

3.2 Low-Power Front-End Design

The ability of the event driven readout protocol, such as EDWARD, to extract hits immediately as they appear in the pixel array (RSU) and route them to the peripherally located serializers for further sending them off to the DAQ must be accompanied by a combination of an in-pixel charge amplifying, voltage pulse forming and discriminating circuit interfacing with the readout protocol structures, which itself do not introduce greater uncertainty in determining the Time of Arrival (ToA) of the incoming hits than the reading protocol. Due to the small size of the pixel, the in-pixel circuit network of the signal processing blocks must be very simple, making correction of the deterministic TW component impossible. Designing such a signal processing system that TW, therefore its dispersions, was small, encounters difficulties related to the power budget, which is pragmatically limited to no more than 100 nW per pixel. An evolutionary, i.e. based on the ALPIDE concept [10], version of an in-pixel amplifying, discriminating, and reset circuit from the MOSS ALICE-ITS3 structure [17] is shown in Fig. 10a. This amplifier choice results in the $\sim 2\,\mu s$ TW at the $1\,\mu s$ rise time of the voltage pulse response and $\sim 40\,nW$ of the static power consumption. It follows that the use of only the proposed event-driven reading system would not bring the expected effect in improving the time resolution, because the ToA measurement error would be dominated by the amplifier circuit in the pixel. An illustration of how TW combined with snapping of frames *aka* "strobing", used in the ALICE-ITS3 sensors, impairs time resolution by routing "stronger" and "weaker" hits into separate time bins, depicted as time "buckets", is shown in Fig. 10b. "Weak" and "strong" hits, shown in Fig. Fig. 10b are small- and larger-amplitude signals, resulting in the slower and faster rise time of the voltage pulse response, respectively. In conclusion, it can be seen that in order to be able to fully use the power of the proposed frameless readout, appropriate R&D required in order to design a suitable in-pixel processing circuit network, which will feature a smaller absolute variation of the signal rise time.

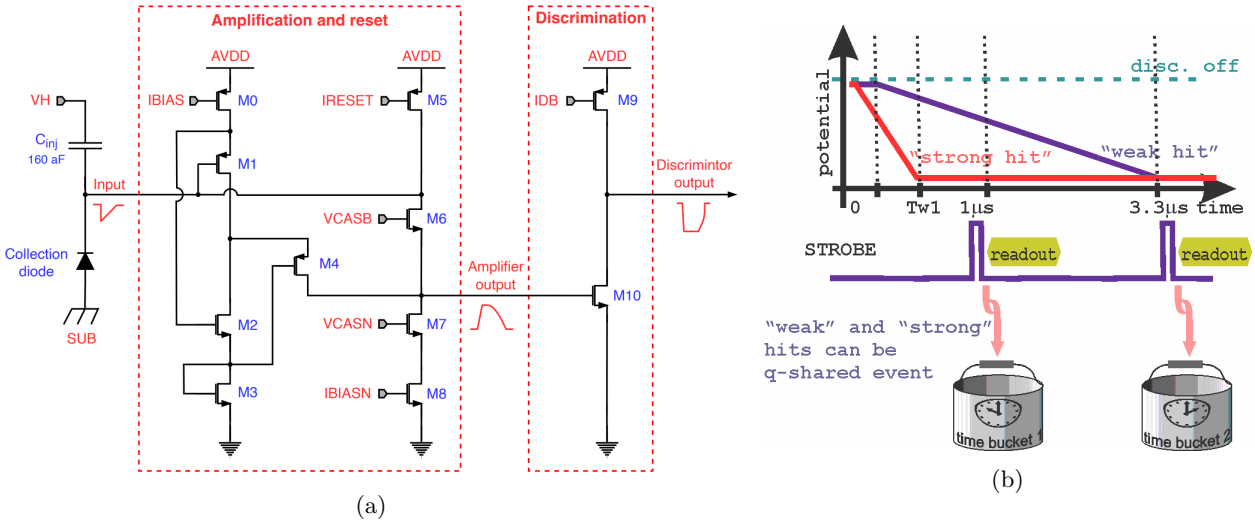
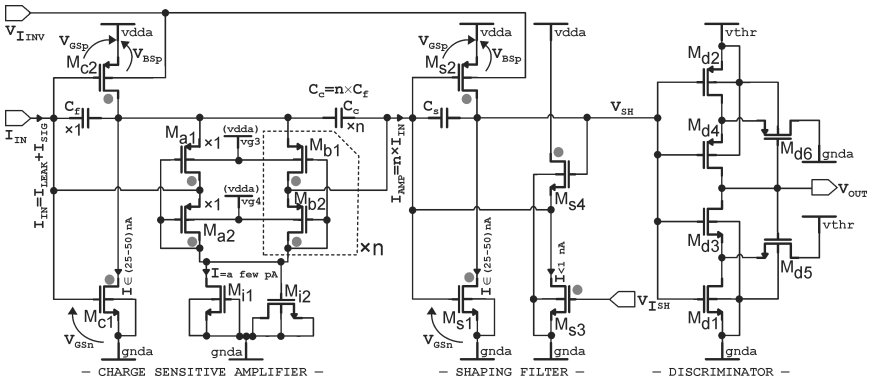


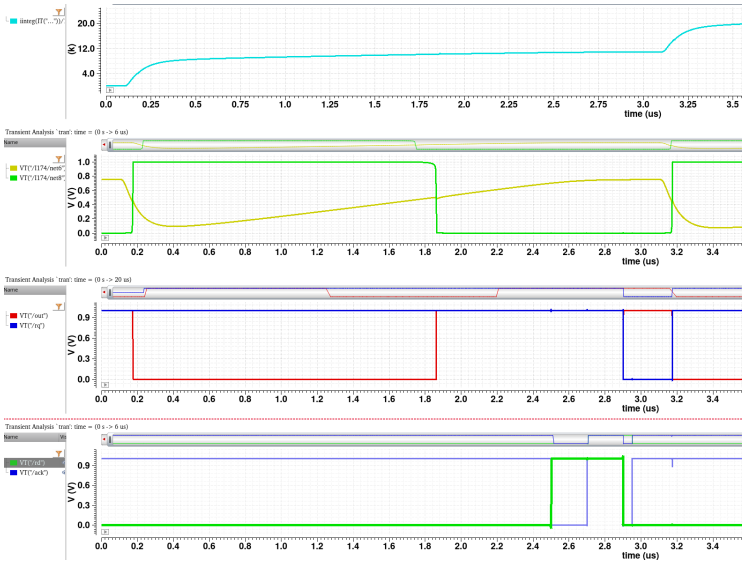
Figure 10: a) Evolutionary from ALPIDE version of an in-pixel amplifying, discriminating and reset circuit from the MOSS ALICE-ITS3 structure [17], b) Illustration of TW-contributed uncertainty of ToA measurement.

The candidate for the in-pixel processing network is a combined amplifier, signal shaping filter and discriminator system, which was developed on the basis of a nonlinear pole-zero canceling circuit network using the Self-Cascoded Field Effect Transistor (SCFET) topology [18] in the course of the LDRD project targetting pixel detector for electron microscopy at BNL. A simplified, transistor-level schematic diagram of the in-pixel charge amplifying, voltage pulse forming and discriminating circuit is shown in Fig. 11a. The

circuit contains three stages built with inverter amplifiers offering the required high open-loop gain at very low bias current. The bias current of the inverters is controlled by a substrate bias that is chosen to set a well-defined bias current regardless of the power supply. The first stage realizes charge gain. The second stage realizes pulse formation, where the initial voltage step is discharged using a constant, low-value current, resulting overall in a unipolar voltage pulse. The last stage is a discriminator that is effectively a Schmitt-gate inverter possessing built-in positive feedback that accelerates swings of the output voltage, resulting in faster discriminative decision. The transition point of the Schmitt gate, therefore the discrimination level, is controlled by the power supply of the gate. The three stage circuit network, shown in 11a, interfaces the readout with a simple, low-area-occupying digital circuit.



(a)



(b)

Figure 11: a) Simplified, transistor-level schematic diagram of an in-pixel charge amplifying, voltage pulse-forming and discriminating circuit [18], b) transient waveforms, showing in order from top to bottom results of input charge multiplication, formed output voltage pulses and responses of discriminator, interfacing with the EDWARD protocol.

The circuit network was developed and simulated at the schematic level in the TSMC 65nm process and has been called the 100 nW Charge Sensitive Amplifier (CSA) for the total power consumed by the circuits. Its use for the EIC requires translation into the target TPSCo 65nm process, optimization at the transistor and layout level, targeting fitting its implementation in the small footprint of the 20 µm pixel cohesively with the distributed circuit of the event-driven readout protocol. Transient waveforms, showing in order from top to bottom results of input charge multiplication, formed output voltage pulses and responses of

discriminator, interfacing with the EDWARD protocol, i.e. exchange of the read request and acknowledge signals, respectively 11b.

3.3 Compatibility of the Proposed Solution with the ALICE ITS3 Sensors Framework and Its Forking for the EIC Detectors: ePIC, Detector-2 and Upgrades

The implementation of the work program included in this proposal is based on the use of the large-area sensors framework that is under development for the ALICE-ITS3 upgrade. To use these sensors for EIC, agreements are being negotiated between the ALICE experiment and the EIC. It is known that the innermost barrel vertex and tracking layers for the ePIC detector will most likely be directly used sensors that will be eventually developed for ALICE-ITS3. As for the outer barrel layers and hadron- and electron- direction endcap wheels, it is planned to build ePIC-oriented sensors based on ALICE-ITS3 sensors, with the main emphasis on stitching optimization, multiplexing of data downloaded by lpGBT IP blocks, etc.

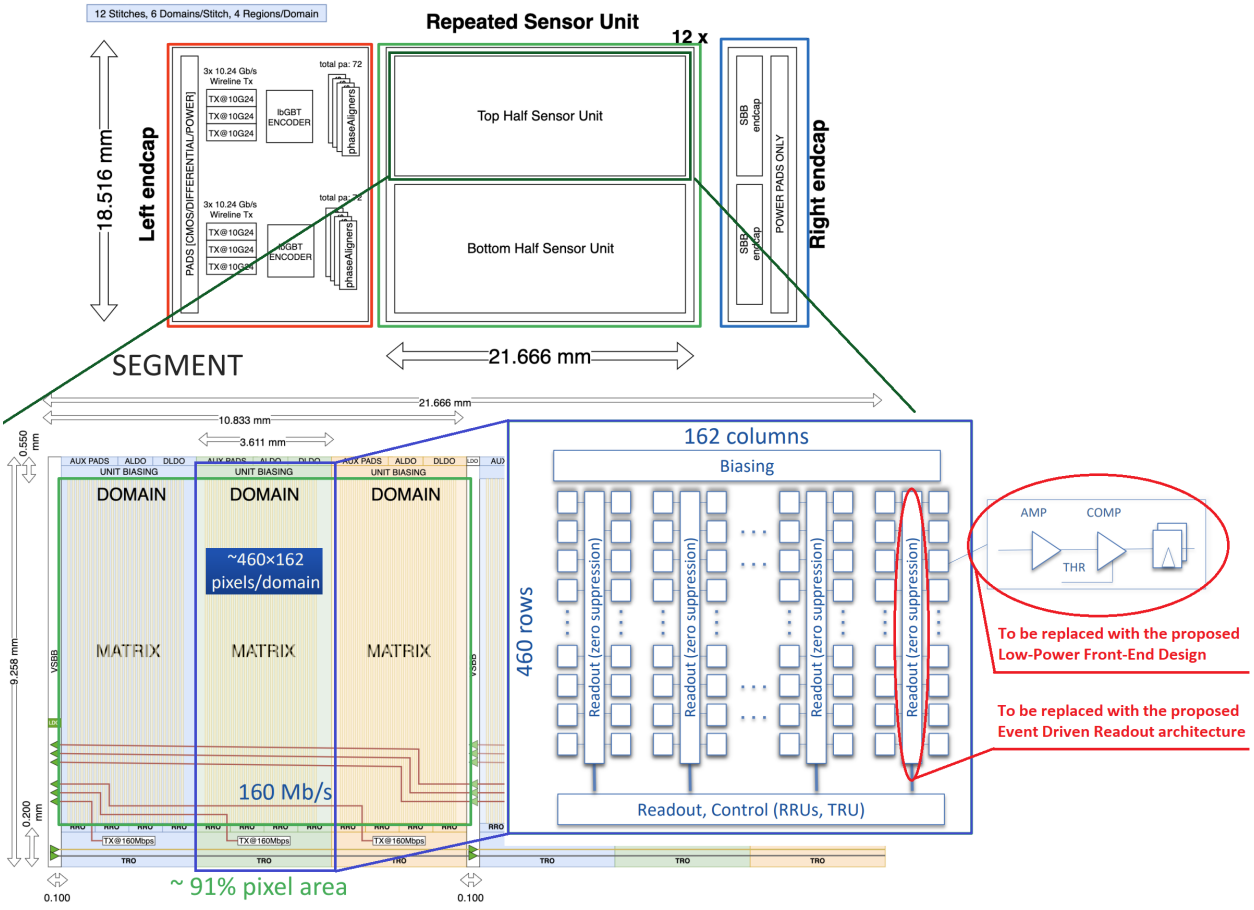


Figure 12: The structure of the stitched detector proposed by the ALICE collaboration for the ALICE-ITS3 sensors to be fabricated on the run ER2, with its internal structure and a proposal for adaptation.

4 Project Implementation Strategy

The proposed list of project tasks is described as follows:

Task 1: Determine detector operating conditions, requirements and needs to compare the capabilities

of the ITS3 detector with the proposed new solution. This task includes work related to identifying areas where the proposed ITS3 fork for the EIC performs below expectations and how the solution proposed here can influence the upgrade of the ePIC detector.

Task 2: ITS3 database exploration and environment configuration. This task, which parallels the theoretical recognition from Task 1, introduces the investigators to the circuit solutions and their implementations proposed in the database received from the ALICE collaboration.

Task 3: Development of architectural adaptations in the detector database. This task aims, as a first step, to describe the interfaces of the current solution, which will then be used to develop design requirements for the Low Power Front-End and the Event-Driven Readout System, elements that this proposal considers as an area to modify or replace.

Task 4: Integration of EDWARD readout architecture into the database. Based on the design requirements described earlier, this task involves making the desired changes to the database in order to obtain the RSU circuit solution with the Event-Driven Readout approach proposed here.

Task 5: Incorporating Low Power AFE into the database. Based on the design requirements described earlier, this task involves making the desired changes to the database in order to obtain the RSU circuit solution with the Analog Front-End approach proposed here.

Task 6: Functional verification of the detector with the new circuits. This task is to confirm the operation of the RSU after the changes and to obtain simulation results showing the benefits of the modifications.

Task 7: Comparison of the performance obtained with the assumptions made. This task involves documenting the implemented changes, describing the obtained results and explaining any differences between the assumptions and the obtained results.

Task 8: Creating the proposal of the new SVT detector which exploits the advantages of the increased timing resolution and low power design.

Note: Tasks 1 and 8 assume close cooperation between the Instrumentation Division and the Physics Department aimed at clearly defining the requirements on the one hand and demonstrating the veracity of the advantages of the proposed solutions. For this purpose, the participation of a Scientific Associate such as Postdoctoral Fellow is envisaged.

5 Development Plan and Milestones

The proposed timeline for completing the tasks described in Section 4 is shown in Table 2. Intermediate milestones are listed below:

- **Milestone 1 (month 3):** Documentation of the design requirements (Task 1-3 completed).
- **Milestone 2 (month 8):** Design of the RSU with the new readout circuitry (Task 4 completed).
- **Milestone 3 (month 8):** Design of the RSU with the new AFE (Task 5 completed).
- **Milestone 3 (month 11):** Simulations results of the modified design (Task 6 completed).

Table 2: Proposed project timeline

Month	Task 1	Task 2	Task 3	Task 4	Task 5	Task 6	Task 7	Task 8
1								
2								
3								
4								
5								
6								
7								
8								
9								
10								
11								
12								

6 Project Deliverables

The key project deliverables are summarized below for the following budget scenarios:

- **Scenario 1**: Realistic nominal budget (baseline budget).
- **Scenario 2**: Nominal budget minus 20%.
- **Scenario 3**: Nominal budget minus 40%.

Deliverable	Scenario 1	Scenario 2	Scenario 3
Documentation of the design requirements	Month 3	Month 3	Month 3
Design and simulation results of the RSU with the proposed readout circuitry	Month 11	Month 11	Month 11
Design and simulation results of the RSU with the proposed AFE	Month 11	Month 11	N/A
Comparison report with proposal of the new SVT detector	Month 12	N/A	N/A

Disclaimer: The implementation of a full, ready-to-use detector, containing the features described in this proposal, is an ambitious task and ultimately requires more resources than those available from the generic R&D for the EIC program. Achieving positive results of implementation studies, which is actually the subject of this proposal, will enable application for further funding and, which is the strong wish of the originators of this proposal, to formulate collaborative efforts, including the team from the ALICE experiment. These efforts are expected to be the result of the design involvements, but also physics simulation studies, as the vertex and tracking detector topology may be reformatted if the sensors are able to provide the response envisaged in this proposal.

7 Resources and Budget

The *money matrix* for the project, which itemizes the budget allocations to the R&D subprojects is shown below

Institution	R&D Subproject	Scenario 1	Scenario 2	Scenario 3
Brookhaven National Laboratory (BNL)	Event-Driven Readout	$72,000	$50,000	$72,000
Brookhaven National Laboratory (BNL)	Low-Power Front-End	$48,000	$46,000	$0

The detailed proposal budget is shown below.

Brookhaven National Laboratory

Directorate:	***Director, Advanced Technology Research Office***
Department:	***Instrumentation Division***
Title:	***LARGE-AREA MONOLITHIC ACTIVE PIXEL SENSORS COMBINING HIGH SPATIAL AND TEMPORAL RESOLUTION***
PIMS#:	***7118***
Principal Investigator:	***GORNI,DOMINIK S***
Period of Performance:	***10/1/2023 - 9/30/2024***
Sponsor:	***DEPARTMENT OF ENERGY***
Project Rate Type:	***IOR DOE & OLABS***

			NOMINAL BUDGET		NOMINAL BUDGET - 20%		NOMINAL BUDGET - 40%	
Sum of Amount			Reporting Year		Reporting Year		Reporting Year	
Cost Type	Group Break Descr	Description	2024	Grand Total	2024	Grand Total	2024	Grand Total
Direct Costs	BNL Direct Labor	Base Labor	$ 59,703	$ 59,703	$ 47,798	$ 47,798	$ 35,809	$ 35,809
		Base Labor - Research Assoc	$ 4,929	$ 4,929	$ 3,907	$ 3,907	$ 2,970	$ 2,970
	BNL Direct Labor Total		$ 64,632	$ 64,632	$ 51,705	$ 51,705	$ 38,779	$ 38,779
	Departmental Charges		$ 10,496	$ 10,496	$ 8,397	$ 8,397	$ 6,298	$ 6,298
Direct Costs Total			**$ 75,128**	**$ 75,128**	**$ 60,102**	**$ 60,102**	**$ 45,077**	**$ 45,077**
Indirect Costs	Indirect Overheads-Project G&A	VAB Common Institutional Recov	$ 33,031	$ 33,031	$ 26,425	$ 26,425	$ 19,818	$ 19,818
		VAB G&A Recovery	$ 7,783	$ 7,783	$ 6,227	$ 6,227	$ 4,670	$ 4,670
	Indirect Overheads-Project G&A Total		$ 40,814	$ 40,814	$ 32,651	$ 32,651	$ 24,488	$ 24,488
	Indirect Overheads - LDRD		$ 4,058	$ 4,058	$ 3,246	$ 3,246	$ 2,435	$ 2,435
Indirect Costs Total			**$ 44,872**	**$ 44,872**	**$ 35,898**	**$ 35,898**	**$ 26,923**	**$ 26,923**
Grand Total			$ 120,000	$ 120,000	$ 96,000	$ 96,000	$ 72,000	$ 72,000

Sum of FTE		Reporting Year		Reporting Year		Reporting Year	
LaborType	Name	2024	Grand Total	2024	Grand Total	2024	Grand Total
SCIENTIFIC	PINAROLI,GIOVANNI	0.07	0.07	0.06	0.06	0.04	0.04
	MANDAL,SOUMYAJIT	0.02	0.02	0.02	0.02	0.01	0.01
	DEPTUCH,GRZEGORZ W	0.02	0.02	0.02	0.02	0.01	0.01
	ASCHENAUER,ELKE C	0.02	0.02	0.02	0.02	0.01	0.01
PROFESSIONAL	GORNI,DOMINIK S	0.18	0.18	0.14	0.14	0.11	0.11
POST DOC	POST-DOC	0.05	0.05	0.04	0.04	0.03	0.03
Grand Total		**0.36**	**0.36**	**0.28**	**0.28**	**0.21**	**0.21**

Sum of Hours		Reporting Year		Reporting Year		Reporting Year	
LaborType	Name	2024	Grand Total	2024	Grand Total	2024	Grand Total
SCIENTIFIC	PINAROLI,GIOVANNI	130	130	103	103	78	78
	MANDAL,SOUMYAJIT	36	36	28	28	21	21
	DEPTUCH,GRZEGORZ W	36	36	31	31	21	21
	ASCHENAUER,ELKE C	36	36	28	28	21	21
PROFESSIONAL	GORNI,DOMINIK S	311	311	248	248	189	189
POST DOC	POST-DOC	95	95	75	75	57	57
Grand Total		**643**	**643**	**513**	**513**	**387**	**387**

Sum of Months		Reporting Year		Reporting Year		Reporting Year	
LaborType	Name	2024	Grand Total	2024	Grand Total	2024	Grand Total
SCIENTIFIC	PINAROLI,GIOVANNI	0.84	0.84	0.67	0.67	0.51	0.51
	MANDAL,SOUMYAJIT	0.24	0.24	0.19	0.19	0.14	0.14
	DEPTUCH,GRZEGORZ W	0.24	0.24	0.21	0.21	0.14	0.14
	ASCHENAUER,ELKE C	0.24	0.24	0.19	0.19	0.14	0.14
PROFESSIONAL	GORNI,DOMINIK S	2.10	2.10	1.67	1.67	1.27	1.27
POST DOC	POST-DOC	0.60	0.60	0.48	0.48	0.36	0.36
Grand Total		**4.26**	**4.26**	**3.40**	**3.40**	**2.56**	**2.56**

8 Diversity, Equity, and Inclusion

Brookhaven National Laboratory recognizes the intrinsic value of an inclusive and diverse workforce in fueling innovation. Our proposed R&D initiative will substantially benefit from the variety of ideas and approaches fostered by diversity and inclusion. A workforce that reflects diversity not only stimulates individual growth but also enhances our collective intellectual prowess, leading to groundbreaking hypotheses,

strategies, and methodologies.

We are committed to providing opportunities to historically underrepresented or underserved groups, and we ensure this through equitable employment practices and a culture that promotes collaboration and fairness. In enhancing our diversity and inclusion measures, we will augment the productivity and effectiveness of our workforce, thus better preparing us to tackle evolving scientific challenges. Ultimately, our investment in diversity and inclusion signifies our investment in the future success of our scientific endeavors.

References

[1] R. Abdul Khalek *et al.*, "Science requirements and detector concepts for the electron-ion collider: Eic yellow report," *Nuclear Physics A*, vol. 1026, p. 122447, 2022.

[2] G. Deptuch *et al.*, "Design and testing of monolithic active pixel sensors for charged particle tracking," *IEEE Transactions on Nuclear Science*, vol. 49, no. 2, pp. 601–610, 2002.

[3] L. Greiner, E. Anderssen, H. Matis, H. Ritter, J. Schambach, J. Silber, T. Stezelberger, X. Sun, M. Szelezniak, J. Thomas, F. Videbaek, C. Vu, and H. Wieman, "A maps based vertex detector for the star experiment at rhic," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 650, no. 1, pp. 68–72, 2011. International Workshop on Semiconductor Pixel Detectors for Particles and Imaging 2010.

[4] W. Snoeys, "Monolithic pixel detectors for high energy physics," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 731, pp. 125–130, 2013. PIXEL 2012.

[5] F. Piro *et al.*, "A 1-µw radiation-hard front-end in a 0.18-µm cmos process for the malta2 monolithic sensor," *IEEE Transactions on Nuclear Science*, vol. 69, no. 6, pp. 1299–1309, 2022.

[6] W. Snoeys *et al.*, "A process modification for cmos monolithic active pixel sensors for enhanced depletion, timing performance and radiation tolerance," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 871, pp. 90–96, 2017.

[7] G. A. Rinella and W. Snoeys, "ER2 Stitched Sensor Design Progress EP R&D WP 1.2 General Reporting Meeting; online access: https://indico.cern.ch/event/1280150/sessions/491674/attachments/2647348/4583111/20230515-er2-design-progress.pdf," 2023.

[8] D. Gorni *et al.*, "Event driven readout architecture with non-priority arbitration for radiation detectors," *Journal of Instrumentation*, vol. 17, p. C04027, apr 2022.

[9] P. Yang *et al.*, "Low-power priority address-encoder and reset-decoder data-driven readout for monolithic active pixel sensors for tracker system," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 785, pp. 61–69, 2015.

[10] G. A. Rinella, "Overview of the ALPIDE Pixel Sensor Chip with focus on Readout Features; online access: https://indico.cern.ch/event/666016/contributions/2722251/attachments/1523408/2380925/20170914-ALPIDE-FoCal-Study-Aglieri.pdf," 2023.

[11] P. V. Leitao *et al.*, "Development of a stitched monolithic pixel sensor prototype (moss chip) towards the its3 upgrade of the alice inner tracking system," *Journal of Instrumentation*, vol. 18, p. C01044, jan 2023.

[12] A. Collaboration, "Letter of intent for alice 3: A next-generation heavy-ion experiment at the lhc," 2022.

[13] D. Gorni, G. Deptuch, and S. Miryala, "Event-driven readout system with non-priority arbitration for multichannel data sources," Oct 2022.

[14] C. L. Seitz, "Ideas about arbiters," *Lambda*, no. 1, pp. 10–14, 1980.

[15] B. Abelev *et al.*, "Technical Design Report for the Upgrade of the ALICE Inner Tracking System," tech. rep., 2014.

[16] J. Shortle, J. Thompson, D. Gross, and C. Harris, "Fundamentals of queueing theory," *Fundamentals of Queueing Theory: Fifth Edition*, 04 2018.

[17] G. A. Rinella *et al.*, "Digital pixel test structures implemented in a 65 nm cmos process," 2023.

[18] G. W. Deptuch, "Charge-Sensitive Amplifier with Pole-Zero Cancellation - provisional patent aplication no: 63/379,887."