Brookhaven National Laboratory

Slim Edge for LGADs

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ABSTRACT

In a silicon sensor, the cutline is usually placed at a distance which is three times the substrate thickness. In standard silicon sensors, which are usually 300um thick, the dead region is therefore about 1 mm away from the active region. In LGADs, which are from 20 to 50 μm thick, the scribeline can therefore be placed about 100 μm away from the active area. However, in present generations of LGADs, the scribeline is still placed quite far away from the active area. With this proposal we plan to fabricate test devices where the cutline is placed as close as possible to the active area, implementing a slim edge on thin devices. The slim edge will be obtained by trenching and subsequent passivation of the silicon; several methods will be explored and put under test.

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U.S. DEPARTMENT OF ENERGY

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Project Narrative

1. Introduction

In a silicon sensor, the scribeline is put at about three times the substrate thickness from the last grounded electrode, so that the depletion region extending from there does not reach the vertical cut. Here, many defects acting as current generation centers are created by the dicing: once the depletion region reaches this highly defecting area, a huge current is injected into the active area, making the device impractical to bias. In a standard silicon sensor, usually 300um thick, the scribeline is therefore placed at about 1 m from the active area; on the other hand Low-Gain Avalanche Diodes (LGADs) are built on thin substrates to preserve fast timing and, if the same rule is followed, the scribeline can be put at a distance of about one hundred microns. However, LGADs with cutline that close to the active area have not been yet produced and standard terminations are routinely used. This proposal aims at implementing for the first time a slim edge in LGADs. Slim edges have been developed in standard silicon devices for use in HEP, NP and Photon Science experiments: a slim edge allows for better tiling, reduction of insensitive area and increased coverage in large area detectors made by several smaller devices. Also, devices can be made smaller, increasing the yield of the fabrication batches. In EIC detectors, this is particular important as large area sub-detectors (TOF, Roman Pots, …) are planning to use LGADs as sensors, which have lower fabrication yields as compared with other silicon sensors.

As the thickness of LGADs can be as low as 1/10th of the standard silicon thickness, it is possible to use trenching techniques that are not practical in thick substrates. In the latter devices, Deep Reactive Ion Etching (DRIE) is usually used, which is a technique developed originally (and used mainly nowadays) for Micro Electro-Mechanical Systems (MEMS). DRIE allows for vertical trenches with high aspect ratio. Other techniques can be equally effective for thin substrates: KOH etch, RIE etching, and laser dicing. Passivation, which is a way to fill-up the generation centers at the damaged trench walls, can also be obtained by standard ion implantation performed on the slanted walls (as those naturally obtained by the etching methods mentioned above). Other methods include alumina or oxide passivation, etc. In the project, we plan to explore several of these methods by fabricating a batch of n-on-p diodes designed specifically for etching test purposes.

2. Termination in standard silicon sensors

Silicon sensors, after fabrication, need to be diced from the wafer along “scribelines”, usually by means of diamond saws or laser dicers. These procedures leave a vertical cut of highly damaged silicon, with unpassivated defects that can potentially generate an extremely high current. To be able to bias the sensor, such current must not be present. If the depletion region extending from the biased electrodes does not reach the damaged area, leaving the cut equipotential with the substrate, no current is present. To achieve this, the standard way to terminate the device is to leave a large inactive area at the edge of the sensor, far away from the active area. The extension of this area is about three times the thickness of the substrate. For example, for a standard 300-um thick silicon sensor, the scribeline is 1 mm away from the active area. In figure 1, an example of a corner of a (single-sided, i.e. with uniform back) microstrip sensor is shown. The distance between the last grounded electrode (Guard Ring #2) and the scribeline is 1mm. Also, to

prevent the depletion region from extending to the edge of the sensor, an n+ implantation is present at the edge of the device. The latter solution, which is implanting a termination implant of the same polarity as the substrate and keeping it at the back voltage by the conductive cut, is present in any kind of silicon sensor.

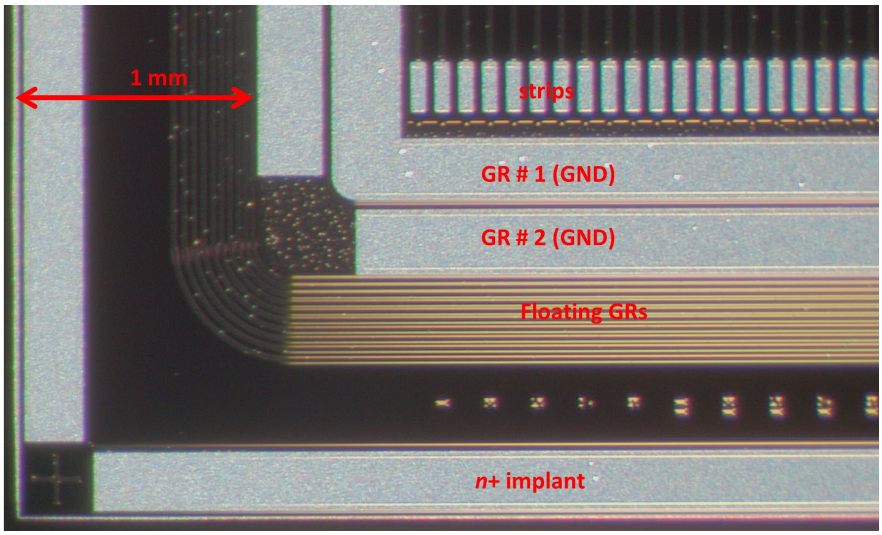

Figure 1. microscope picture of a corner of a standard microstrip sensor built on 300-um thick silicon. Scribeline is 1-mm away from the last grounded electrode (Guard Ring # 2).

If the sensor is used as a stand-alone detection unit, the large dead area does not pose any issues. However, for more advanced applications where large sensitive areas are needed, silicon sensors must be tiled together, and dead areas are of concern and should be minimized. Such detectors include, for example, pixel/strip arrays in industrial and or scientific applications (trackers at HEP/NP experiments). An example of these effects is shown in Figure 2. A way to minimize the dead area is to process a “slim edge”.

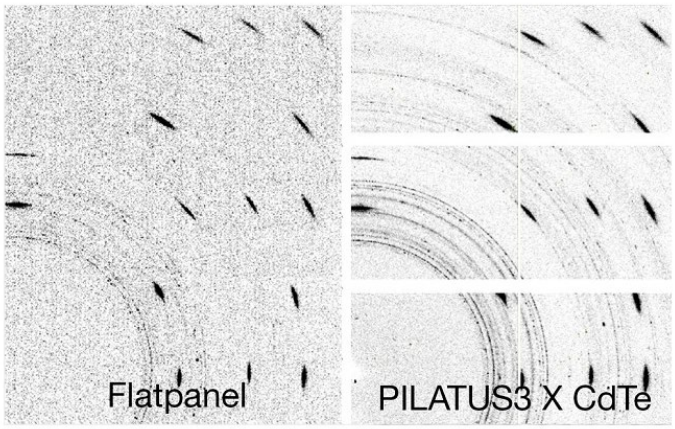

Figure 2: effect of dead regions in the imaging performance of a state-of-the art pixel detector (Dectris’ Pilatus)- right, as compared to a very large area detector (left). Inactive regions at the edge of the tiled sensor are clearly seen as white stripes with no events. From the web: https://www.azom.com/article.aspx?ArticleID=12442

3. Slim Edge for Standard silicon sensors

To reduce the inactive region from the standard of about 1mm down to a few tens of microns, a vertical trench can be etched close to the active area. The trench is then doped by diffusion in a furnace to make electrical contact with the substrate. Once the depletion region, which extends from the active area, touches the trench it stops there while, as the trench defects are passivated by the doping, no leakage current is generated at the trench walls. The technique to etch the trench is called Deep Reactive Ion etching (DRIE) which allows highly anisotropic etch process typically with high aspect ratios (up to 1:30). A SEM picture of a section of a trench is shown in Figure 3 [1].

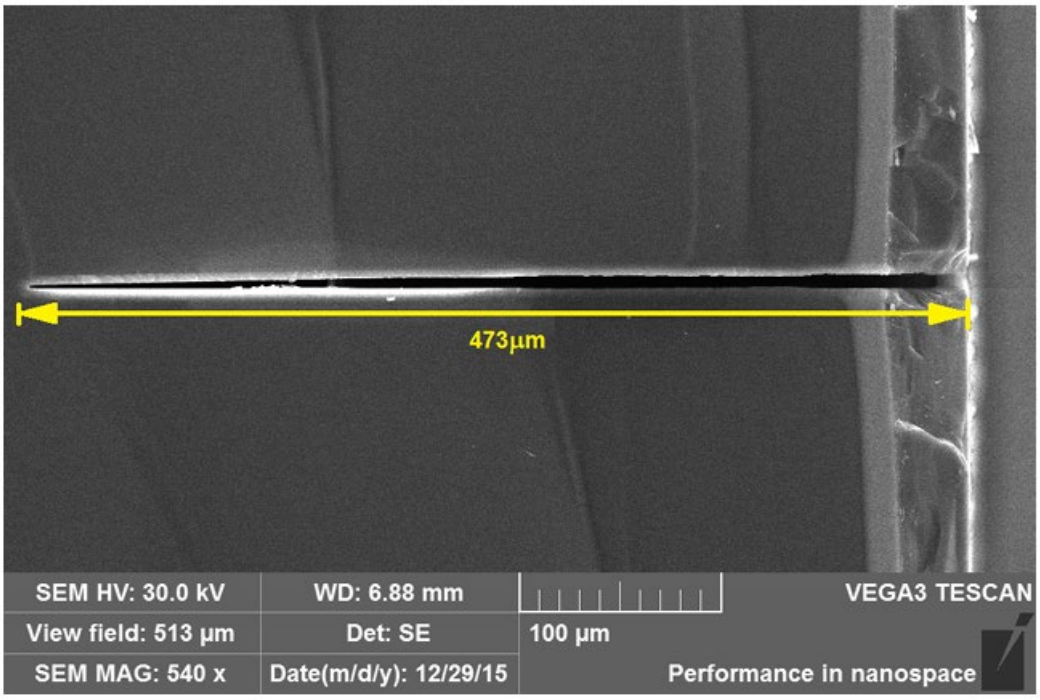

Figure 3. SEM image of the section of a deep trench etched in silicon (from [1]).

An example of trenched devices, used however for an X-ray detector, is shown is Figure 4 [1]. The same technique can be used to etched columns. In fact, the use of trenches and columns in NP and HEP was first proposed by S. Parker and al.[2], to make fast and radiation hard detectors for mips and X-rays. The concept was first applied in the ATLAS IBL (Insertable B-Layer) [3], where 3D detectors were placed at the end of this small barrel. Columns and mini trenches can also replace a continuous trench, with the important advantage that the wafer is self-sustaining during the clean room process and there is no requirement of a support wafer. In Figure 5 the layout of an example of such termination is shown. It was demonstrated that the depletion region stops at the mini trenches, without reaching the highly defective scribeline, which can therefore completely replace the use of a continuous trench [4].

DRIE etchers, however, are not found in any clean room and use highly toxic gases to etch the silicon (SF_6 and C_4F_8).

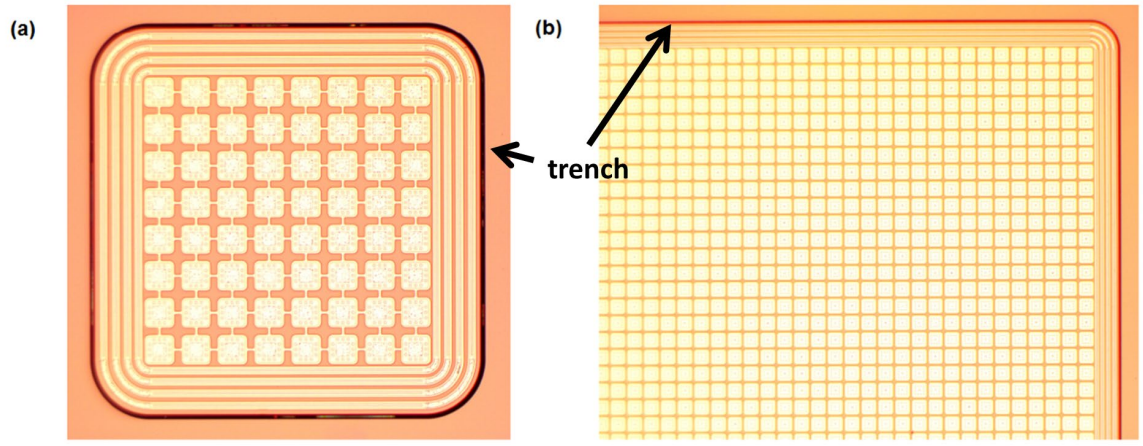

Figure 4. examples of continuous trenches etched at a short distance from the of the active area of pixel detectors, in this case, for X-rays detections at FELs.

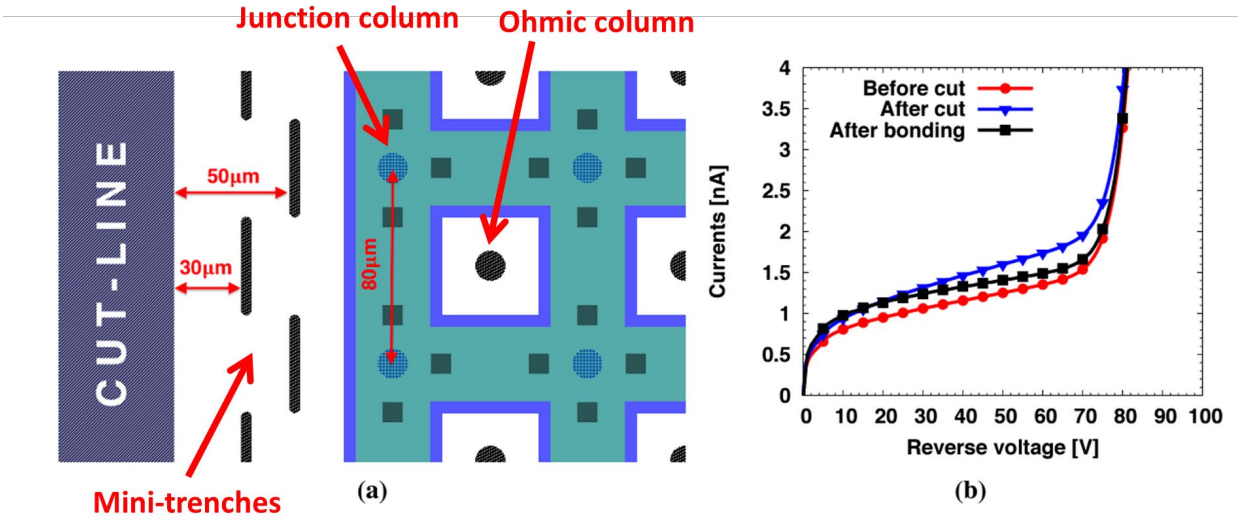

Figure 5. left: layout of a 3D silicon detector (with columnar junction and ohmic electrodes) which is terminated by a series of mini-trenches, which are however effective in preventing the depletion region extending outward up to the cutline. On the right, measured I-Vs show no difference in the leakage current before and after the actual cut.

4. Termination in LGADs

Low-Gain Avalanche Diodes are the baseline device to equip several sub-detectors in EPIC. Because of their excellent timing performance, down to 30ps per plane, they will be used in the TOF barrel and in the Roman Pots. As they are built on thin silicon wafers of 50um or less, when the rule-of-thumb described above is applied in the LGAD case, the distance between the active area and the scribeline needs just to be a few hundred

microns only. On the other hand, to achieve good timing, LGADs need to be biased well above depletion voltage, which extends laterally the depletion region considerably. For example, 50um thick devices are usually operated at about 200V, while the depletion voltage is usually lower than 50V (most of the depletion voltage is used to deplete the gain layer). But also in the case of overdepletion, TCAD simulations (as the one shown in Figure 6) show how the depletion region barely extends twice the substrate thickness, suggesting that the scribeline can be brought closer. Despite this, available LGADs still feature dead regions of the order of 1 mm.

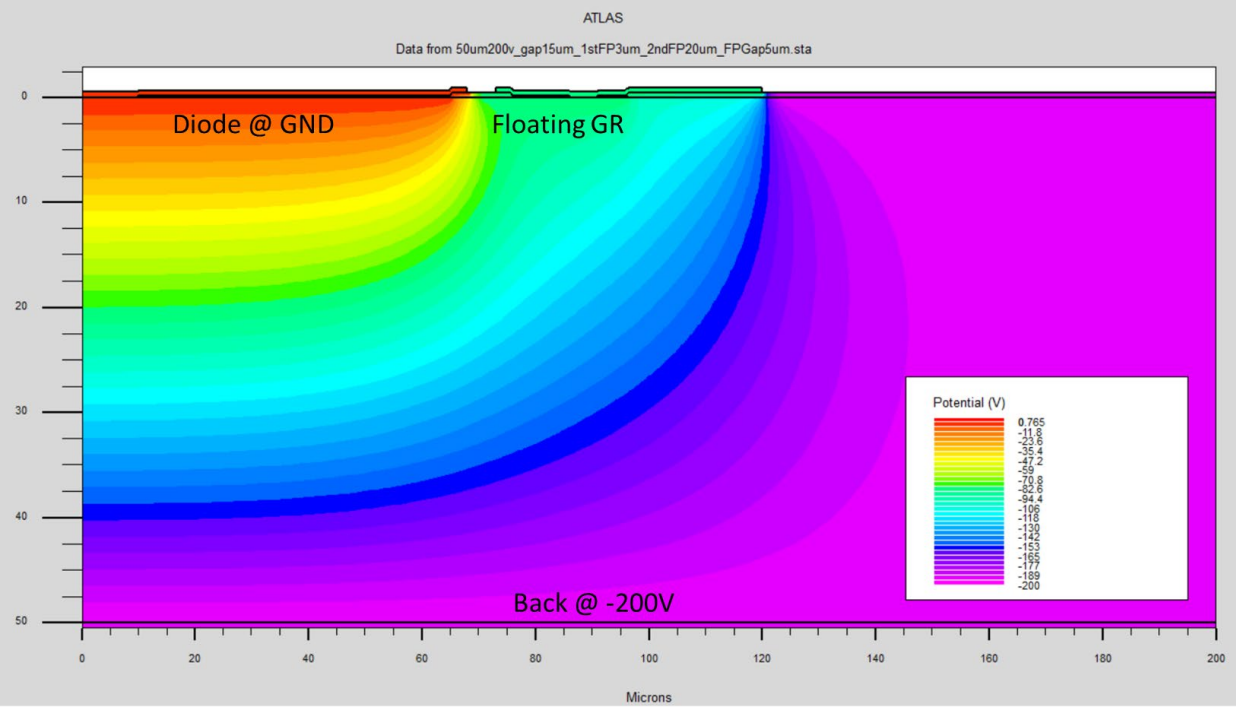

Figure 6. TCAD simulation of the electrostatic potential at the termination of a 50-um thick diode, biased in overdepletion: the depletion region extends laterally by less than 100um (simulation by J. Duncan, UofM, SULI intern at BNL).

Limiting the extension of the dead area at the edge of the sensor is important in large area detectors enclosing the interaction point (as the TOF) as one wants ideally to track all particles emerging from the IR. Tiling should avoid dead areas at all, but with large inactive region is not always possible. Moreover, in detectors such as those inside the Roman Pots, the sensitive area must go as close as possible to the beam spot yet avoiding any interaction of the beam halo with the dead region at the sensor border. In this application, the dead region must be minimized. It must also be stressed that LGADs are silicon devices with intrinsically low yield for large areas: defects in the lithographies which are harmless for standard strip and pixel devices are deadly for LGADs, as they cause anticipated breakdowns in LGADs. Keeping the extension of the dead regions to a minimum helps tiling smaller area devices, while still having good coverage. Small area devices translate in a (much) higher yield and reduced fabrication costs.

The R&D towards having a slim edge on LGADs, to the best of our knowledge, has not been considered yet.

5. Proposal: slim edge in LGADs

We propose to develop methods to implement trenches in thin silicon substrates, to bring the dead region of LGADs down to a few tens of microns. To do so, we propose to fabricate in our class-100 clean room at BNL, dedicated to the processing of silicon only, a simple batch of n-on-p diodes on thin silicon wafers and surround them with trench etched in different ways. While the difference between an LGAD and a diode is only in the presence of a gain layer in the latter device, there is no need of fabricating LGADs as the trenches will be etched externally of the active area where the gain is. The techniques can be applied to either one of the devices with no changes.

Techniques to etch trenches will avoid DRIE and rely on wet-etch (KOH on <100> oriented substrates) or regular dry etching (RIE). The advantage of such solutions is that no toxic gases are used (wet etch), or more readily available machines are deployed (RIE). Also, both techniques give origin to trenches with slanted walls that can be exposed to ion implantation of boron to passivate the damaged trench. Furnace diffusion is therefore not needed. Passivation with aluminum oxide (characterized by a negative charge, therefore inducing a hole accumulation layer at the interface) is also an option that will be explored.

A challenge may arise when lithographies need to be defined after trench etching. The wafer coverage by resist spinning may not be optimal, making the lithography impossible. While we succeeded in the past to make lithographies on not-flat surfaces, we can mitigate the issue by developing a process requiring as few lithographies as possible after trench etching or relying on spray resist coating (as last resource).

6. Deliverables and milestones

For this one-year project (FY24) we foresee the following deliverables:

month 1-2: design of the photolithographic masks, TCAD simulations, process flow based on studies with generation of a spreadsheet with the list of the fabrication steps to be performed in clean room. Submission and fabrication of the photolithographic masks to Photronics Inc.

- **Deliverables**: **production of photolithographic masks and definition of the clean-room process**

month 3-4: fabrication process in clean room, with exclusion of trench etching

- **Deliverables**: **silicon substrates ready for trench etching**

month 5-6. Implementation of trenches on a few wafers, leaving other wafers behind for alternative solutions, should the first etching method prove unsuccessful. Process may require additional steps to complete the sensors after trenches are etched.,

- **Deliverables**: first wafers completed with trenches

month 7. Static tests on device (including failure tests, SEM imaging etc) to check functionality of trenched devices.

- **Deliverables: static characterization of device and next plans laid down**

month 8-9. New method for trench etching and passivation. This activity will be carried on in either case of success or failure of the first trenching method.

- **Deliverables**: **method #2 for trench etching/passivation**

month 10. Static tests on device (including failure tests, SEM imaging etc) to check functionality of trenching method # 2.

- **Deliverables: static characterization of device**

month 11 -12. Additional tests and trenching methods can be explored on remaining wafers. Static characterization will follow. Writing of reports and papers will possibly be carried out at this stage.

- **Deliverables**: **additional methods for trenching, reports/papers.**

7. Budget

Budget (full funding)

- Consumables for device fabrication: 15k$

5K$ for lithographic masks, 5k$ for ion implantation, 3k$ for miscellaneous clean room expenses (gas, acids, wipes, etc), 2k$ for testing materials.

- No travel is foreseen.

- Personnel:

BNL: 2 weeks for scientist (PI) to coordinate and supervise the work and perform research studies on slim edge techniques, 1 month of an engineer to design the wafer layout, define the process flow in clean room, follow most of the process and perform measurements on the final devices, 2 months of technicians to perform the work in clean room, set-up new work-stations (wet-benches etc) for wet-etch of silicon and wafer dicing.

The full funding will be 130k$ (BNL only).

Budget scenario (80% full funding)

The labor effort will be reduced to fit in the reduced budget. Fewer variations of trenching methods will be tried. A reduced number of wafers will be processed as well.

Budget scenario (60% full funding)

Also in this case, the labor effort will be reduced to fit in the reduced budget. Even fewer methods will be explored, and fewer wafers will be processed.

8. Cost Effectiveness

Trench etching by DRIE is a capability not commonly found in clean-rooms. Developing alternative techniques to trench LGADs (or thin silicon in general) will be beneficial as many actors can supply devices using such techniques. BNL collaborates with semiconductor companies by means of SBIRs (e.g. Cactus Materials Inc, Tempe, AZ) and the technology can possibly be transferred to them. If the technology proves successful and it is required for EIC detector(s), fabrication can be entirely carried out at Cactus Material Inc, or in another US company. The use of trench may lead to smaller area devices being compatible with the sensors required to tile large area detectors at EIC, decreasing fabrication costs by increasing the yield.

Supply of silicon wafers is also not a concern, as BNL has a few wafers in storage and in case they can be fabricated according to specs. Clean room supplies are not a concern, if orders are properly and timely dispatched. Furthermore, chemicals commonly used in the fabrication in clean room have a very long shelf life, so they can be ordered well in advance. At the time of writing, BNL is well equipped to start the fabrication immediately.

9. Diversity, Equity and Inclusion

BNL understands the importance and has a strong commitment to work with underrepresented or underserved minorities following DEI guidelines. If the proposal is funded, we will attract students from underrepresented neighborhoods surrounding BNL, and mentor them to work on multiple parts of the projects. We will accept undergraduates for the spring and summer terms, as well as high school students. They will be in the outstanding position to observe the research work leading to the fabrication of a device starting from scratch. Hopefully, it will inspire young researchers from underrepresented minorities to undertake much needed careers in instrumentation, electronic engineer, or STEM at large. The PI has a history of mentoring students from high schools, community colleges and local universities, and usually select students coming from underrepresented minorities. A list of mentored students is available upon request.

References

[1] L. Pancheri et al *2016 JINST 11 C12018, https://iopscience.iop.org/article/10.1088/1748-0221/11/12/C12018*

[2] S. Parker et al. NIMA Volume 395, Issue 3, 1997, https://doi.org/10.1016/S0168-9002(97)00694-3

[3] G. Darbo, https://arxiv.org/abs/1411.6937

[4] M Povoli et al 2013 JINST 8 C11022, https://iopscience.iop.org/article/10.1088/1748-0221/8/11/C11022