Design, Fabrication and testing of a multi-channel System on a chip for Low-Power High-Density High Timing Precision Readout ASIC for AC-LGADs (HPSoCv3)

14 July 2023

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Abstract

The HPSoC (High Timing Precision System on Chip) is a multi-channel waveform digitizing and processing ASIC being developed to read out ultra-fast, high-density sensor arrays such as AC-LGADs. The chip will ultimately be able to service up to ~100 channels, operate with 10 GSa/s waveform digitization, and use autonomous triggering, feature extraction and multichannel data fusion while providing timing precision <10 ps. To date, based on previous SBIR and EIC funding, we have developed the chip architecture design, and have been designing, fabricating and testing 2 prototype “chiplets" to optimize and validate the front-end components on the chip. Funding is sought to continue development and testing of the third revision (HPSoCv3), incorporating 9 channels into a full digital System-on-Chip readout modular component for the final multi-channel array readout. The new prototype will be tested both in isolation as well as in combination with EIC-specific AC-LGAD sensor array prototype(s). The compelling need for high-timing precision subdetectors to fully leverage the EIC machine and optimize physics sensitivity is discussed in detail in the EIC Yellow Report. AC-LGAD sensors are the designated sensor technology for the ePIC time-of-flight particle ID and Roman Pots subdetectors, and would also likely be part of the design of any second EIC detector.

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1. Proposal

1.1. Introduction, Motivation

Over the past several years, the introduction of Low Gain Avalanche detectors (LGADs) [1] photodetectors with low pitch and very high timing accuracy has enabled high-density designs for high energy and nuclear physics detectors offering excellent spatial and timing precision, including the EIC. Their use, however, is currently limited by the capabilities of existing readout electronics. Time-to-Digital Converter (TDC) and time-over-threshold solutions permit only an indirect estimate of integrated charge, cannot easily provide sub-pixel spatial resolution or correct for pile-up, sensor aging, radiation and other environmental effects, and suffer from a variety of effects contributing to timing imprecision such as e.g. timewalk, baseline wander, and waveform shape variations.

In order to address the limitations of time-based approaches such as TDCs, Nalu Scientific has designed a compact low-power readout ASIC, the High Timing Precision System on Chip (HPSoC), that implements full waveform digitization, programmable feature extraction and data fusion capabilities based on our previous experience with such readout chips [2, 3, 4].

When evaluating the electronic contribution to the timing resolution of LGAD-based detection systems, it is conventional to only consider the jitter contribution that arises from the fluctuation of the electronic noise around an optimized discrimination scheme. However, as the performance of fast timing systems is pushed farther, additional electronic contributions to the timing resolution arise, including those from digitization noise, pulse amplitude fluctuations, threshold-value fluctuation, timing reference jitter, and TDC time-scale fluctuations. When all these are taken into account, the overall electronic contribution to the timing resolution can be significantly worse than that of the isolated jitter contribution.

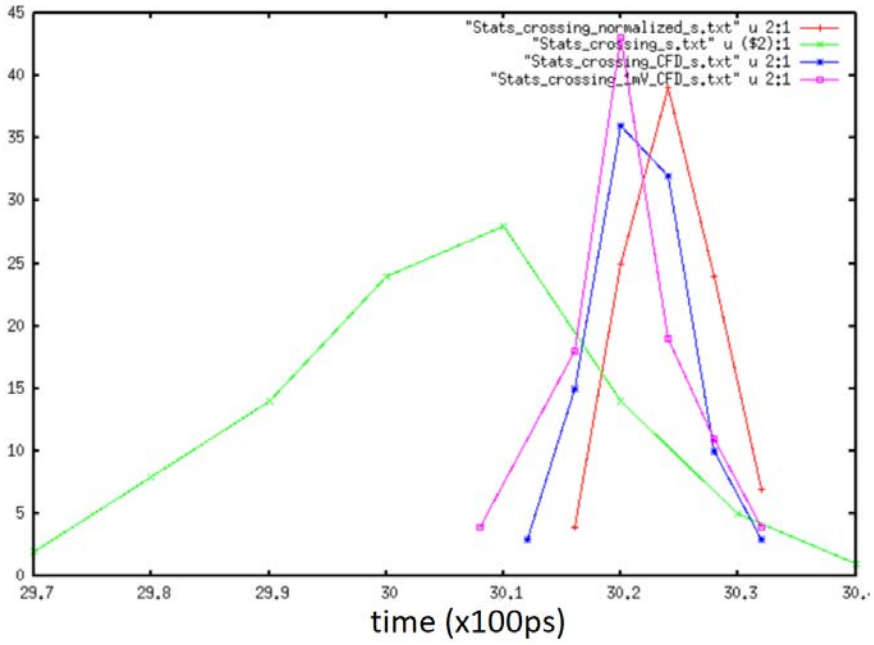

Figure 1: Histogram (number of events vs time of arrival) for various methods. Comparison of readout-associated timing resolution between constant-level discrimination and more sophisticated forms of time-of-arrival determination permitted by waveform analysis. The green histogram represents the spread of time-of-arrival results under the assumption of constant-level discrimination, when all sources of electronics-induced

uncertainty are included, yielding a timing resolution of 14 ps. The red and blue histograms show the improvement when the waveform is made use of to correct for varying pulse height, or perform full constant-fraction discrimination, respectively. For the pink histogram, a realistic digitization step of 1 mV is also included. The use of digitization restores the performance to the 5 ps target.

These contributions have been estimated in the context of the HPSoC system, for which all of these elements appear within the architecture of the ASIC, which, unlike other ASIC development efforts, includes an on-board 10 GS/s waveform digitizer[7, 8]. Figure 1 shows a histogram of time-of-arrival estimates available to a system employing a standard discrimination-based timing scheme, including all the potential sources of time-resolution degradation attributable to the readout (to ground the results, we used the output of the TIA designed as part of this project as described in the progress report of section 4). A resolution of approximately 14 ps is observed, far worse than the expected jitter contribution of 5 ps, and not compatible with a goal of 20 ps overall timing resolution once sensor contributions are added in. However, in comparison and also shown in Figure 1, are results obtained when a simple waveform analysis is performed, showing that an electronic contribution in the 5 ps range is recovered. Thus, the ability to measure and capture LGAD waveforms could be essential to achieving EIC goals for TOF timing resolution. Waveform digitization could also prove important in making use of information in neighboring channels to improve both timing and spatial resolution.

To date, two versions of the initial four-channel HPSoC prototype “chiplet” have been designed: the first to probe the relative performance of several analog front-end variants; the second, as part of FY2022 funding for this program, to refine the front end performance and to incorporate all features necessary for a self-operating channel acquisition. The latter chip is currently being fabricated and it will be performance tested in Fall 2022 without and with input sensor signals. As the next step, support is requested here to design, fabricate and evaluate a new nine-channel prototype chip version (a) incorporating all possible corrections in consequence of the testing of the previous design (b) integrating 9 channels in a single operating unit; and (c) designing the digital front end to permit feature extraction and data fusion. This new chip version (HPSoCv3 or “mini-HPSoC” in the following) will be a modular element ultimately incorporated in a larger readout device capable of directly interfacing large AC-LGAD arrays. Subsequent to that, we plan to finalize development of the full HPSoC with a minimum of 3x3 array of mini-HPSoC modules leading to a total of 3x3x9 = 81 channels integrated readout system. Evaluation of performance for EIC TOF systems for each of these HPSoC development stages is planned.

The target specifications of the fully developed HPSoC ASIC which is expected following the overall multi-year development process are given in Table 1, below. This is followed by an overview of the envisioned full chip architecture and testing results from the initial prototype chiplet which has been fabricated, as well as a summary of the design and fabrication of the second prototype as part of our EIC-Related Generic Detector R&D FY22 funding. Following that, we present our proposed FY23 objectives, along with a plan of work and the respective responsibilities of both institutional proponents. We subsequently briefly discuss participating personnel, including each institutional proponent’s efforts in advancing diversity, equity, and inclusion, and the areas of responsibility of each person for whom support is sought. We

conclude with effort and funding tables summarizing the proposed overall FY23 project, and a progress report for FY22.

1.1.1. LGADs based detectors at EIC

The EIC has a rich scientific program whose possible physics reach has been surveyed and summarized in the EIC Yellow Report [5], where LGADs based detectors were singled out as a technology of choice for far forward Roman Pots and Time of Flight (TOF) detectors. The spatial and timing precision possible with LGAD-based detectors directly correlates with fundamental detector properties such as e.g. charged particle identification performance. There is a critical need for a readout which can both meet the stringent limits on size and power for readout of the high-density LGAD arrays typical in large NP/HEP detectors while providing the ps-level timing precision required to fully leverage the capabilities of the sensor.

Existing EIC LGADs detector and generic R&D (eRD) efforts are on-going and one of the proponents here (UCSC) has been an active contributor in those efforts. Nalu Scientific has joined this effort more recently but has already been substantively participating in EIC for the past few years with the University of Hawai'i in the design and development of the baseline readout chip (HDSoC) for the hpDIRC.

Parameter	**Specification**
Channel no.	miniHPSoC chip (this proposal): 9 Full chip (post FY23): ~100 (pitch ~300µm)
Process	65nm CMOS
Sample rate	10 GSa/s
Bandwidth	2 GHz
No. bits	10
Supply Voltage	1.0V (2.5V for digital I/O)
Timing accuracy	5 ps
Front-End stage	Embedded TIA
Buffer length/channel	256 samples
Power/channel	<2mW
On-chip integration	miniHPSoC chip (this proposal): 9 channel autonomous sampling, digitization, calibration, initial feature extraction, packetization, data streaming Full chip (post FY23) adds: Integration in large channel count array readout (96+)

Table 1. Target HPSoC specifications.

1.2. HPSoC Architecture Design and Current Status

1.2.1. HPSoC Architecture

Channel Architecture: The overall structure of the HPSoC channel design is composed of three partitions, as shown in Figure 2. The main purpose of the first two chiplet designs was

to examine several front-end variants, and to test an enhanced four-channel prototype chip including an optimized front-end preamplifier design with autonomous digitization and autonomous triggering. The scope of this proposal is to extend the integration to a fully self-contained module capable of internal data calibration, feature extraction and fast serial communication, thus probing the entire system level features of the architecture.

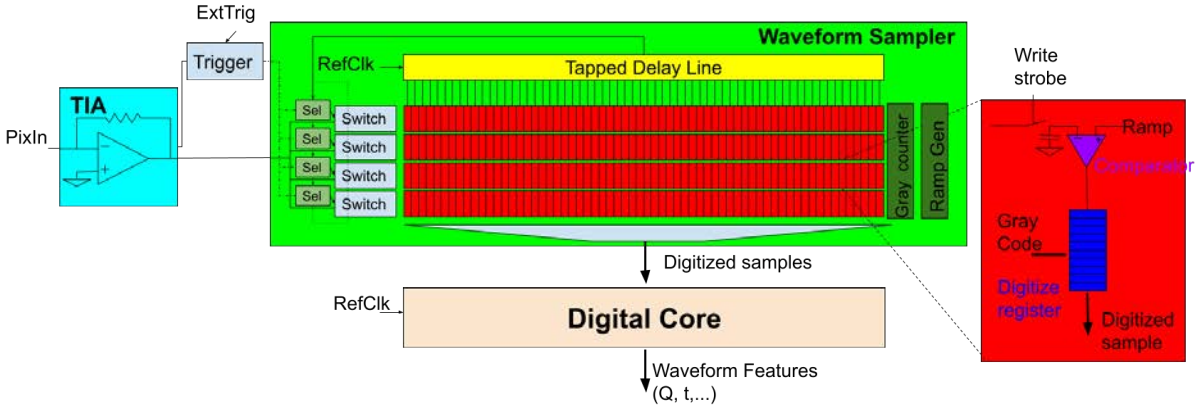

Figure 2. Overall channel architecture for the HPSoC chip, from left to right: transimpedance amplifier (TIA, blue), waveform sampler (green), and the digital partition (red).

Front-end amplifier: The front-end interface of each channel has been designed to satisfy the requirements of low power, adequate transimpedance gain to produce measurable voltage pulses, and capability of capacitive drive consistent with the load of the sampling array and signal to-noise ratio targets.

Waveform Sampler: This component will perform data sampling, analog storage, digitization and readout. It consists of a switched-capacitor array in which many samples can be converted to digital format in parallel. A hardwired mechanism is used to coordinate between (continuous) sampling and (on-demand) digitization, permitting simultaneous operation. Digitization will be able to be self-triggered via an internal discriminator (included in revision 2) for autonomous operation.

Digital partition: The digital partition will handle the readout of the digitized signal, together with calibration and feature extraction. For every triggered acquisition, the feature extraction module will identify the number of individual hits occurring on the pixel and the precise time and charge deposited. Feature extracted data consist of time of arrival and charge estimates.

All three components have been designed to permit area and power estimation and the layouts are shown in Figure 3, where the size of the digital component fits the long channel profile. This permits the layout of the complete channel tile within a small elongated area as a basic building block of the full system.

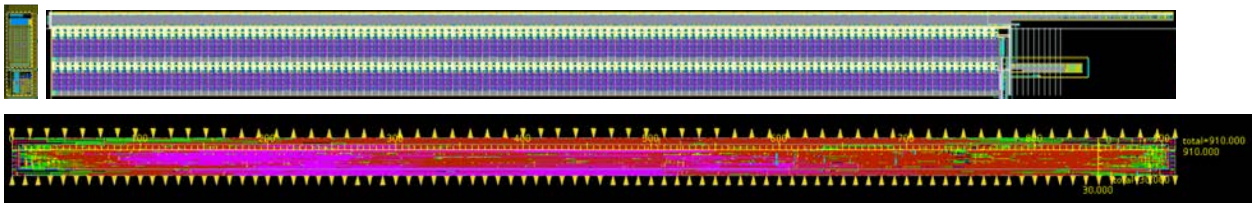

Figure 3. (Top) Front end amplifier and channel layout - approximate size: 900um x 80um for 256 samples. (Bottom) Fully placed and routed channel control - dimensions are 900x30um^2, including power rails.

Full chip architecture and floorplanning (Figure 4): The HPSoC will be modularly built as an array of channels, or "tiles", each capable of independently gathering data from the corresponding pixel. Each channel/tile will perform the operations detailed above and convert the signals from the sensor into timing and amplitude (charge). In the example in Figure 4, the four "hit" tiles respond with charge/timing pairs that encode the information of the hit. The time and charge information is then transferred to a data concentrator that can perform data fusion between neighboring channels to calculate an accurate estimation of the arrival position with sub-pixel accuracy and a sub-sampling time estimate of the event arrival.

The design of the digital and analog channel will permit the layout of the tile within a small area that can be further arranged in groups of nine pixels in a square configuration (a "super-tile"), as shown in Figure 5 (left). Using this concept, a possible floorplanning for a complete chip is shown in Figure 5 (right), where it can be seen that a final die of only 3x3 mm^2 could allow readout of a 9x9 array of pixels at ~350µm pitch or less. This takes into account the space which will be needed for common mixed signal logic (timing generation, in yellow in Figure 5, right), that we estimate is sufficient for the back-end logic to perform the data fusion operation. The super-tile design and testing is the goal of the present proposal.

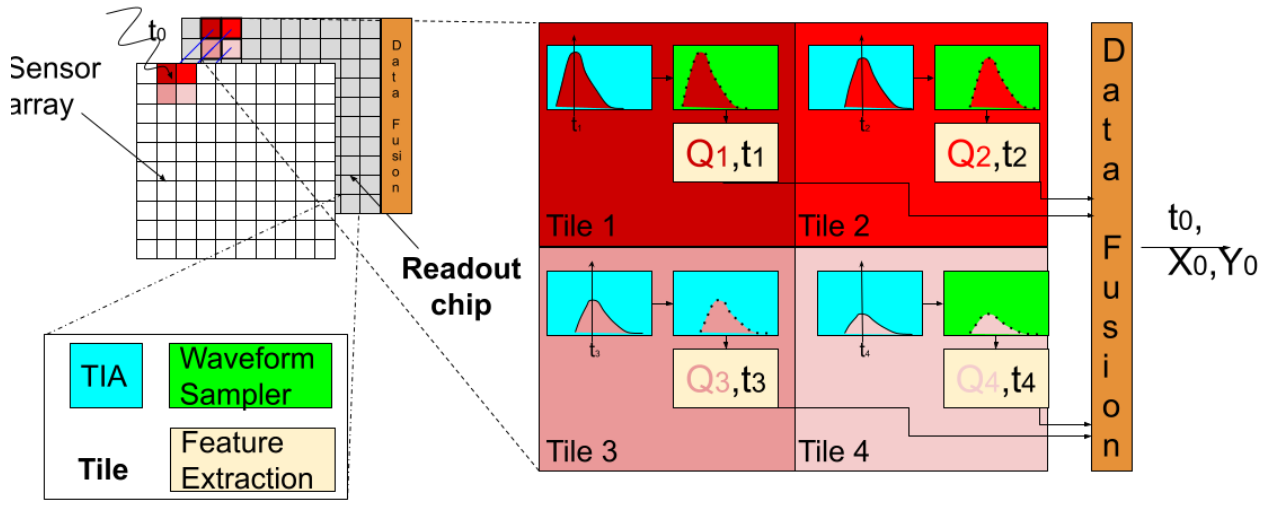

Figure 4. Conceptual operation of HPSoC-based sensor array readout.

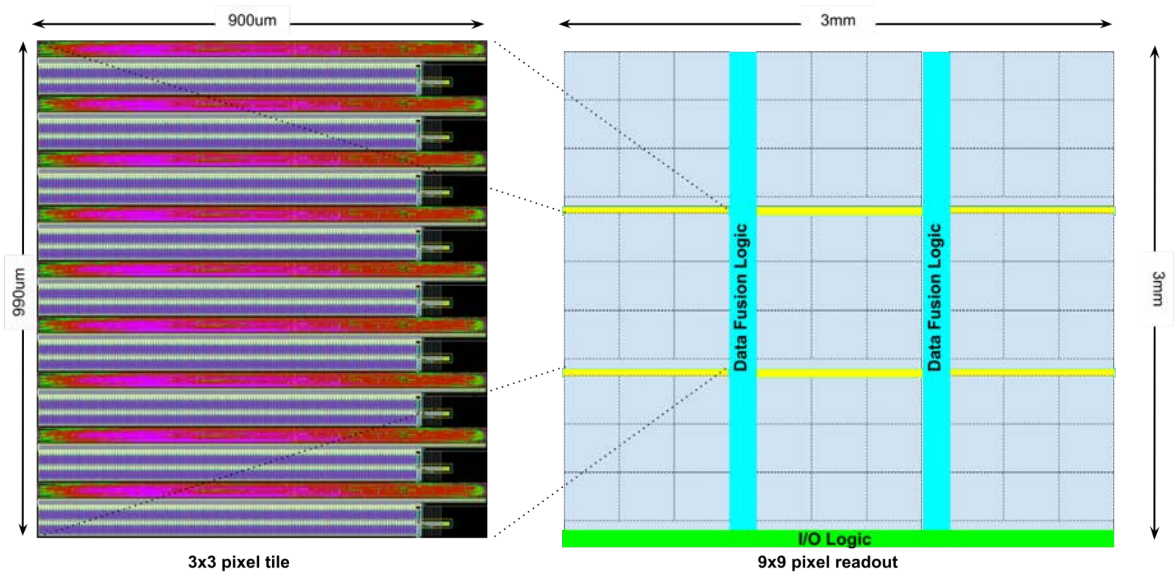

Figure 5. "Super-tile" floorplanning for 9 input channels, and conceptual floorplanning for a 9x9 channel HPSoC.

1.2.2. Overall HPSoC project evolution and current status

Due to the complexity of the design and the tight requirements on every part (TIA front-end, Channel Digitizer, Digital control, calibration and feature extraction, data fusion and fast rate data export), the overall project is evolving through a series of stages to validate the components sequentially. For this reason, we expect a 4-tiered approach to achieving the final performance, as shown in figure 6:

1. **Tiny-HPSOC (HPSoCv1)**: Small and inexpensive "tiny chip" fabrication (1.5mmx1mm) to incorporate the TIA and the basic sampling and digitizing array, for initial concept validation - this design and testing has been completed as part of an SBIR-funded project performed by Nalu in collaboration with SCIPP.
2. **4-HPSoC (HPSoCv2)**: Incorporation of 4 channels with independent triggering, self digitization, and improved TIAs based on the result of the previous experience. The design is finished and the testing and evaluation is being completed now as part of the performance of EIC-Related Generic Detector R&D for FY2022 of which this proposal is the continuation.
3. **Mini-HPSoC (HPSoCv3)**: Based on the results from 4-HPSoC, the individual channel operation is now defined and validated, and 9 channels (possibly modified to address potential shortcomings of the previous design) are integrated in a single self-contained module by the addition of digital back end to perform voltage calibration, feature extraction and data fusion. A fast interface is also introduced to allow at-speed data rate testing. The chip is the core atomic module that permits tiling into large array sizes. This is the task of the present proposal. The size of the device, albeit larger, is still expected to be reasonable and relatively inexpensive, based on the results from the previous integration efforts.
4. **Full-HPSoC (HPSoCv4)**: Integrate multiple modules into a large array readout (e.g. covering 9x9 channels or more) - this will require the coordination of the operation of the

individual modules and calibration memories, as well as the redistribution of I/O to facilitate grid readout for dense sensor arrays. It is outside the present scope, mostly due to the prototyping cost of the full chip, but it should be substantially de-risked through the results of testing for mini-HPSoC.

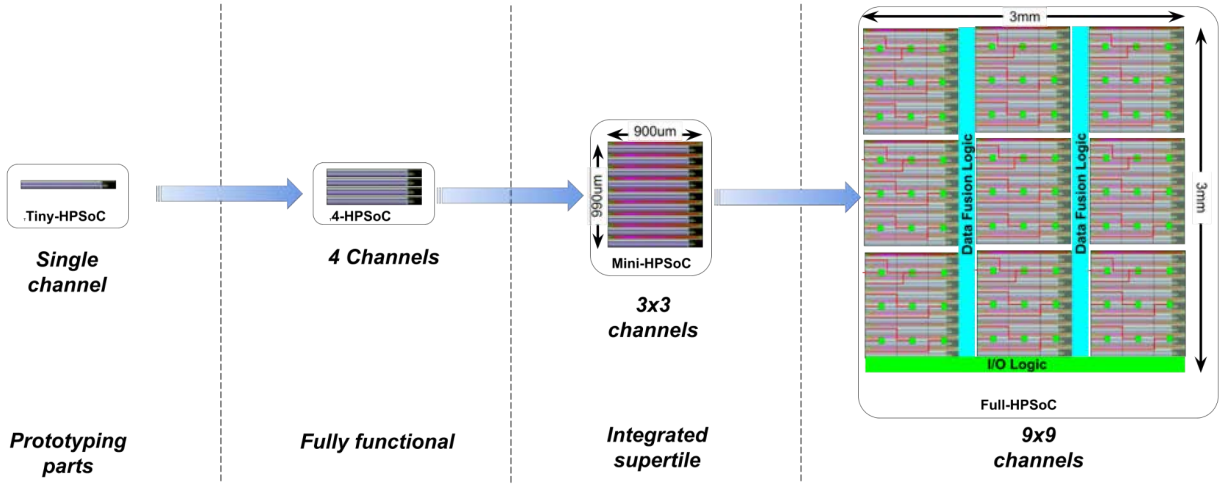

Figure 6. Evolution of HPSoC project

Tiny-HPSoC

HPSoC design and development was initiated under a DOE-HEP SBIR Phase I award. As discussed in detail below, support is requested here to continue HPSoC development and perform testing of the next iteration of the HPSoC chip using EIC-specific prototype sensors. The main findings and results of the Phase I DOE-HEP project were:

- **Architecture exploration:** a feasible HPSoC architecture, described above, was defined based on the target specifications**.**
- **Process exploration:** completing design of full analog, mixed signal and digital submodules in 65nm proved the process sufficient for both analog and digital performance.
- **Feasibility and achievable pitch:** it was found that area tiling permits an achievable pitch down to <~300 um.
- **Performance evaluation of front end:** using simulations after post-layout parasitic extraction of a selected design for TIA and gain stage, a gain stage capable of reaching the agreed-upon SNR necessary to achieve the desired timing performance for the whole system (<10ps) was designed. Using the output of a TIA stage, and estimating time jitter as the ratio between the RMS of the noise and the slope of the rising edge we obtain an estimated resolution of ~12.5ps, which is in line with estimates from simulation for a full input capacitance of 0.4pF.
- **Performance evaluation of mixed signal:** simulation taking into account device variability has shown the feasibility of a waveform sampling within the desired resolution. It is expected that up to 4 individual groups of 64 samples can be operated in parallel,

providing sufficient depth for deadtime-free operation at a maximum rate of ~1 MHz rate per pixel.

- **Preliminary design of digital channel component and architectural design of back end:** a full implementation of the channel digital component was completed and shown to fit within the area required to reach the pitch target. The digital component performs signal calibrations and simple feature extraction. The back end digital design to perform data gathering and fusion has also been analyzed and is expected to fit within the overall available area.

Tiny-HPSoC chiplet Fabrication

In order to perform an initial validation the HPSoC architecture design, a subset of the required components has been fabricated in a small 1.5x1.0 mm^2 chiplet (the “tiny-HPSoC” of figure 6), shown in Figure 7 (left), which contains:

- Four TIAs, with and without an extra gain stage;
- Four separate readout channels, with three different sampling cells and direct connection to the input to separately validate channel performance; and
- One channel connected to a TIA+gain stage to validate the overall signal chain from sensor output to digitized waveform.

Figure 7 (right) shows the chiplet test board; in the figure, the large yellow rectangular space is a fixture for incorporation of various sensor array configurations, the small square at the right of the rectangle is the housing of the fabricated die, and the components at the bottom permit calibration testing. Figure 8 shows close-ups of (left) a wire-bonded die connected to the calibration traces rather than a sensor, and (right) a chiplet wire bonded to an AC-LGAD sensor (here, FBK - RSD1 production 500um pitch, 200um pads). Test results to date, both with calibration inputs and connected to an AC-LGAD sensor, are presented below.

Tiny-HPSoC chip test results

The chiplet has been tested using both calibration inputs as well as with an AC-LGAD sensor. The sensor used was a 3x3 array FBK AC-LGAD [LGAD-Test] from RSD1 production 3x3, 500 um pitch, 200 um pads. This was connected to the 4 chiplet inputs using 3 sensor pads in a row to 3 chiplet inputs, N+ connection to input, GR + other pads to ground. A Sr90 source aligned with back of the sensor was used for testing, however, the low <1Hz data-taking rate limited the size of the collected dataset, which amounted to ~150 events on one channel and ~40 events on a second channel, and further testing with a IR laser is planned. Analogous sensor testing results were obtained from both channels. Only two of the chip channels produced usable data; issues in bonding with the other two channels precluded data-taking with them. The calibration dataset, which is for all four channels, was generated by feeding a voltage signal with a fast rise time (300ps 20-80%) from a function generator to an input network consisting of a termination resistance and a series small capacitor (0.1pF) into the chip input.

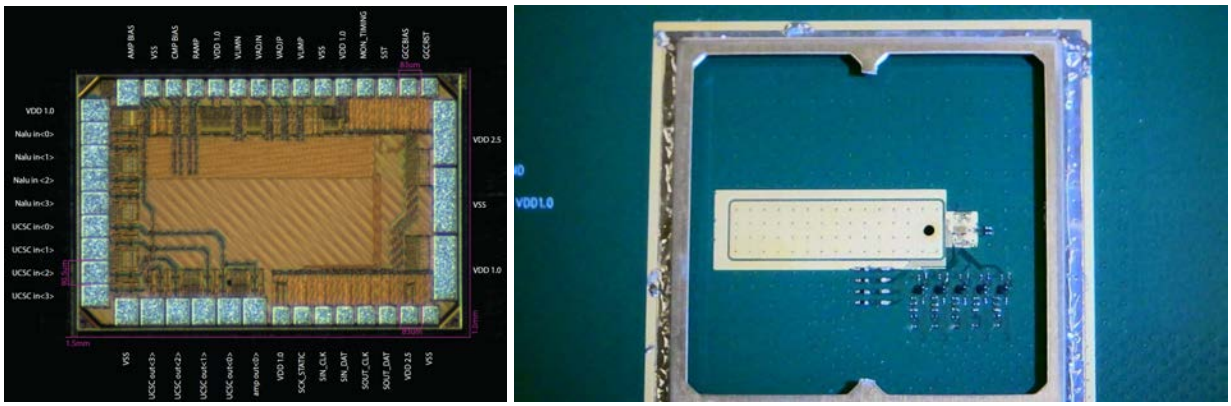

Figure 7. (left) Micrograph of fabricated HPSoC prototype chip; (right) chiplet test board, the large yellow rectangular space is the fixture for incorporation of various sensor array configurations, the small square at the right of the rectangle is the housing of the fabricated die, the components at the bottom permit calibration testing.

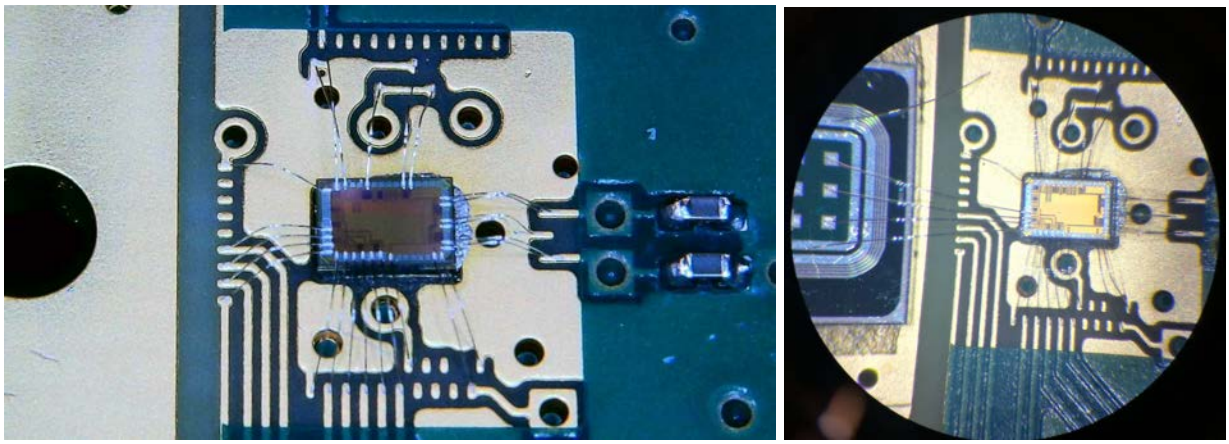

Figure 8. (left) Close-up of a mounted chiplet showing the wire bonded die connected to the calibration traces on the test board, it is used without a sensor array; (right) Chiplet wire bonded to an AC-LGAD sensor (here, FBK - RSD1 production 500um pitch, 200um pads).

Using calibration inputs at different levels, we performed linearity measurements as shown in Figure 9. As shown in the left sub-figure, output relative to the input step is reasonably linear with a slope ~0.1, for channels 1,2,3. When a full model of the input stage is considered, this translates into a transimpedance gain of ~1.4Kohm, as expected from our simulations, which is relatively high, and it was addressed in the design of the TIA for HPSoCv2. Channel 0 is followed in the chip by a voltage gain stage, and the lower response of channel 0 relative to the other channels is expected, as it arises from the added loaded capacitance associated with the output of the stage. An analogous measurement performed on the cascade of TIA+extra gain stage is compared with the pure TIA output in Figure 7 (right), which shows the linearity of the response as well as an effective gain increase by more than a factor of 4.

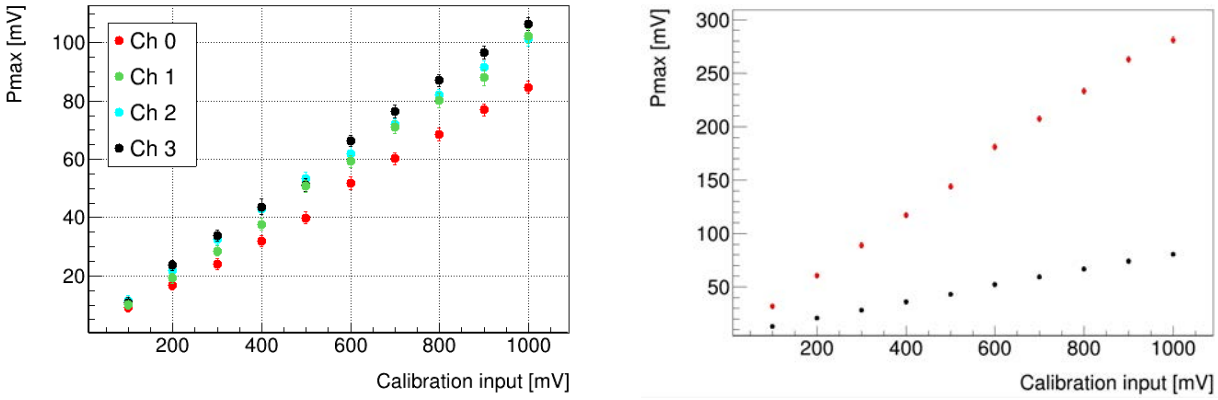

Figure 9. (left) TIA gain measurement. Comparisons of TIA and TIA+VGS on the same input channel - effect of gain stage.

Sideband data from the calibration dataset was used to estimate the noise from the amplifier stage. Figure 8 (left) shows an example of noise measurements corresponding to different impulse levels. The mean values are reproducible and independent of the input, as expected for a pure amplifier noise (as opposed to other types of crosstalk or feedthrough). The RMS value, around 2.6mV, should have the value obtained by measuring the probe and scope by themselves, which is approximately 1.7mV, subtracted in quadrature. This yields a noise level of ~1.7mV, which is higher than expected from simulations. The rise time (20-80%) of the output signal was evaluated at different input levels (Figure 10, right) and is largely independent of input level at ~500-600 ps, consistent with simulation.

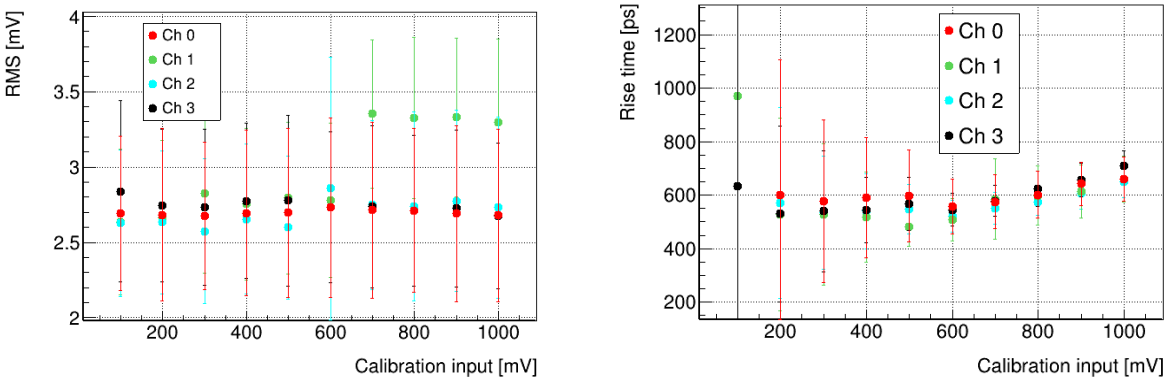

Figure 10. Calibration dataset measurements of (left) TIA noise, and (right) TIA rise time.

Figure 11 (left) shows a typical waveform with a reasonably high voltage peak ~60 mV over baseline acquired using the Sr90 source to excite a minimum-ionizing signal in an FBK AC-LGAD sensor. This would already be sufficient for the HPSoC to identify the deposition and provide precise timing even without the help of a gain stage which can increase the gain by a factor of ~4-5. However, such a gain stage will likely be a necessity for smaller pitch sensors - a proper design of high gain stage was performed as part of HPSoCv2 design. Figure 11 (right) shows the distribution of voltage peak amplitudes for the smaller of the two Sr90 datasets.

Figure 12 (left) shows the distribution of rise times from the “large” Sr90 dataset with a mean of ~540 ps, which is consistent with the expected response of the sensor used. Estimating the time jitter using the ratio between the RMS of the noise and the slope of the rising edge (slew rate), we found a resolution of 1.7mV/(74/546 mV/ps) or ~12.5ps, which is quite encouraging and in line with estimates from simulation for a full input capacitance of 0.4pF.
Some extra information on the topology and testing of the TIAs can be found in [1].

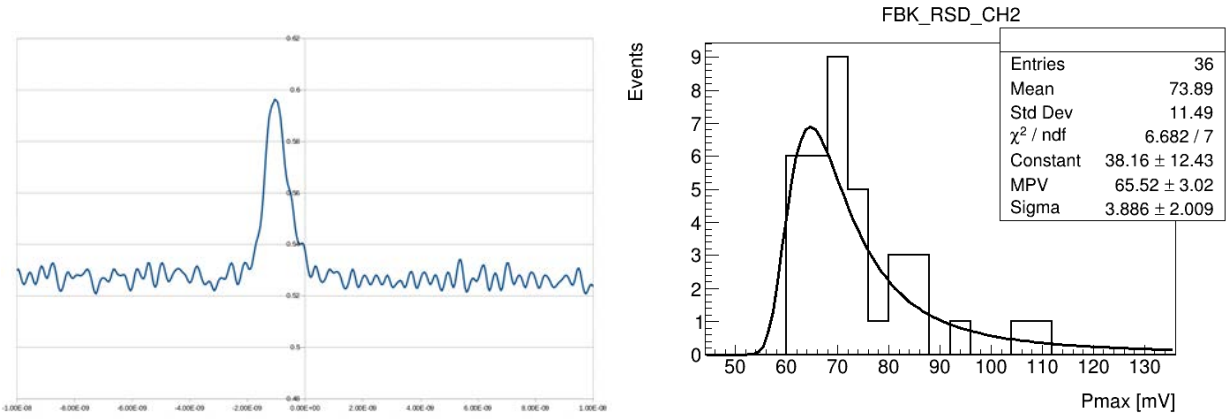

Figure 11. (left) Typical TIA output response (rise time ~540ps); (right) Sr90 AC-LGAD “small” dataset distribution of peak waveform amplitudes.

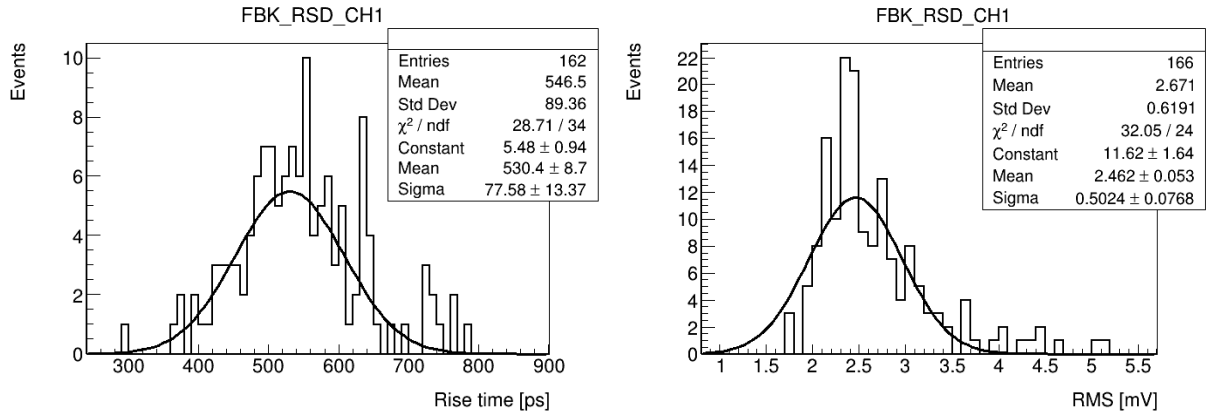

Figure 12. Sr90 AC-LGAD “large” waveform dataset distributions: (left) rise time (~540ps); (right) sideband noise.

JLAB-EIC project - 4-HPSoC

The main outcome for the FY22 effort was the second version of prototyping channels, along with calibration and sensor test results, of the **full four-channel prototype HPSoC chip**, which implements (a) an **optimized front-end design** informed by the testing results from the initial prototype chiplet, (b) a **full digitizer**, (c) on-chip **autonomous operation**, The chip is currently under fabrication and is expected to be shipped back by September 1st. An evaluation **test board**(s) is currently being designed to permit testing **with EIC-specific prototype LGADs** sensor(s) as well as **calibration signals**.

More details on the effort from the 2022 effort can be found in section 4.

1.3. Objectives; institutional areas of responsibility

The overall goal of the multi-year HPSoC project is to design and fabricate a readout chip meeting the specifications given in Table 1, above, and which has been synergistically developed and optimized for use with EIC-specific sensors. The more immediate FY23 goal for which support is sought is to design, fabricate, test and evaluate a first version of the fully integrated hPSoC module containing nine fully autonomous channels capable of (a) self-triggering (b) internal calibration (c) internal feature extraction (d) data packetization and (e) fast data interface. The final FY23 goal is to fully test the new chip integrated with EIC-specific sensor arrays on both the bench and, assuming availability, with beam testing.

Nalu Scientific will be primarily responsible for all HPSoCv3 chip and board design as well as chip fabrication, including, in particular:

- Evaluate and optimize the existing channel performance based on tests performed on HPSoCv2;
- Design a digital backend capable of integrating the information of the 9 channels, an initial feature extraction, packetization and data delivery;
- Fabricate the device;
- Participate in the design of the evaluation test board to accommodate the third prototype chip's use in both calibration input and sensor-based testing;
- Design and implementation of all firmware.

UCSC/SCIPP will be responsible for sensor selection/mounting and testing, including, in particular:

- Guidance on the design of the third iteration of the HPSoC prototype chip as it relates to its application to the Electron-Ion-Collider detector Time-of-Flight system - in particular as it pertains to optimization of algorithm to estimate of time of arrival and spatial positioning, based on the result from the previous chip measurements;
- Participate in the design of the evaluation test board to accommodate use with EIC-specific sensor(s);
- Loading and verification of the modified evaluation test board;
- Characterization of the new HPSoCv3 chip using calibration and sensor data collected through both bench and beam testing, including
    - Confirmation of basic functionality,
    - Overall channel signal quality and noise features,
    - Evaluation of timing performance,
    - Analysis of characterization data as it relates to physics performance.

1.3.1. Work plan

The work plan for FY23 will allow achieving the objectives outlined above to design, fabricate, test and evaluate a first iteration of the fully functional HPSoC 9-channel module with EIC-specific prototype LGADs sensor(s). ***Many elements in the WBS below inherit from the existing HPSoC effort. Each will be reviewed to verify whether any changes and/or modifications are needed in order to best support the addition of the new/enhanced functionality which is the focus of this request.***

WBS 1. Analysis and high-level design of SoC features: Based on the result from the HPSoCv2 prototype measurements, the trade-off between performance achievable with the digitized data and the computational complexity will be assessed and guide an high-level architecture for the chip digital portion. At the same time, the testing will be used to identify existing weak points in the analog implementation and corresponding corrective measures.

WBS 2. Design of the HPSoCv3 9 channel module ("mini-HPSoC"): Based on the result from the HPSoCv2 prototype measurements, an optimized nine-channel self-contained SoC module will be designed and implemented. The following additional elements will be designed for the new chip iteration:

- Module level mechanisms for cross-channel triggering and channel coordination.
- Digital back end for system-on-a-chip elaboration of the digitized data - comprising voltage calibration ("pedestal subtraction"), estimation of timing and charge parameters ("feature extraction")
- Digital backend collecting the information from each individual channel and performing high level combination ("data fusion") as well as packetization and serialization

These elements will be added to the existing design and validated using the existing chip simulation updated for the new elements above, combined with experimental data from readout of the individual channels as obtained from the experiments with HPSoCv2. The current design choices for the following will be reviewed and validated, with modification as needed to accommodate the additional new features. In the interests of economy, simple single channel data flow and extraction, will be implemented to assess the timing accuracy capability of the mechanism (following the experiments as shown in figure 1) - but full data will be allowed with a testing mode, to compare the results with more sophisticated DSP extraction mechanisms to be eventually incorporated.

WBS 3: Integration of test chip, verification and foundry submission

- Chip floorplanning and final layout: Final selection of components and test structures to be submitted. Test Channel assembly, exposed test points and integration with I/O pads
- Functional verification - analog functional model: Analog subsystems in the ASIC are designed and verified with transistor level simulators. Their functions are then represented in chip level simulations with combined structural and HDL (hardware description language) models which are used for whole chip simulations.
- Combined testbench for each chip subsystem: Final simulation verification of the test chip will test the combined analog and digital models' netlists. The simulation is done to ensure proper connections and signal interpretation between the digital and analog domains. This step ensures that each subsystem of the ASIC functions together as intended.
- Full chip layout vs. schematic: The assembly of the test ASIC will require the placement and interconnection of the digital and analog cores' physical layouts and with the IO pads. The entire physical layout will undergo DRC (Design Rules Checking for manufacturability) and LVS (Layout Versus Schematic) to ensure matching of desired netlist structures with silicon devices. DRC and LVS will use commercial tools (such as

Cadence PVS) and foundry provided rules files. This phase concludes with tape-out to the IC foundry fabrication facility.

WBS 4: **Evaluation PCB test board design, fabrication and chip testing:**

- Chip packaging and footprint: After the chip is submitted for fabrication, it is possible to proceed with the choice of package, allowing definition of the chip footprint for the PCB layout. Some fabricated dies will be left unpackaged to allow for direct bonding to LGAD sensors. Due to the complexity of direct bonding, the external interface will be kept minimal (simple serial interface) to minimize the amount of required bonding wires.
- Evaluation PCB test board design: The existing board design will allow the testing of the individual chip channels as well as the cross-channel features (i.e. low level crosstalk, channel to channel timing estimation, charge and position estimation). As needed, the board design will need to accommodate the new prototype chip and/or EIC-specific prototype sensor(s).

All results of testing will be reported in the relevant EIC eRD and detector group(s), and we will additionally report results at conference and/or in instrumentation papers and other documents, such as internal notes and programmatic documents i.e. internal reports, TDRs, etc.

WBS 5: **Firmware Design:** Firmware implemented in an FPGA on the evaluation test board will be required to e.g. configure the chip, provide external triggering, collect and save data at reasonably high rates for the high level tests.

1.3.2. Personnel, performance schedule; support request, deliverables

The Nalu Scientific team will be led by PI Dr. Luca Macchiarulo, Nalu's Senior IC Designer, with additional effort from other staff members with relevant specialized skills, including Sr. Design Engineer Dr. Greg Uehara, Integration Engineer Chris Chock, Physicist and Firmware engineer Dr. Ben Rotter, and CEO Dr. Isar Mostafanezhad. (No support is being requested for Dr. Mostafanezhad.)

The UCSC/SCIPP team will include the PI Prof. Bruce Schumm, faculty emeriti Abraham Seiden and Hartmut Sadrozinski, postdoctoral researchers Dr. Simone Mazza and Dr. Jennifer Ott, and the three technical staff members for whom support is requested here: electro-mechanical technician Forest Martinez-McKinney, and electronic design specialists Max Wilder and Dr. Taylor Shin.

Table 2 summarizes the start and duration for completing the major elements of the WBS. Table 3 summarizes the 100% baseline level of effort, the particular scope addressed and the accompanying resource request for each individual seeking support here. The relative apportionment of funding and effort proposed between Nalu and UCSC/SCIPP is ~75%, 25%, respectively.

Beyond personnel, support is additionally sought for fabrication of the new chip prototype ($18k) and the modified evaluation test board plus procurement of parts required for the board ($10k), along with a small amount of M&S for miscellaneous expenses and travel. UCSC indirect costs are 54% of direct costs, Nalu's effective indirect rate is ~40%. All numbers provided in Tables 3 and 4 include fringe and are fully loaded.

Table 2. Objectives and schedule for FY23, by months 1-12 (F=Fabrication).

FY23 Month Objective	1	2	3	4	5	6	7	8	9	10	11	12	Principle Responsible Part(ies)
WBS 1. Analysis and high-level design of SoC features	X	X											Nalu, UCSC
WBS 2.Design of mini-HPSoC	X	X	X	X	X	X							Nalu
WBS 3. Integration of test chip, verification and submission					X	XF	F	F					Nalu
WBS 4. Evaluation test board design, fabrication						X	X	X					Nalu, UCSC
WBS 5. Testing, reporting of results									X	X	X	X	UCSC, Nalu
WBS 6. Firmware design, implementation						X	X						Nalu

Table 3. Level of Effort, Scope Addressed, Resource Request for each person

	100% Baseline		
Team Member, Institution	**FTE months**	**Request ($k)**	**Function, Scope**
Dr. Luca Macchiarulo, Nalu	2.55	64.5	Principal chip designer, Digital design, lead PI
Dr. Greg Uehara, Nalu	0.75	18	Design, implement analog corrections
Dr. Ben Rotter, Nalu	1.2	30	Design, implement firmware
Chris Chock, Nalu	1.65	30	PCB board design and implementation; chip layout, integration
Dr. Taylor Shin, UCSC	2.25	25.5	Electronic design specialist; PCB board design and implementation
Max Wilder, UCSC	1.29	15	Electronic design specialist; PCB board design and implementation
Forest Martinez-McKinney	0.6	7.5	Electro-mechanical technician; PCB board implementation
Total:	6.86	190.5	

Table 4 provides a line item budget summarizing the total 100% baseline request of 158k in FY23, along with the requested ~80% and ~60% reductions. However, given that a true 40% reduction in the budget would not allow successfully addressing the minimal scope of fabricating and testing any version of a next iteration of the HPSoC chip, a 70% baseline budget is given. Most of the reduction from baseline to 80% is accomplished by reducing the scope of the investigation and implementation of feature extraction algorithms. This will significantly reduce Dr. Macchiarulo's effort and, to a lesser extent, that of Mr. Chock in the integration. The "60% baseline" budget, which is actually ~70% here, further descopes the multi-channel trigger functionality as well as reduces the serial interface streaming to the bare minimum required to verify chip level functionality.

Table 4. Line item budget

Item	100% Baseline Request ($k)	80% Baseline	"60% Baseline"
Chip fabrication	18	18	18
Board fabrication, parts	10	10	10
Nalu personnel	142.5	114	85.5
UCSC personnel	48	38.4	28.8
M&S, travel (trvl only at 100%)	3	1	1
Total:	221.5	181.4	143.3

The main deliverable for the FY23 effort will be the first iteration of the modular nine-channel core for the HPSoC family of chips. Test results based on the prototype chip will be presented and shared with the relevant EIC AC-LGADs detector and other working groups such as e.g. eRD112.

Subsequent to FY23, multiple nine-channel HPSoC modules will be integrated into an ultimate 81-channel full chip composed of a 3x3 array of mini-chips, as shown in the right of Figure 6, which could be available in FY25.

2. Cost effectiveness

Through its localization of the digitization of fast-timing signals from advanced solid-state detectors onto the primary readout ASIC, the successful development of the HPSoC ASIC will significantly reduce the per-channel cost of digitizing and processing information from fast timing sensors. In addition, the development of an ASIC to replace conventional digitization and communication chipsets will reduce reliance on supply-chain disruptions, placing the production and procurement of critical electronics in much tighter control of the scientists and engineers developing and working with fast timing systems.

3. Diversity, Equity, and Inclusion

Both Nalu Scientific and UCSC strongly support the goal of advancing diversity, equity and inclusion. UCSC/SCIPP PI Prof. Schumm is the Director of UC Operations for the inter-segmental Cal-Bridge Program (https://www.cpp.edu/calbridge/index.shtml), currently funded at $5M per year by the California Legislature, that mines the diverse talent of the California State University undergraduate student body, bringing competitively-selected students into close mentoring relationships with UC faculty and cultivating them for admission to graduate school. As a result, SCIPP has access to a significant pool of talented graduate students from historically under-represented backgrounds. Two such students (fourth-year Rene Mora Padilla and second-year Miguel Escobar Godoy) are currently active in the Fast Sensors group that will host the UCSC portion of the proposed work, which would provide significant additional opportunity for their education and professional development.

Nalu's close partnership with the University of Hawai'i since the inception of the company has afforded it opportunities to engage in internships with students and new engineers of under-represented groups in the past and undoubtedly will in the future. Reflecting the State of Hawaii's underlying "majority-minority" demographic make-up, Nalu's workforce has organically developed over the past several years to reflect its naturally diverse environment. In turn, Nalu has the opportunity to provide high-tech mentoring and professional development to

local graduate students participating in UH research groups collaborating with Nalu as well as students from further afield, including both the U.S. and internationally.

4. Progress Report

As mentioned in section 1.2, this project follows the completion of the FY22 contract, and this section describes the activities performed as part of that effort:

1. **Evaluation of the existing pre-amplifier stage followed by design optimizations to improve overall gain and signal-to-noise ratio.**
2. **Design of mixed signal parts from the original design (i.e. ramp generator and distribution, triggering system) to enable independent operation of the channels.**
3. **Completion of self-contained acquisition channel - triggerable acquisition of channels.**
4. **Completion and optimization of simple I/O interface to permit testing of all chip features.**
5. **Integration of components in a single chiplet with four channels, all connected to independent stages, new pre-amplifier for independent testing, full new channel for independent testing - note that** one of the 4 channels has bypassable TIA to permit direct testing of digitization.
6. **Final Verification** and fabrication of the new chiplet.
7. Design, fabrication and population of the evaluation test board.

Steps 1 through 6 have been completed and we are currently performing the design of the evaluation board - we aim to fabricate the board by the time the fabricated samples are shipped (September 1st) and complete the evaluation at Nalu for electronic and digitization testing and at SCIPP for TIA calibration and full chain testing including LGAD readouts.

The features of the designed chip are as follows:

1. 4 channel device
2. Each channel has an optimized front-end with improved TIA performance targeted at AC-LGAD readout
3. Each channel has a waveform digitizer (128x2 samples) following the gain stage:
    a. Digitization at 10 Gsps
    b. Number of converted bits: 10
    c. Note that the original plan had a single group of 128 samples - this was doubled to permit testing of the ping-pong feature to reduce deadtime.
4. Channels can operate independently (i.e. do not require external electronics to perform the digitization)
5. Extra Independent TIA is available for independent testing
6. One channel (number 3) has direct access to the digitizer to test its performance independently of the TIA (original plan had a single separate channel, but the adoption of the 2x128 samples made it impossible to fit in the allotted space and fabrication budget).

Apart of the design effort, new core component had to be designed or redesigned - in particular:

Front end Trans-Impedance Amplifier, redesigned with the objectives of Improving the

Signal-to-Noise Ratio, mostly by boosting gain and noise shaping (for this task we used signal templates from real detectors for simulations) and improve input resistance, which were the main concern for the v1 of the TIA. The submitted design is expected to have a substantial reduction of input resistance (<250ohm DC, ~50 ohm at pulse BW), and adequate gain bandwidth, and expected jitter ~10ps. Figure 14 shows comparison with old TIA and an alternate design that was developed.

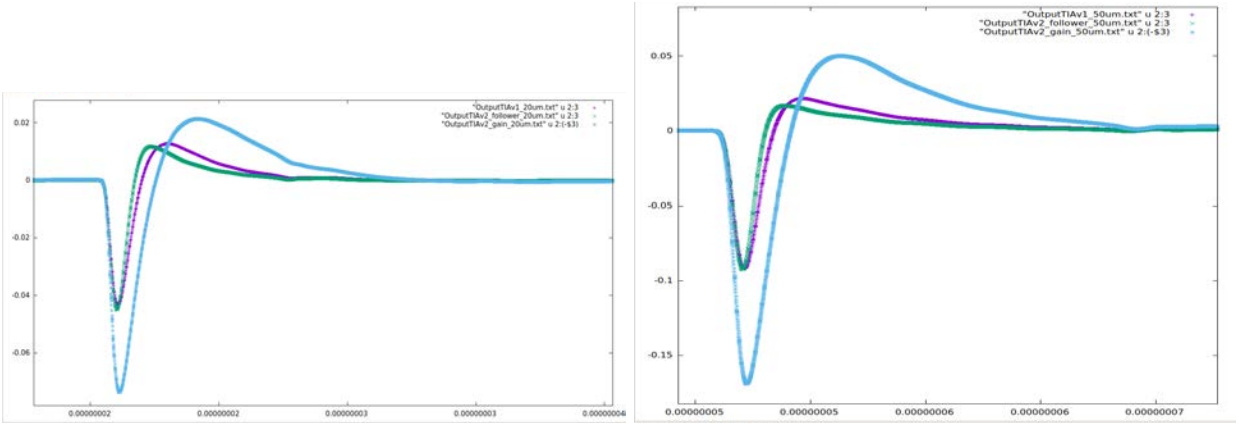

Figure 14: Comparison of simulated response of TIA candidates to expected 20 and 50 um thick AC-LGAD sensor output - Green: tinyHPSoC; purple: New TIA plus voltage follower, blue: New TIA plus optimized gain stage)(selected topology)

Ramp Generator: For this part we explored different architectures - (through simulations), 1. Simple mirror (default/baseline), 2. Cascode mirror, 3. Low overhead cascode mirror, 4. triple cascode - the latter architecture was chosen and a range matched with the input as expected (0-0.6V). Furthermore, it was decided that it was possible to incorporate an individual ramp generator per channel, which in turn reduces the need for buffering due to the relatively limited number of samples load (256).

Triggering system: The design of a channel discriminator turned to be tricky as the self triggering needs to be able to respond to the rapid and relatively weak signal from the AC-LGAD output - after a few attempts a design was converged on that incorporated a novel mechanism to impose a self-threshold set-up with sensitive 3 stage differential pair architecture - for simplicity this was targeted for the expected signal polarity.

The digital control was organized as follows: The device is continuously sampling in a group of 128 samples (a “bank”) and it switches to sampling to a second “bank” at the arrival of a trigger. The after also automatically starts a digitization of the “frozen” bank. This permits acquisition of multiple hits without deadtime and high rate processing.

For the triggering dual operation is possible:

- “*Manual*” - with external control of digitization, readout and Banking control, to facilitate testing of low level features of digitizer
- “*Automatic*”:

- Uses a trigger to: 1. Switch sampling to secondary bank if not in use 2. Perform full window (128 samples) digitization. 3. Export data using serial interface.
- Triggers can be external (all channels) or internal (individual discriminator).

The entire digital design was placed and routed by hand to guarantee symmetrical routing for the timing critical bank switching.

Note that the final HPSoC design requires a more complex digital operation to permit calibration, feature extraction and data fusion. Such mechanisms will be studied and implemented as part of the new project performance (i.e. this proposal), but the existing core self-triggering logic, if proven successful, will be largely incorporated within the new digital partition.

A picture of the layout submitted for fabrication is shown in figure 15.

Figure 15. tinyHPSoC layout as submitted for fabrication - the entire die, including I/O pads on 3 sides, occupies an area of 1.5mmx1mm.

5. References

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