Title: R&D of 4D Detectors with EICROC and AC-LGAD at EIC consolidating a US-Japan Consortium

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Japanese Collaboration Members			
Number	**Name**	**Institution**	**Position**
1	Kenta Shigaki	Hiroshima University	Professor
2	Satoshi Yano	Hiroshima University	Research Assistant Professor
3	Yoshiyuki Miyachi	Yamagata University	Professor
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PROJECT SUMMARY/ABSTRACT

One promising technology for 4D detectors is the AC-coupled LGAD (AC-LGAD), which has emerged as a prime candidate for applications at the Electron-Ion Collider (EIC). This technology has been a candidate for Barrel and forward Time-of-Flight and Far forward detectors. However, developing suitable readout electronics to harness the fast-time and fine-pitch capabilities of AC-LGAD sensors remains a significant technological challenge. The BNL team has successfully demonstrated the readout of AC-LGAD prototypes using the ALTIROC fast-time ASIC, originally designed by IJCLAB/Omega for the ATLAS experiment at the HL-LHC. In collaboration with the BNL team, the same partners have developed the EICROC chip, an evolution of ALTIROC with a pixel pitch of 500 x 500 μm^2. Japan has also been a key player in the AC-LGAD sensor development, through the efforts of KEK, HPK Photonics and a US-Japan Cooperation project with FNAL, BNL and UCSC-SCIPP. Japan aims to expand its expertise in the readout electronics, in order to take significant roles in the building of future collider experiments. As a result, a thorough testing of its performance with different sensors combined with the latest version of EICROC is necessary.

This project aims to establish a long-lasting collaboration between the United States and Japan and foster workforce development in Japan. In the short term, the project focuses on characterizing the EICROC chip using custom-made test boards provided by BNL in collaboration with IJCLAB/Omega. The chip will be tested with AC-LGAD sensors fabricated at BNL and by Hamamatsu, featuring different geometries (e.g., pixels and strips of varying dimensions) and fabrication processes (sensor capacitance, resistivity). The obtained results will be shared with the EICROC designers and will lay the foundation for designing and prototyping new chips that meet the performance requirements of next-generation AC-LGAD-based 4D detectors.

Additionally, this project plans to utilize several HPK sensors fabricated in previous fabrication campaigns, leveraging other funding sources, and then contribute to a new HPK submission for sensors with geometries and processes that are dedicated to EIC and include improvements informed by the simulations and studies carried out with sensors from an older batch.

Furthermore, the project will leverage the BNL expertise and unique capability of having a full chain of sensor+ASIC+prototype readout device, and host Japanese students/postdocs for short-term visits, training them on the technology and facilitating technology transfer. The project will also aim to expand Japan's involvement in ePIC and detector two at the EIC, to strengthen the collaboration and to secure future participation of Japanese researchers.

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Project Narrative

1.0 Background/Introduction

The Electron-Ion Collider (EIC) is a high-priority project for the US and the international nuclear physics (NP) and high-energy physics (HEP) communities. It is an excellent frontier for technology development through fostering collaboration and coordination among different research communities and institutions to advance the detector R&D program [1]. One promising technology for 4D detectors is the AC-coupled LGAD (AC-LGAD), which has emerged as a prime candidate for applications at the EIC and other future colliders. These devices provide excellent timing resolution as well as fine spatial resolution, which are crucial for improving the performance of future or upgraded detectors such as Roman Pots, Forward and Barrel Time-of-Flight for the ePIC detector at the EIC, as well as strong candidates for a possible second detector at the EIC. Resistive Silicon Devices, such as AC-coupled Low Gain Avalanche Diodes (AC-LGADs) sensors, are best suited for this purpose as they allow us to achieve fine segmentation of devices down to a pitch size of tens of microns while maintaining tens of pico-second-level timing performance [2-3]. For the front-end-electronics (FEEs), Application-specific Integrated circuits (ASICs) are designed to have small enough contribution to the timing resolution and to handle the finer granularity of the sensor design. Significant R&Ds have been ongoing in the areas of sensor and FEEs, and BNL has played a leadership role [4]. DOE has invested in recent years in the R&D for 4D detectors, and are now leading the community in the AC-LGAD technology in the US. Japan, through KEK, HPK Photonics and a US-Japan Cooperation project with FNAL, BNL and UCSC-SCIPP, has also a leading role in the AC-LGAD sensor development, and wants to grow in the area of the readout electronics in view of taking major roles in the construction of future collider experiments. However, there is a need for workforce development in Japan to provide the necessary impetus for increasing participation in ePIC and a possible second detector at the EIC. There is no current funding available for such training and workforce development. This proposal aims to initiate a primary effort in this direction by identifying areas of research on 4D detectors, joining forces to perform R&D in the US, hosting Japanese students/postdocs and training them on the technology, and facilitating technology transfer. This proposal will also expand our knowledge and expertise to Japan and strengthen international collaboration in this area.

1.1 The development of 4-dimensional sensors (AC-LGADs)

Thanks to the invention of novel sensor technologies, a great effort has been dedicated to developing 4-dimensional (4D) detectors in recent years, achieving a few tens of picoseconds in the time resolution domain [5]. A bottleneck for the implementation of such technologies in a large-scale collider experiment is now the development of readout electronics that can match the sensor performance in both time and space domains. Among such transformative sensor technologies, the Low-Gain Avalanche Diodes (LGADs) [6] are silicon sensors engineered for the fast detection of minimum ionizing particles (MIPs). They are built on thin silicon substrates (20 - 50 μm) and, thanks to the presence of a gain layer that multiplies the signal by a factor of a few tens, they can achieve a timing resolution of about 30 ps or less [7-9]. Since their introduction, the interests in the HEP community has grown, as detectors based on LGADs will constitute the High Granularity Timing Detector (HGTD) [10] and MIP Timing Detector (MTD) [11] upgrades of the ATLAS and CMS experiments at the HL-LHC, respectively. However, to achieve a uniform multiplication in most of the area and a high fill factor, the pad pitch must be far greater than the substrate thickness, therefore, pixel or strip pitches in the order of ~100 μm are not achievable in LGAD technology [12]. To overcome this severe limitation, the AC-LGAD concept was developed [13–17], in which the signal is capacitively induced to metal electrodes placed over the active area but separated from it by a thin dielectric film made of silicon oxide or nitride (see Fig. 1).

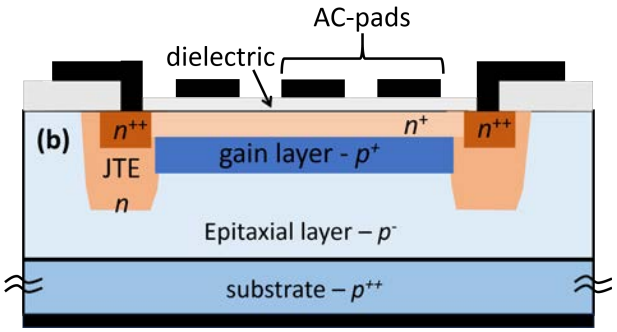

FIG. 1: Section of a segmented AC-LGAD (not to scale). It shows the gain layer (p+), the (resistive) n+ layer that ends in a n++ implant that provides the DC-connection and is embedded in a deep implant called the Junction Termination End (JTE), the dielectric layer that provides the AC-coupling between the bulk and the electrodes, as well as the electrodes (AC-pads) and the passive substrate (p++).

One of the consequences of the AC-coupling of signals in AC-LGADs is that the signal is shared among neighboring electrodes. Such a property was demonstrated to provide precise spatial resolution in the order of few microns with sparse electrodes [18-20]. Such good spatial resolution results from the interpolation of signals shared among several AC-coupled electrodes. This signal-sharing feature makes AC-LGADs first-class candidates and the most advanced silicon technology for 4D detectors, especially for EIC that have low event occupancy, in addition to low radiation levels. The most significant limitation for the broad use of AC-LGADs in scientific applications is the lack of ASICs that match the precise spatial and time resolution of AC-LGADs.

The characterization studies of LGAD and AC-LGAD sensors have been performed so far on custom-made test-boards, designed for the evaluation of a small quantity of sensors. These readout test-boards are based on discrete electronics which are not optimized for power dissipation and can only read out a limited number of channels through the aid of an external fast oscilloscope. For large-scale, multi-channel systems targeting 4D tracking, it becomes clear the need to evaluate the AC-LGAD performance when coupled to higher-complexity readout systems. For example, in the EIC experiments, the AC-LGAD is the sensor baseline to be used in the Time-of-Flight (TOF) and Roman Pots detector [21]. The readout in such a detector will be based on a chip, named EICROC, tailored to match the features of an AC-LGAD pixel sensor with pixel size of 0.5 mm×0.5 mm. The EICROC is based upon an existing readout ASIC designed for the ATLAS HGTD - ALTIROC [10, 22-23] - but features a pixel size almost 7 times smaller than that used in the HGTD (or the MTD).

The BNL team recently demonstrated that the ALTIROC [24] can read out AC-LGADs and preserve their signal characteristics for example the signal sharing and allow fast and precise tracking. The ALTIROC chip performance in reading out a BNL-made AC-LGAD sensor was tested with beta particles from a ^{90}Sr source and an infra-red (IR) laser (see Fig. 2).

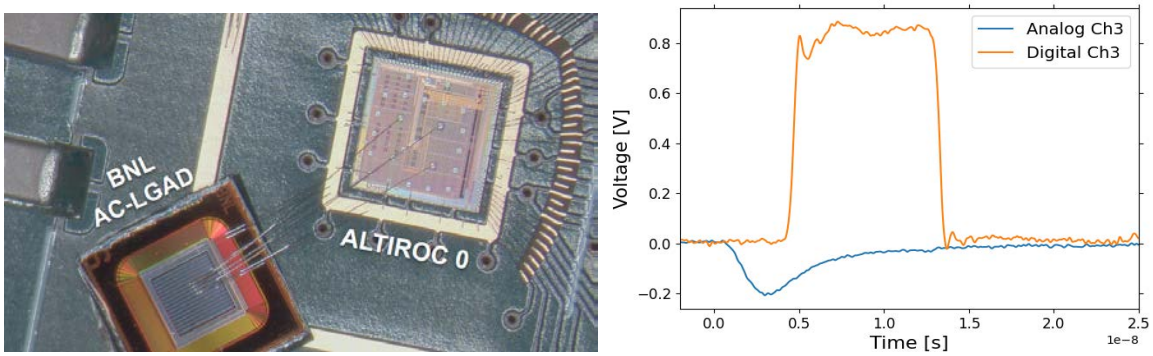

FIG. 2: Photo of a BNL-made AC-LGAD sensor with 4 electrodes wire-bonded to the ALTIROC v0 ASIC, mounted on a discrete test-board designed by FNAL (left). The analog and digital outputs of one channel of the ALTIROC v0 chip are when infrared laser light is injected in the AC-LGAD (right).

While designed to acquire DC-coupled signals from LGAD sensors, the ALTIROC proved to be a suitable readout for bipolar AC-coupled signals generated in an AC-LGAD. Characteristics of the readout signals such as pulse shapes (e.g. amplitude and widths) are compatible with those measured with test-boards and with previous ALTIROC results obtained for standard, i.e. DC-coupled, LGADs.

The particle physics community is investigating several AC-LGAD designs for different applications. For example, fine pixel and strip pitches are studied for application in high occupancy environments, such as hadron or muon colliders; large-pitch stips are considered for low-occupancy experiments, such as those like EIC Time-Of-Flight; a thin active bulk (20 μm) is studied to improve the time resolution to levels below 20 ps; long strips, in the order of the centimeter, are considered to reduce the number of readout channels and power dissipation thus costs in low occupancy environments; large pads of few cm^2 area are also considered for several applications including 4D calorimetry; the resistivity of the n+ layer is optimized to either maximize or minimize the signal sharing, depending on the application etc. (see Ref [25] for a short overview). While the precise specifications of 4D detectors at future collider experiments are still to be determined, an in-depth understanding of the limits of the current technology is a condition to the development of detectors that are capable of fulfilling the physics performance of future experiments.

The positive results obtained by the BNL team with the ALTIROC are a stepping stone for the development of novel types of readout chips that are tailored to match AC-LGAD signal properties, aimed at 4D reconstruction of particles. The EICROC chip was developed by the same group, led by IJCLAB/Omega (Paris, France), who developed the ALTIROC chip and is based on the same process. The EICROC has the potential to spearhead the development of the readout electronics for 4D detectors, but thorough performance studies are needed to establish its compatibility with different AC-LGAD designs and to possibly modify its design to expand its range of applicability.

1.2 The EICROC chip

The primary purpose of the EICROC ASIC is to read out an AC-LGAD for the EIC Roman Pots, i.e. with a pitch size of 0.5 × 0.5 mm^2 with a time resolution of 30 ps and power dissipation of about 1 mW per channel. To minimize costs and maximize the acquired expertise, the TSMC 130 nm CMOS process will be used as for the ALTIROC. The current design foresees a precise time measurement (Time-Of-Arrival or TOA) with a Time-to-Digital-Converter (TDC) combined with an ADC (Analog Digital Converter) for the amplitude measurements, see Fig. 3.

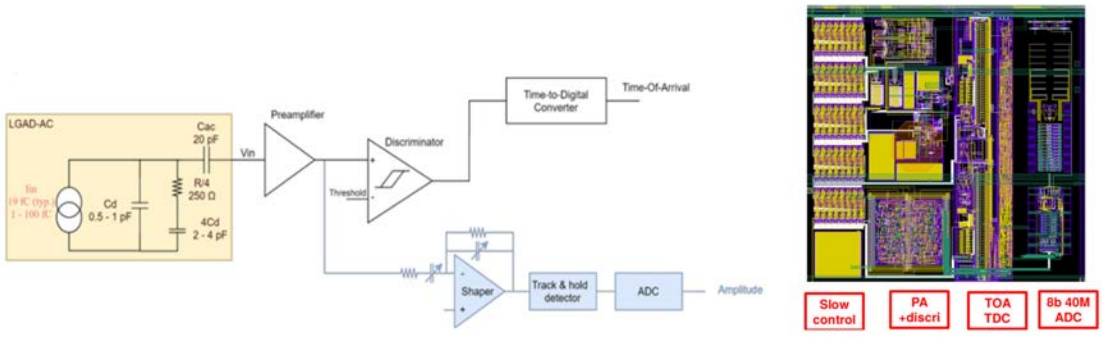

FIG. 3: Schematic architecture (left) and design (right) of one channel of the EICROC0 ASIC prototype dedicated to the readout of an AC-LGAD sensor. A TDC is used to measure the time-of-arrival of the charge and an 8-bit ADC measures the amplitude of the charge filtered by a shaper step.

The signal amplitude measurements are necessary to exploit the signal sharing among sensor electrodes and in turn improve the space resolution to the 20-micron-level (well beyond the typical digital resolution in pixel detectors that is the pixel size divided by √12). The development of the EICROC relies on complementary teams with expertise in micro-electronics, instrumentation and semiconductor detector

characterization from French institutes (IJCLab, CEA-Saclay/Irfu/DEDIP and OMEGA) and from BNL that is involved in the design of AC-LGAD sensors for EIC.

One challenge is the reduction of the power per channel to a fraction of mW to minimize costs associated to cooling, while ensuring GHz bandwidth, ultra-low noise (< 1mV) for the frontend, picosecond accuracy in the TDCs and good signal-to-noise ratio at the ADC level. In addition, fitting the current electronic blocks in a smaller pixel area represents a second challenge while maintaining their performance. Therefore, the development of a pixel-like ASIC with a few picoseconds timing accuracy represents a technological challenge and requires several iterations that have to be carefully characterized.

A first version of the EICROC chip, named EICROC0, has been designed and fabricated in 2022, see Fig. 4 (left). It is a 4 × 4 channel test-chip with a pitch size of 0.5 × 0.5 mm^2 based on ALTIROC front-end (TZ pre-amplifiers), a TDC and an 8-bit ADC. The TDC is used to measure the TOA of the charge and an 8-bit ADC measures the amplitude of the charge filtered by a shaper step. The TDC was optimised in terms of dynamic range and resolution as well as spatially optimized to fit within a pad of 0.5 × 0.5 mm^2. It also implements a I2C slow control and a digital readout with FIFO depth of 8 (200 ns). Five slow control bytes per pixel are used: 6 bits for local threshold, 6 bits for ADC pedestal, 16 TDC calibration bits, and several on/off and probes. To achieve an excellent time resolution, any coupling between the sensor input and the digital electronics activity in the ASIC or the bias voltage connection (inductance) needed to be carefully controlled, which implied constraints on the module design.

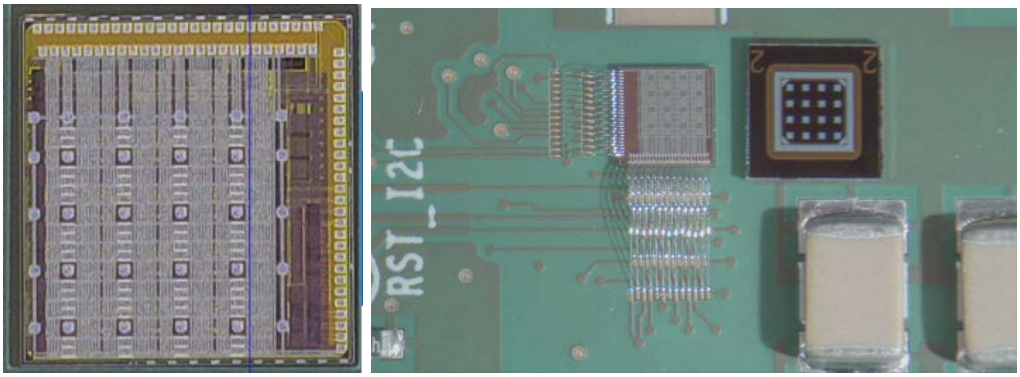

FIG. 4: Photo of the EICROC0 (left) and of a Carrier Board mounting a wire-bonded EICROC0 and an AC-LGAD sensor (right). The AC-LGAD in this photo was not wire-bonded for testing purposes.

The purpose of EICROC0 is to evaluate the readout of AC-LGAD sensors with a dedicated test-bench. Table 1 summarizes the EICROC targeted specifications as well as those of the ALTIROC as a reference.

TABLE 1: Comparison of specifications of the EICROC and the ALTIROC.

	ALTIROC	**EICROC**
Sensor Type	LGAD	AC-LGAD
Pixel size [mm^2]	1.3x1.3	0.5x0.5
Pixel thickness [µm]	50	50
Pixel capacitance [pF]	4	0.5
MIP equivalent charge [fC]	5-20	10
Power per channel [mW]	5	1

TDC Least Significant Bit [ps]	20	12
Threshold [fC]	4	2
Bandwidth [MHz]	800	800
TDC (ToT)	8 bits/10 bits	-
ADC	-	8 bits @40 MHz

A printed circuit test-board (Carrier Board) associated with the EICROC0 was designed by OMEGA. Such a board is used for characterizing the EICROC0 together with an AC-LGAD. The main components are level translators (1.2V and 2.5V), on-board regulators for low voltage, 4 SMA connectors for pre-amplifier signal output. Space has been left near the chip location to accommodate for one or two AC-LGAD sensors wire-bonded to the chip. Pictures of an EICROC0 chip placed on the bare printed circuit board are shown on Fig. 4 (right).

FIG. 5: Picture of a bare Carrier Board connected through FMC connector to a Xilinx ZC706

In order to control the parameters of the system, a commercial Xilinx ZC706 (Interface Board) is used, and a dedicated firmware has been developed at IJCLab. The connection between the Interface Board and the Carrier Board is made through a FMC connector. A picture representing a bare printed circuit board connected to the Xilinx ZC706 is shown on Figure 5.

The BNL team, leveraging an on-going collaboration with IJCLAB/Omega team for the EIC Roman Pots (eRD112 project), has assembled four EICROC0 chips on Carrier Boards provided by IJCLAG/Omega. Two of these boards also have a BNL-made AC-LGAD sensor attached. These assemblies will be used at BNL, IJCLAB and Omega for preliminary tests of basic functionalities of the EICROC0 chip. The testing of EICROC0 is still at a very early stage, and careful studies require a major effort. A design, named EICROC1, is expected to take place in 2023 to implement a low-power ADC, and a full size 32×16 ASIC. An in-depth characterization of the EICROC0 functionalities is critical before the EICROC1 design is completed. In this early phase of testing, the feedback on the compatibility of such an ASIC with a range of AC-LGAD designs is also very important as it will guide the designers towards a more flexible chip that can match the requirements of future EIC detectors like TOF and Roman Pots.

2.0 Objectives

The project aims at establishing a long-lasting collaboration between the US and Japan on the development of readout electronics for 4D detectors for EIC applications. More specifically, within the time-scale of this project the immediate goal is to study and expand to several future detector applications of the currently most advanced ASIC - EICROC - that is being developed for the AC-LGAD sensor readout. Such an ASIC has had the limited scope of providing the readout for the EIC Roman Pots that require 500x500 μm^2 pixels with 30 ps time resolution, but its current specifications may be compatible with other types of AC-LGAD sensors, e.g. strips etc. It has also been proposed to be a candidate for the barrel and forward TOF. In addition, its design is sufficiently flexible that slight modification will make it compatible with a variety of other sensor geometries and processes.

3.0 Proposed Research and Methods

The requirement to develop TOF and Roman Pot detectors for EIC and a variety of future colliders urges the US and the international community, including Japan, to strengthen R&D on sensors and their associated readout electronics. Recent research on silicon sensors has resulted in several technologies that can meet a vast range of performance specifications for future collider experiments. Among these technologies, the most advanced is the AC-LGAD. While great progress has been made in characterizing AC-LGADs, their implementation in any collider experiment is limited by the readiness of readout electronics that match the AC-LGAD potentials for unprecedented resolution in time (15-20 ps) and space (micron-level) domains. This project aims at utilizing the AC-LGAD sensor technology as the baseline for future 4D detector developments, and leveraging an experienced team of ASIC developers for timing applications to expand the scope of an advanced ASIC prototype - EICROC - that is being developed for the EIC Roman Pots. BNL and DOE have invested in recent years in the R&D for 4D detectors, and are now leading the community in the AC-LGAD technology. Japan, through KEK, HPK Photonics and a US-Japan Cooperation project with FNAL, BNL and UCSC-SCIPP, has also a leading role in the AC-LGAD sensor development, and wants to grow in the area of the readout electronics in view of taking major roles in the construction of future collider experiments such as EIC. This project aims at forming an US-Japan Consortium that leverages the specific expertise of the BNL team on AC-LGAD sensors and the existing collaboration between BNL and the developers of the EICROC ASIC to enable the Japanese colleagues to strengthen their effort on 4D detector R&D, and specifically on the readout, exploiting their historical strengths in silicon detectors for tracking applications as well as the main producer of silicon sensors, i.e. HPK Photonics.

The Consortium will study and characterize the performance of the EICROC chip with AC-LGAD sensors fabricated by both BNL and the Japanese vendor HPK. The sensors will feature different geometries and processes with the goal of testing the range of applicability of EICROC as a function of sensor properties: e.g. a) pixels vs strip electrodes, b) strips with different lengths (1 mm to 2 cm) and metal sizes (i.e. with different detector capacitance), c) sensors with different active thicknesses (20-50 μm), which affect the sensor readout speed and time resolution (expected to reach 15-20 ps with 20 μm active thickness), d) sensors with different resistivities of the n+ (resistive) layer, which affects the signal sharing between electrodes and in turn the spatial resolution, e) the AC-coupling of the sensor bulk to the electrodes etc.

The Japanese side of the Consortium will study sensor designs using TCAD simulations and feed this information to HPK for future fabrication. The laboratory tests will start from stand-alone validation of the ASIC channels. The ASIC will be wire-bonded on the Carrier Board and its characteristics will be studied using a calibration charge injection and an internal capacitance mimicking the sensor's one. The main steps are the determination of the lowest threshold of the discriminator, the noise measurement and efficiency as a function of the charge. The TDC quantization steps will be measured by shifting the input calibration signal with a precise delay and the jitter extracted as a function of the charge. By injecting different charge inputs, the ADC quantification step and the ADC non-linearity will be extracted. The signal-over-noise at the output of the ADC is also a key measurement. As a second set of tests a sensor will be connected at the input of the ASIC through wire bonding and then through bump bonding. The sensor voltage will also be supplied in order to deplete the sensor. This characterization of the system is a cornerstone step before starting to look at real energy deposits in the sensor as quite often integration issues/coupling are observed.

Finally a module is characterized with realistic energy deposits from particle beams. Such tests will include measurements of charge collection and time resolution using beta particles from a ^{90}Sr source, as well as an infrared pulsed laser light (1056 nm). The IR laser will also allow the measurement of the charge sharing between neighboring electrodes benefiting from a precise location of the light injection. Test-beams at the FNAL Test-Beam Facility (FTBF) with 120 GeV protons and at ELPH with GeV-photons in Japan are foreseen. They allow the accurate characterisation of the time and space resolution of the modules.

Several of these tests will initially be conducted at BNL within the scope of the R&D for the EIC Time-of-Flight and Roman Pots. The Japanese institutes in the Consortium will replicate the test systems at BNL to expand the scope of these tests for future collider experiments, and will characterize the functionalities of the EICROC with AC-LGADs produced by HPK, with a variety of geometries and fabrication processes, as listed above. The involvement of HPK in this project is a major asset for any future collider experiment, as it guarantees sensor quality and large production volumes for large-scale 4D detectors. This project plans to utilize several HPK sensors fabricated in previous fabrication campaigns, leveraging other funding sources, and then contribute to a new HPK submission for sensors with geometries and processes that are dedicated to EIC and includes improvements informed by the simulations and studies carried out with sensors from an older batch.

The results of these studies of EICROC chip performance with HPK batches of AC-LGADs will be made public to the international community through peer-reviewed publications and presentations at conferences and workshops. In addition, the Consortium will everage the already close collaboration between BNL and IJCLAB/Omega to feedback the results of such studies to the ASIC designers such that they can implement suggested changes in future designs, e.g. EICROC1 and EICROC2, which are scheduled for the next few years.

BNL and the Japanese institutes are in a unique position of bridging the gap between HEP and NP and other fields of science, thanks to their leadership roles in LHC, HL-LHC, RHIC and EIC.

4.0 Timetable of Activities & deliverables

The project scope is limited to one year and the activities and deliverables are uniquely assigned to the various institutes of the Consortium. More specifically, BNL will provide the EICROC chips, the Carrier Boards and their components, and will assemble them together with the AC-LGAD sensors provided by Japan (HPK). Only preliminary sets of mechanical and electrical tests are carried out at BNL, while the in-depth characterization of the EICROC + AC-LGAD modules will be carried out in Japan. Here follows the list of deliverables and timescale of the work, expressed in months from the start of the project.

BNL deliverables:

- By leveraging on-going collaboration with IJCLAB/Omega, BNL will provide EICROC chips and Carrier Boards for the equivalent of 10 modules (Month 1),
- By leveraging on-going collaboration with KEK and HPK, BNL will provide a set of existing AC-LGAD sensors produced by HPK for the equivalent of 5 modules (Month 1),
- BNL will assemble 5 modules: EICROC chips by IJCLAB/Omega and AC-LGAD by HPK on IJCLAB/Omega Carrier Boards, including wire-bonding (Month 2),
- BNL will carry out basic functionality tests of such 5 modules, and 4 of them will be sent to Japan for in-depth characterization, while 1 will be kept at BNL for testing (Month 3),
- BNL will train Japanese colleagues how to install the equipment and readout software and firmware (Months 2-4), as well as how to operate and test the devices (Months 4-8),
- BNL will produce 5 additional modules with a new batch of AC-LGAD sensors produced by HPK specifically for this project (Months 8-10).

Japanese deliverables:

- The Japanese side of the Consortium will set up the equipment as well as software and firmware (Months 2-4),
- They fully characterize the BNL-made assemblies of EICROC + AC-LGAD using available HPK sensors (Months 4-10),
- TCAD simulation studies of AC-LGAD geometries ad processes (continuing effort),
- They will join an HPK submission (Months 6-8) to produce more AC-LGADs to be tested with a

new and improved version of EICROC, named EICROC1, that is expected in 2023.

- They will fully characterize the 2nd batch of modules made by BNL with the 2nd batch of HPK sensors (Months 10-12).

Both the US and Japanese sides of the Consortium will share the following deliverables:

- Participation in test-beams at the FTBF and ELPH (schedule depends on beam-time availability).
- Dissemination to the broad particle physics community of the results, i.e. the range of applicability of EICROC chip, and feedback to EICROC developers for improvements to make EICROC more flexible for other applications, beyond EIC Roman Pots (Months 10-12).

5.0 Project Management Plan:

The BNL PI, Prithwish Tribedy and Alessandro Tricoli, will coordinate the activities at BNL, i.e. the work of technicians for the assembly of test-modules, students and postdocs for testing the modules before they are sent to Japan. Tribedy and Tricoli will also supervise the Japanese student or postdoc who will be sent to BNL for an extended period to familiarize with the system test and the data-taking operations. The student/postdoc will in turn function as technical liaison between BNL and Japan for the setup and operation of the system test in Japanese institutes. They will also serve as liaison between US-Japan Consortium and the IJCLSB/Omega team to acquire EICROC chips, Carrier Boards and bi-directional communication of findings and results.

The PI in Japan, Kenta Shigaki, will coordinate the activities in Japan, i.e. scheduling meetings, consolidate information, and be in charge of discussions regarding sensors to HPK.

A mailing list will be created with all participating members and e-mail exchanges will be used as the main means of communication on a weekly basis. Monthly virtual meetings will be arranged between the members of the Consortium to discuss the progress of the activities.

6.0 Separate Institutional Responsibilities

US - BNL:

- Acquiring of EICROC chips and Carrier Boards from IJCLAB/Omega,
- Assembly (gluing and wire/bump-bonding) of EICROC chips and HPK's AC-LGADs on Carrier, Boards, i.e. modules,
- Test of basic functionalities of modules before shipments to Japan,
- Instruct Japanese colleagues how to set up system tests in their institutes,
- Train Japanese student/postdoc on module testing,
- Liaison with IJCLAB/Omega and their ASIC designers.

Japan - Hiroshima:

- Coordinate the activities in Japan.
- Learn how to set up system and module tests.
- Test and evaluate strip modules with different geometries and processes.
- Study sensor designs using TCAD simulations and feed the information to HPK.

Japan - Yamagata:

- Learn how to set up system and module tests.
- Test and evaluate pixel modules with different geometries and processes.

Japan - RIKEN:

- Lead discussions regarding the submission of sensors to HPK.

Japan - Shinshu:

- Prepare and be responsible for the test beam in Japan.

7.0 Budget Justification

Labor - Senior/Key Personnel ($26,938)

Dr. Prithwish Tribedy (0.06 FTE) and Alessandro Tricoli (0.06 FTE) will lead the proposed research including all experimentation, publication and presentation of results and supervision of postdocs, students, and technicians.

Labor - Other Personnel ($17,461)

A technician from BNL's Instrumentation Division (Enrico Rossi) will be supported at 0.06 FTE level, corresponding to $7,112, over the course of the 1 year period. His duties will include testing on probe-stations the sensors before they are used for module assembly (i.e. including the attachment and bonding of an EICROC chip and an AC-LGAD sensor on the test-board), and preliminary testing of test-board functionalities prior to module assembly as well as after mounting an EICROC chip and then an AC-LGAD sensor.

Labor for the module assembly by the Interconnect Laboratory in BNL's Instrumentation Division, led by Donald PInelli and Antonio Verderosa, is estimated at 0.06 FTE for a total of $7,112.

An undergraduate summer student (0.2 FTE) and a graduate internship student (0.3 FTE) are expected to be selected and participate in the testing, data-analysis, and presentation of the results at no cost for this project as other funds will be leveraged.

Salaries at Brookhaven National Laboratory are defined in labor bands which include fringe.

Equipment Description ($8,000)

A high voltage power supply to bias the AC-LGAD sensors (Keithley 2410) at a direct cost of $8,000.

Travel ($7,000)

A trip from Japan (RIKEN and Hiroshima) to the US for Japanese colleagues is about $4,000.

A trip to FNAL to participate in a week-long test-beam is foreseen at an estimated cost of $3,000.

Estimates are based on prior travel experience and standard GSA rates.

Participant/Trainee Support Costs ($40,000)

Support for Japanese colleagues to visit and stay at BNL for housing and per diem.

<u>Other Direct Costs</u>

Materials and Supplies: ($18,800)

The AC-LGAD sensors will be provided by the Japanese colleagues, utilizing the Japanese HPK vendor. Therefore, no funds are requested for sensors from the US side of the Consortium.

For conducting preliminary testing of the modules, prior to sending them to the Japanese colleagues, several materials and supplies are needed, as detailed below.

Two commercial Xilink ZC706 evaluation boards, at the direct cost of $3,400 each, one needed for preliminary testing of the modules at BNL, another $3,400 to set up the lab in Japan for a total direct cost of $6,800.

BNL will purchase for the whole Consortium all the EICROC test-boards (also known as Carrier Boards) that are designed by IJCLAB/Omega. It is estimated that 2 boards will be used at BNL, while 8 will be sent to Japan, i.e. 2 per institute. The estimated total cost is $5,000. Please note that each Carrier Board can host up to 2 sensors to allow for more sensor testing with a single board.

For the readout of the EICROC chip a laptop computer running Windows is needed at BNL. The cost is estimated to be about $2,000.

Several consumable parts are expected to be needed, such as connectors, cables, electrical and mechanical components for connecting and testing the modules. Such consumables are estimated at the level of $5,000.

Publication Costs:

No cost.

Consultant Services:

No cost.

ADP/Computer Services:

No cost.

Subawards/Consortium/Contractual Costs:

None.

Equipment or Facility Rental/User Fees:

None. (Other sources of funds will be leveraged to use the FNAL Test Beam Facility for testing the modules with a 120 GeV proton beam.)

Alterations and Renovations:

None.

Other:

None.

Other Indirect Costs

BNL charges Overheads utilizing a Value-Added-Base (VAB) method, which includes Organizational Burden, Procurement Burden, Common Support Burden, G&A Burden, and LDRD Burden.

Organizational Burden: ($3,206) This expense covers the costs for departmental management, financial and business management support services, environmental safety and health facility support services, and the cost for electric power.

Procurement Burden: ($1,358) Calculated for total materials, subcontracts, and travel.

General and Administrative (G&A) Overhead ($26,503) is assessed on all BNL research activities as a percentage rate against a calculated value-added base. G&A consists of the following segments:

Common Institutional G&A which is $21,449

Traditional G&A which is $5,054

Laboratory Directed Research and Development (LDRD): ($3,320) Is assessed on the total project cost at a rate of 3.0%

Total Budget: $152,585

8.0 Three budget scenarios

TABLE 2: Budget Allocations by Institution and Scenario

Name	Institution	FY2024 Nominal	FY2024 -20%	FY2024 -40%
Participant/Trainee Support Costs	Hiroshima University	40,000	32,000	24,000
Salary - scientific	BNL	26,938	18,289	16,163
Salary - professional	BNL	17,461	13,969	11,220
Equipment	BNL	8,000	8,000	8,000
Travel	Hiroshima University	7,000	7,000	7,000
Materials & supplies	BNL	11,400	11,400	11,400
Materials & supplies	Hiroshima University	7,400	7,400	7,400
Total (w/o overhead)	BNL+Hiroshima Univ.	118,199	98,058	85,183
Total (w overhead)	BNL+Hiroshima Univ.	152,585	127,154	108,989

1. **A realistic nominal budget (baseline budget):** All deliverables presented above will be completed.

2. **A nominal budget minus 20%:** Deliverables other than the following will be accomplished. Testing on probe-stations of the sensors before they are used for module assembly will be limited, as the budget for that FTE will be reduced. The weeks for training at BNL for Japanese collaborators will be reduced, as the budget for support will be cut. A possible budget scenario would be as follows:
    - The FTE for probe-station testing and bonding of chip to sensor will be reduced by 20%, which means limiting the number of bonded sensors and chips and the testing of the sensors before they are used for module assembly.

- The support for training will be cut by 20%, reducing the weeks for training at BNL for Japanese collaborators.
- The FTE associated with supervision of BNL activities will be reduced by 30%.

3. **A nominal budget minus 40%:** Deliverables other than the following will be accomplished. Testing on probe-stations of the sensors before they are used for module assembly will be limited, as the budget for that FTE will be reduced. The weeks for training at BNL for Japanese collaborators will be reduced, as the budget for support will be cut. Participation in the Fermilab beam testing will be limited. Production of additional modules with a new batch of AC-LGAD sensors produced by HPK specifically for this project will be limited. The FTE for supervision of BNL colleagues will be affected. A possible budget scenario would be as follows:
    - The FTE for probe-station testing and bonding of chip to sensor will be reduced by about 36%, which means further limiting the number of bonded sensors and chips and the testing of the sensors before they are used for module assembly
    - The support for training will be cut by 40%, reducing the weeks for training at BNL for Japanese collaborators.
    - The FTE associated with supervision of BNL activities will be reduced by 40%.

A “money matrix” itemizing the budget allocations to the individual institutions, shown on Table-2.

9.0 Cost effectiveness

The project achieves high efficiency and low cost by leveraging the existing expertise, collaboration, and resources of the US and Japanese partners, as well as other funding sources, to develop and test 4D detectors for the EIC. It also takes into account the environmental and social aspects of the project, such as reducing carbon emissions, overcoming supply chain difficulties, and prioritizing domestic suppliers. For example, it uses sensors produced by HPK Photonics, a Japanese company that is the main producer of silicon sensors in the world. It also minimizes travel costs by hosting Japanese colleagues at BNL for training and testing, and by participating in test beams at FNAL and ELPH. It also maximizes the benefits of the project by sharing the results with the EICROC designers and the broader particle physics community, as well as by fostering workforce development and technology transfer in Japan. Moreover, the project plans to bring people together for workforce and development instead of having parallel efforts around the world, thereby saving resources and enhancing collaboration. Furthermore, the project will use equipment and in-house BNL facilities, such as the Silicon Testing Laboratory, the Interconnect Lab, and the machine shop, to save money and ensure high-quality testing and assembly of the modules.

10.0 Facilities & Other resources

The proposed research would not be possible without the unparalleled facilities and expertise of the scientists and engineers at BNL and in the Japanese institutes.

As part of this research project the BNL PI is considering to make use of the following facilities and resources:

• Silicon Testing Laboratory with a probe station and several test-benches.

• Interconnect Lab for wire and bump bonding

• The machine shop

BNL's Silicon Testing Laboratory is equipped with probe stations, a laser system and several types of other equipment as detailed in next section 'EQUIPMENT'. It also includes various radiation sources that emit different types of particle beams, useful to characterize in full the detector performance, e.g. ^{90}Sr, ^{55}Fe, and ^{241}Am sources, such as charge collection efficiency and time resolution.

The BNL's Interconnect Laboratory in the Instrumentation Division is equipped with advanced machines that allow wire and bump bonding of ASICs to sensors and/or PCB. Several inspection instruments are also available, e.g. X-ray scan.

The machine shop in the BNL Physics Department will be used for construction of parts necessary for fixtures for the probe station, measurements with the laser system or radiation sources, to perform adjustments as needed during prototype testing. The machine shop includes technicians and mechanical designers available for the high-energy physics experiments. BNL has in addition a Fabrication Services Group, which has a full-service prototype shop with production capabilities. Facilities include heavy machine, wire EDM, welding, and sheet metal shops with the capability of working from miniature to 20-ton assemblies.

11.0 Equipment

For the characterization of silicon devices the BNL PI will use the Silicon Testing Laboratory which includes several test-benches, a probe station and other types of equipment as detailed below.

A system that allows the application of the so-called Transient Current Technique (TCT). The TCT system at BNL comprises infrared and red lasers of 640 and 1064 nm wavelengths and three stages with micron precision in x, y and z directions together with an amplifier and a Bias-T for powering and reading out the devices under study. In addition this system is equipped with a cooling system for low temperature studies, particularly useful after irradiation.

For AC-LGAD characterization the BNL team will utilize a 4-channel fast oscilloscope (LeCroy Waverunner 9404M-MS), an Evaluation-Board DRS4 V5 produced by PSI, Switzerland, a pre-amplifier designed and built at BNL, a Keithley high voltage power supply, a multichannel analyser, a probe station equipped for current-voltage (IV) and capacitance-voltage (CV) analyses that can operate at room temperature as well as cold at -30 ℃. A telescope will be used for studies of sensor response under particle beams from ^{90}Sr radiation sources, while ^{55}Fe and ^{214}Am sources will be also available.

In addition, a variety of instruments, readout electronics and DAQ system test-stands as well as a vast array of instruments including signal generators, analyzers, high performance oscilloscopes, precision impedance meters and environmental chambers will be available in Physics Dept. and in Instrumentation Div. for this project.

Synergetic will be the major commitment that BNL has taken in the construction and assembly of the ITk barrel Strip detector. More specifically, BNL has taken the responsibility of assembling half of the ITk Barrel Strip modules and is the only institute in the United States to assemble modules on staves, i.e. mechanical structures with electrical and cooling components that host 28 modules, before they are shipped to CERN for the final installation. As part of this activity two clean rooms of class 10,000 were built in the BNL Physics Department and are equipped with instruments and machines, such as for visual inspections, metrology, wire bonding etc. of which this project may benefit. The expertise that the ITk assembly team has acquired on silicon modules and their electronics will also provide an extremely valuable contribution to this project too.

12.0 Promoting Inclusive and Equitable Research (PIER) Plan

Section I: Diversity, Equity & Inclusion at Brookhaven National Laboratory

An inclusive environment and diverse workforce are crucial for Brookhaven National Laboratory (BNL) to successfully pursue its mission on behalf of the U.S. Department of Energy's Office of Science.

Innovation requires a work environment that promotes diversity of thought and perspective, allowing employees to feel valued and to flourish through an inclusive work environment respecting everyone's input. The Laboratory promotes equity to ensure that historically underrepresented or underserved people in Science, Technology, Engineering, and Mathematics (STEM) have the opportunity to grow, contribute, and develop thereby being their authentic selves. We do this by ensuring consistency in our employment practices, and by promoting collaboration, and fairness.

The Diversity, Equity, & Inclusion (DE&I) Office at BNL supports the Laboratory's mission to perform world-class science by facilitating the development of a pipeline of qualified, diverse candidates, ensuring equitable treatment for all employees, and helping to create an environment that encourages respect for individual differences through inclusivity. The Lab has also developed cross-functional DE&I councils and committees throughout its operations to effectively advance DE&I efforts at central and local levels.

There are numerous diversity policies at BNL which we adhere to. These include:

- Anti-Sexual Harassment Policy
- Brookhaven Veterans Policy
- Equal Opportunity & Affirmative Action Policy
- Respectful Workplace Policy
- Anti-Retaliation Policy
- Workplace Lactation Program

Brookhaven's Talent Acquisition team, DEI Office, and Office of Educational Programs (OEP) collaborate to establish pathways for undergraduate and graduate students through workforce development and "Expanding the Circle of Peers" programs, such as a memorandum of understanding (MOU) with minority-serving institutions (MSIs) to foster collaborations with faculty members and develop student access.

BNL is focused on implementing an array of growth and development opportunities for early-career and postdoctoral researchers to attract and retain diverse, high-quality talent. These initiatives include a Science and Engineering Development Program for early-career researchers focused on exposure to senior scientific leaders, deepening understanding of how the laboratory operates, conduct of research, engagement with funding agencies, proposal writing, communicating science, and professional networking and growth.

Section II: PIER practices and DEI activities that will be used in this proposal:

The principal investigator Tribedy, has a strong commitment to promoting inclusive and equitable research (PIER) in all aspects of their work, based on their experience supervising graduate and postdoctoral advisees from diverse backgrounds. The PI has also worked in large experimental collaboration STAR, composed of 71 institutes from 14 countries, with a total of 715 collaborators. The PI has a research experience of nearly seven years in India and another seven years in the USA. Additionally, the PI has actively engaged in promoting PIER through outreach programs and volunteer work, such as supervising undergraduates and minors as high-school students in the summer program. Specifically, the PI has been involved in the outreach program at BNL and the World Science Festival, as

well as volunteering for the Stony Brook National Chapter of Black Physicists. These experiences have further strengthened the PI's commitment to promoting PIER and provided valuable insights and skills that they will apply to their research projects.

The PI will implement existing BNL policies, training, and code of conduct to foster a psychologically safe and respectful workplace for all members of the Consortium to feel their authentic selves. The PI will ensure frequent communication among all staff, daily, including feedback to leadership from students and postdocs. He will utilize BNL's training resources to ensure all staff working on the project are trained in DEI. Half way through the project, he will survey the people in the Consortium to assess whether he and his senior collaborators have been successful at creating the desired environment.

The PI has annually offered internship summer programs to undergraduate university students from several international universities, and he plans to continue this tradition in the coming years. Tribedy has been participating variously in the supervision of graduate students from US and abroad under the NP program. Among other members of this proposal, Tricoli, as co-investigator of the DOE Traineeship program in HEP instrumentation for PhD students from Brown and Princeton Universities, he will ensure all the participating students are well trained and mentored, and will provide guidance to their growth as physicists and as citizens by following the DEI principles.

Tribedy and Tricoli are also considering hosting a Science Undergraduate Laboratory Internship (SULI) or Community College Internship (CCI) Student. In the year 2023, Tribedy is already supervising one SULI student. The DOE's SULI program encourages undergraduate (two- and four-year) students to pursue STEM careers by providing research experiences at a DOE laboratory. The SULI program provides interns the opportunity to work under the guidance of scientific and engineering staff on projects that are relevant to the DOE mission of ensuring America's security and prosperity by addressing its energy, environmental, computational, and nuclear challenges through transformative science and technology solutions. The DOE's CCI program encourages 2-year college students to enter technical careers by providing training experiences at a DOE laboratory.

As a testimony of his commitment to diversity, one of his students was awarded the prestigious BNL's Gertrude Scharff-Goldhaber Women in Science Prize in 2022. In his recruitment of students the PI will pay special attention to diversity and promote gender balance. As a testimony of his dedication to this cause, about half of the students he has recruited were female, and were of diverse geographical origins, e.g. Italy, UK, India, China. When seeking institutional collaborators for this project, the PI will consider Minority-Serving Institutions (MSIs) as part of the search.

The PI promotes visibility and exposure of young members of his team to the scientific community, by inviting them to give conference or workshop presentations, and be first authors in co-authored scientific papers in which they have given substantial contributions. In addition, he will ensure the students and postdocs will receive the appropriate training to accomplish the assigned research and to prepare them to excel in their future career as physicists or engineers, or in the private sector. One of Tribedy's former Ph.D. students has established himself as a postdoctoral researcher at LBNL, and another has also become a faculty member in India. Tricoli's students have historically succeeded in their careers by graduating in prestigious universities, e.g. Oxford University among others, and several have continued their studies in PhD programs, for example a student of minority descent has been admitted in the robotic PhD program at Princeton University. To facilitate the training and mentoring he encourages the senior students and postdocs to help with the training of the youngest members of the team. This also trains the most senior

members of his early-career team to create a friendly and cohesive atmosphere in the group and practice their teaching skills.

In all the meetings that he arranges, the PI is cognisant to build a diverse agenda that is balanced between gender, diverse in regional origins of the speakers, and ensures that hearing-impaired participants are supported with the best possible close-captioning tools. A testimony of his dedication to this cause are the Snowmass meetings he arranged that were not only balanced on gender and geographical origin, but the WhiteCat close captioning service was also provided by the PI, and supported by the BNL DEI office.

The PI is active in outreach in the local Long Island community, as he arranged multiple public events on science in local public libraries and on podcasts, and has arranged events for high school students at BNL. He plans to continue with such effort during the period of this project and will invite students and postdocs in the Consortium to do the same.

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