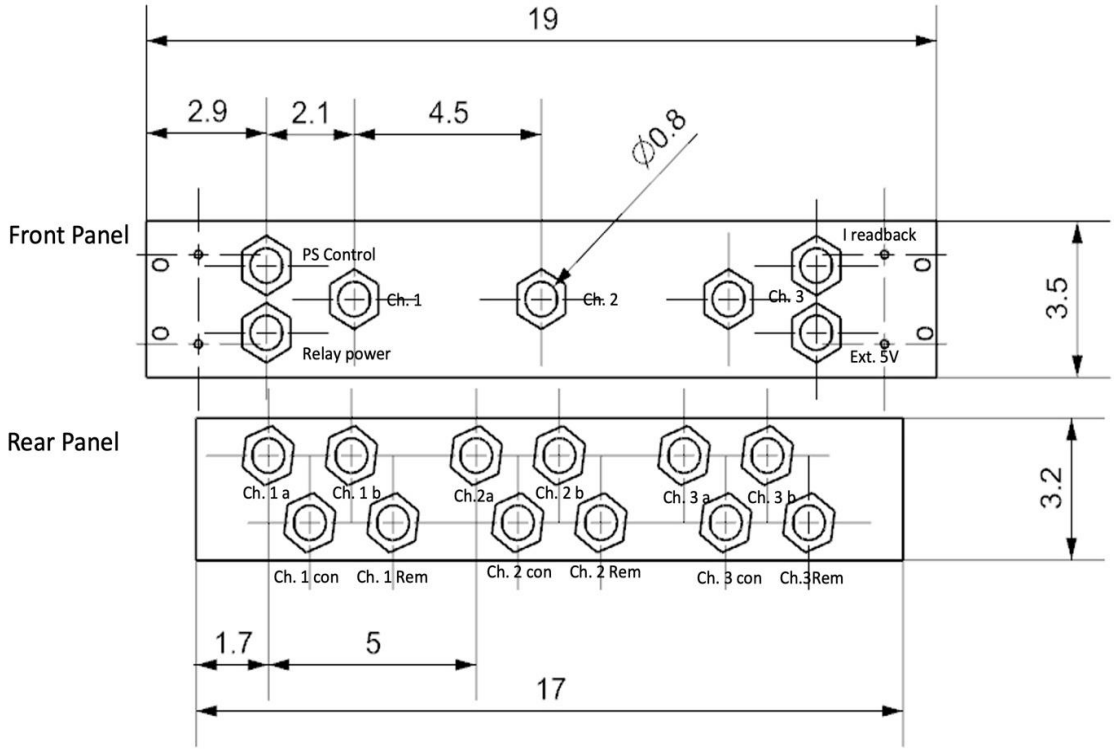
Hall A – ECAL

Marc McMullen

- Drew manufacturing design of front and rear panels with connector holes for the power supply controls interface chassis
    - ✶ Front has seven connectors— power supply control, relay power control, current readback, 5 V input, and three output power
    - ✶ Rear has 12 connectors— six power input (only three are connected), three remote and standby (both is same cable), and three power supply control



Drawing of the front and rear panels of the power supply interface chassis

Hall A LAPPD

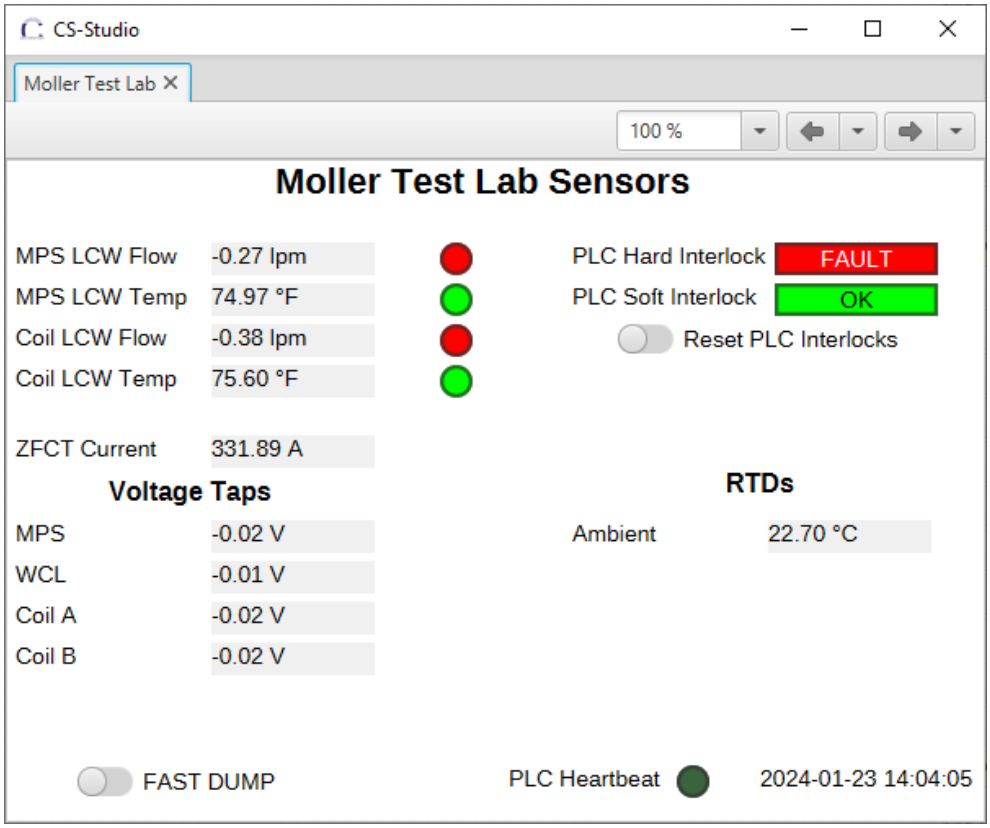
Marc McMullen

- Started 3D model of the detector test stand

Hall A – Møller

Brian Eng

- Continued setup of test of TM3 magnet power supply (MPS), which is connected to coil A and coil B of TM4
    - ✶ Connected voltage taps to iso amps MPS output, water cooled lead (WCL) output+, coil A, and coil B
    - ✶ Connected five of seven RTDs: coil A supply and return, coil B supply and return, and ambient; missing WCL supply and return
    - ✶ Made testing Phoebus screen to monitor values (not via PLC)



Phoebus screen to monitor values.

Hall B – ALERT

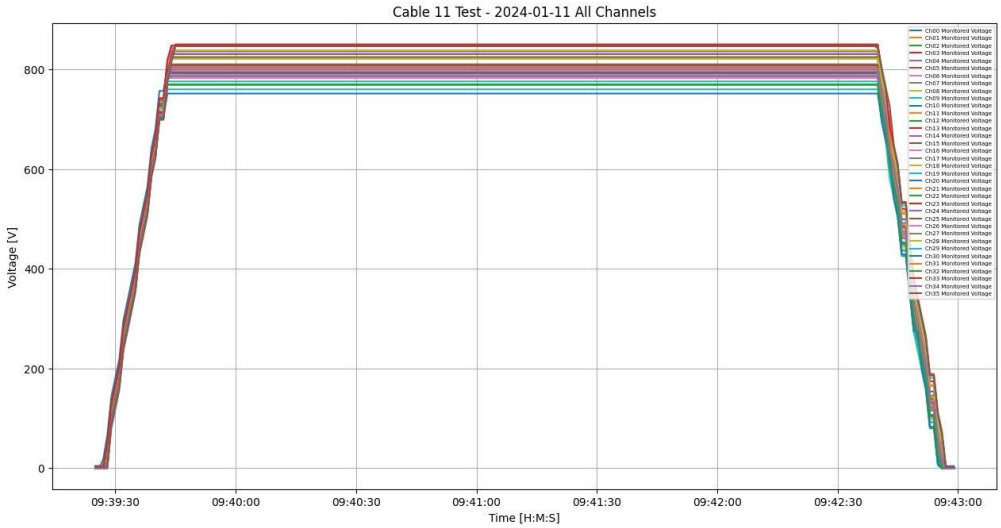
Brian Eng, George Jacobs, and Marc McMullen

- Using fitting specifications for MFCs and pressure transducers, calculated flow rates for MFCs

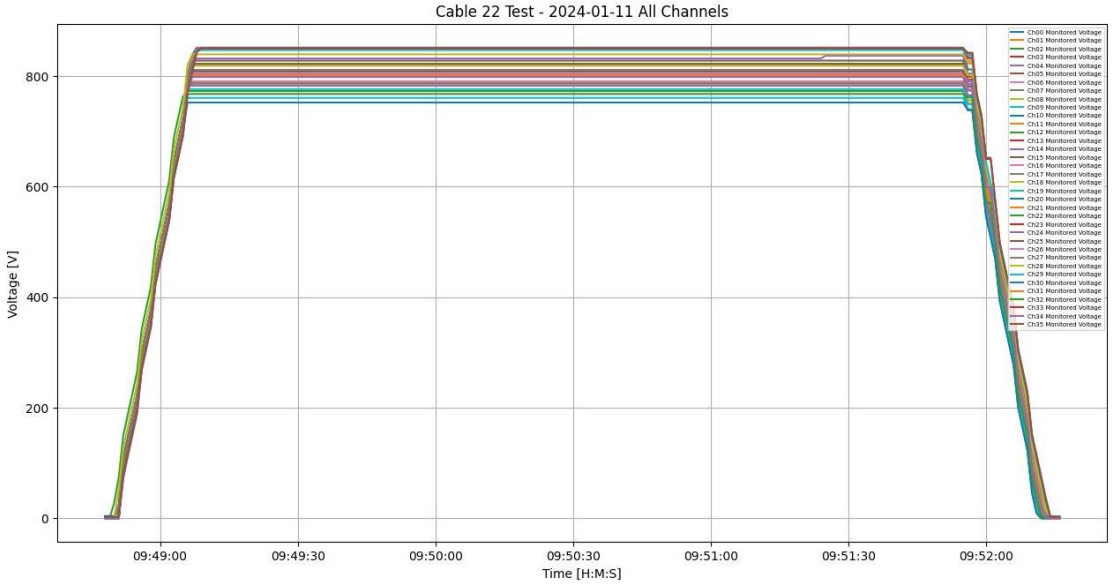
Hall C – NPS

Mary Ann Antonioli, Peter Bonneau, Aaron Brown, Pablo Campero, and Tyler Lemon

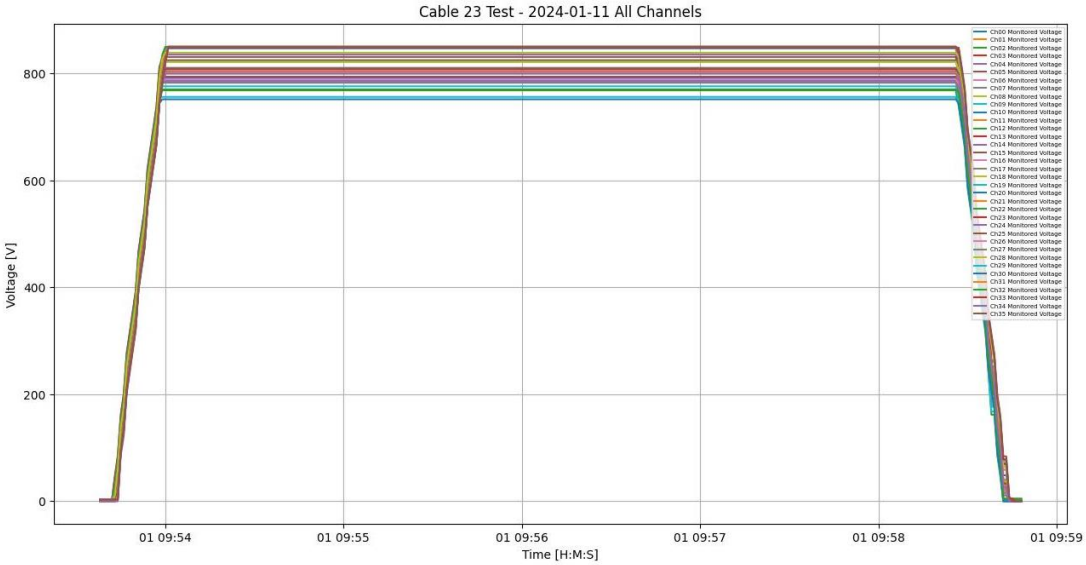
- Debugging control and monitoring LabVIEW program, vers. 2
  - ✶ Combined all interlock enables into one array and averaging enables into one array; made resulting needed changes to subVIs. Interlock enable and averaging enable now disable when sensor is disabled, as required
  - ✶ Made changes to the configuration file utility subVI to account for the changes in array sizes and initialization order
  - ✶ Fixed permission issue that was preventing new configuration files from being written
  - ✶ Debugging loss of initialization in trip and interlock times
- Analyzing data from high voltage supply cable testing
  - ✶ Generated plots of voltage and current for all channels of cables #11, #22, #23, and #26; cable #26, channels #16, #26, #30, and #31, are the only problem



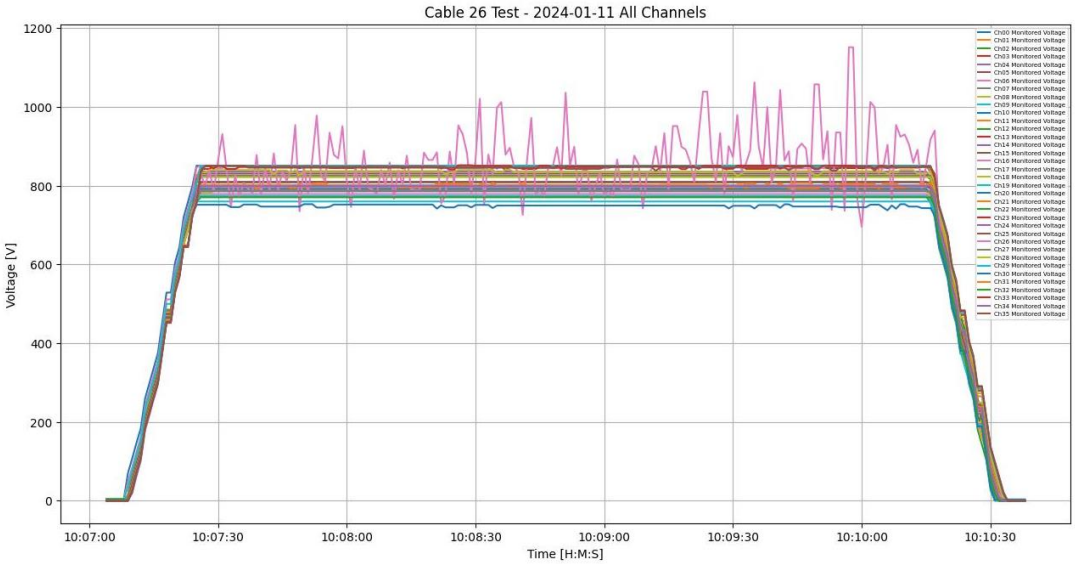
Voltage for all channels of cable #11.



Voltage for all channels of cable #22.

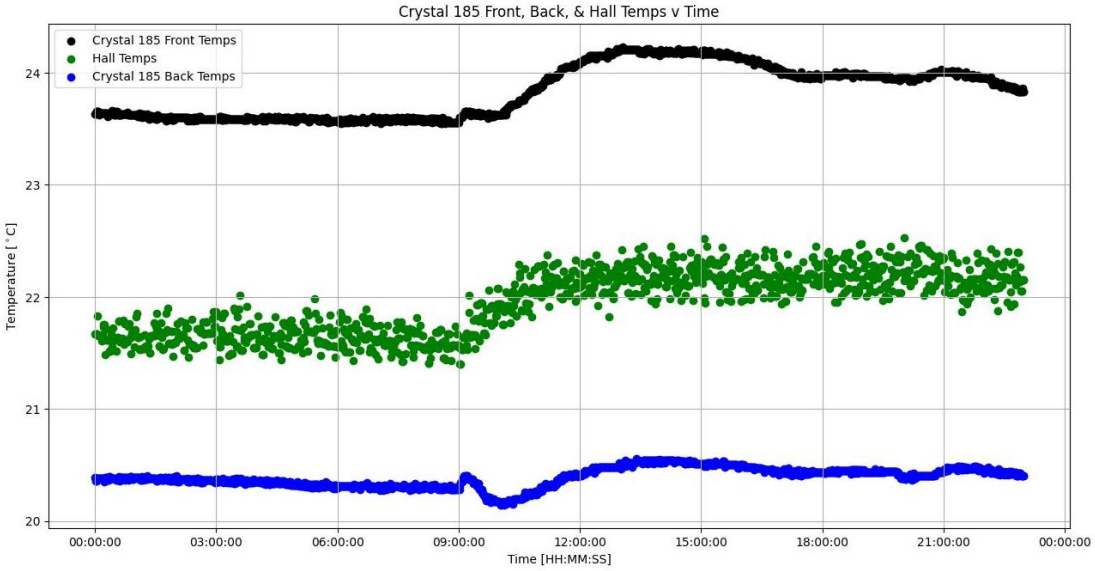


Voltage for all channels of cable #23.

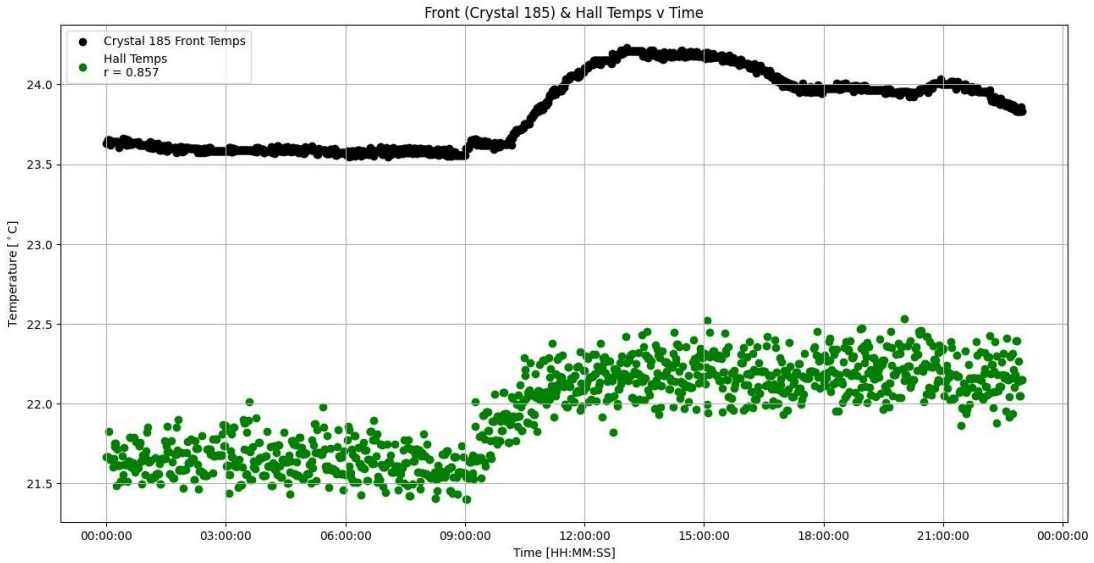


Voltage for all channels of cable #26.

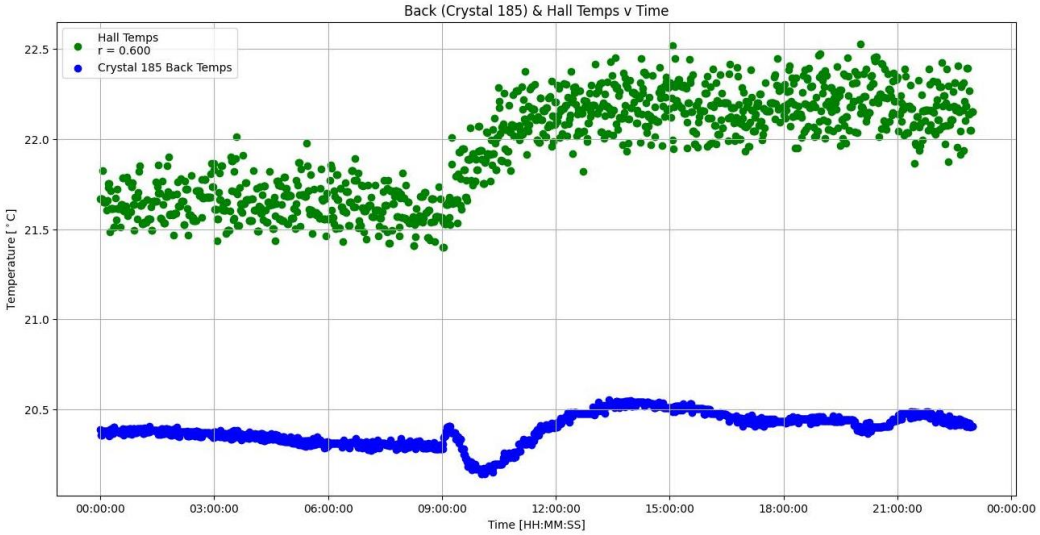
- Generated plots of crystal 185 temperatures vs ambient temperatures; data confirms that the crystal temperature is determined by the ambient temperature



Crystal 185 front and back temperatures and ambient temperatures.



Crystal 185 front temperatures and ambient temperatures.



Crystal 185 back temperatures and ambient temperatures.

Hall D – FCAL2

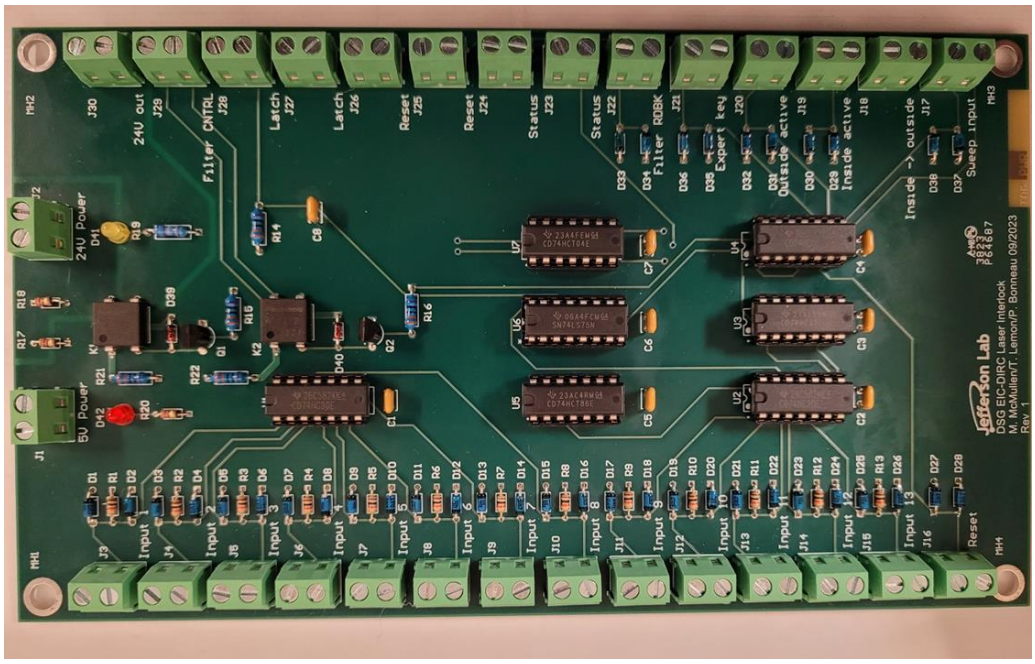
Mindy Leffel

- Populated 60 PMT bases; Completed 1300 of 1650
- Cut 120 wires

EIC - DIRC

Peter Bonneau, Brian Eng, George Jacobs, Mindy Leffel. Tyler Lemon, and Marc McMullen

- Completed populating laser interlock board



Populated laser interlock board.

- Completed Phoebus alarm system test code to independently test alarm system using two Phoebus development computers
    - ✶ First computer functions as an EPICS softIOC server and simulates the cRIO laser interlock process variables; the second monitors the interlock process variables for alarm conditions via the network and Phoebus
    - ✶ Setting up networking for the test